

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M core logic

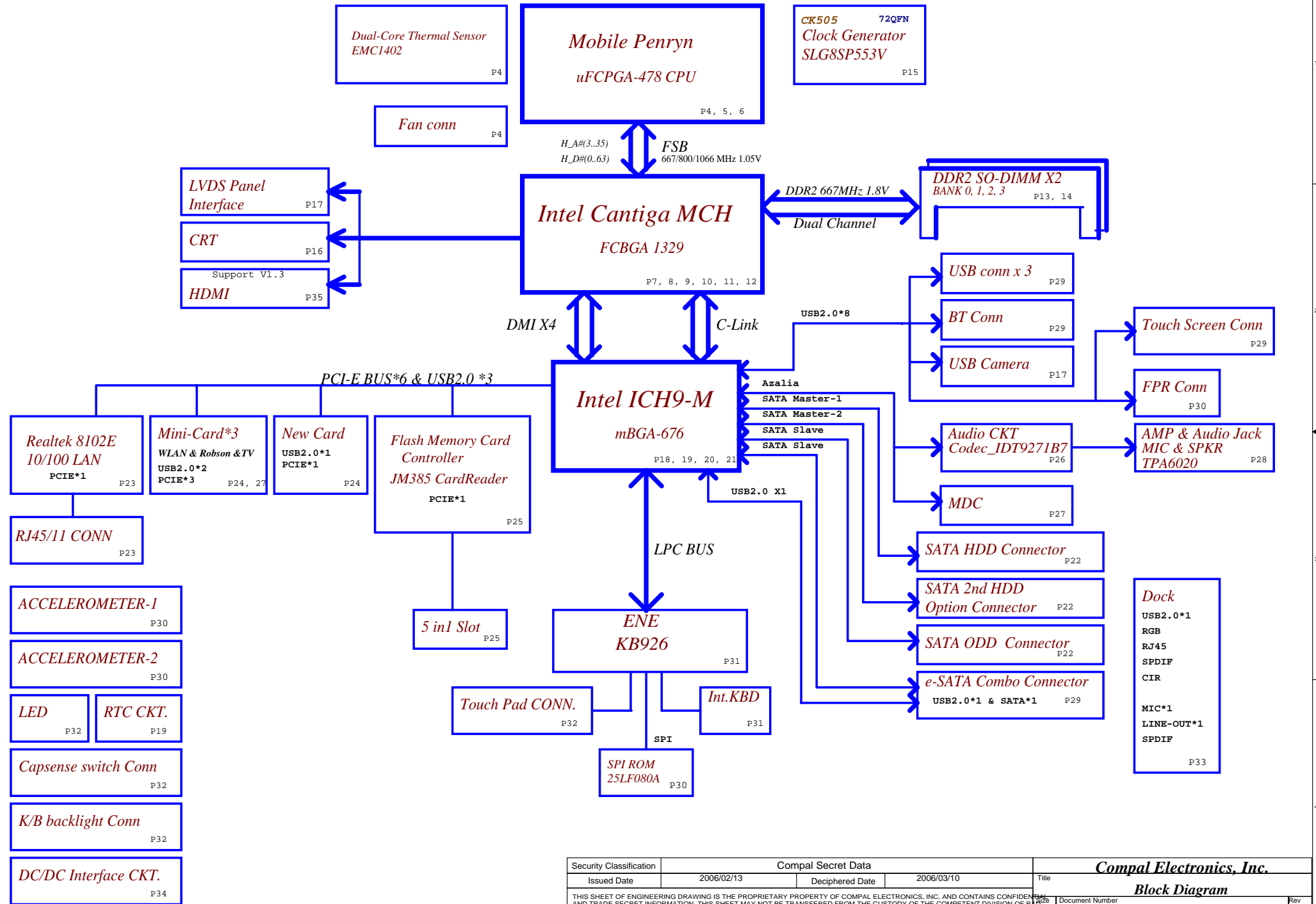
2008-05-22

REV : 0.3



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				Montevina Consumer UMA	0.3
				Date: Friday, May 23, 2008	Sheet 1 of 44

Montevina Consumer UMA



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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Block Diagram	
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				Montevina Consumer Discrete	0.3
				Date: Friday, May 23, 2008	Sheet 2 of 44

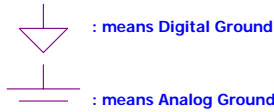
Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

USB assignment :	PCIe assignment :
USB-0 Right side port	PCIe-1 WLAN
USB-1 Right side port	PCIe-2 Robson
USB-2 Left side port (combo with ESATA)	PCIe-3 TV-tuner
USB-3 Dock	PCIe-4 LAN
USB-4 USB Camera	PCIe-5 Card reader
USB-5 WLAN	PCIe-6 New card
USB-6 Bluetooth	
USB-7 Finger Printer	
USB-8 TV-tuner	
USB-9 New card	
USB-10 Left side port	
USB-11 Touch screen	

Symbol Note :



45@ : stuff when 45 level assembly.
 @ : just reserve , no stuff.
 DEBUG@ : reserve for debug only.

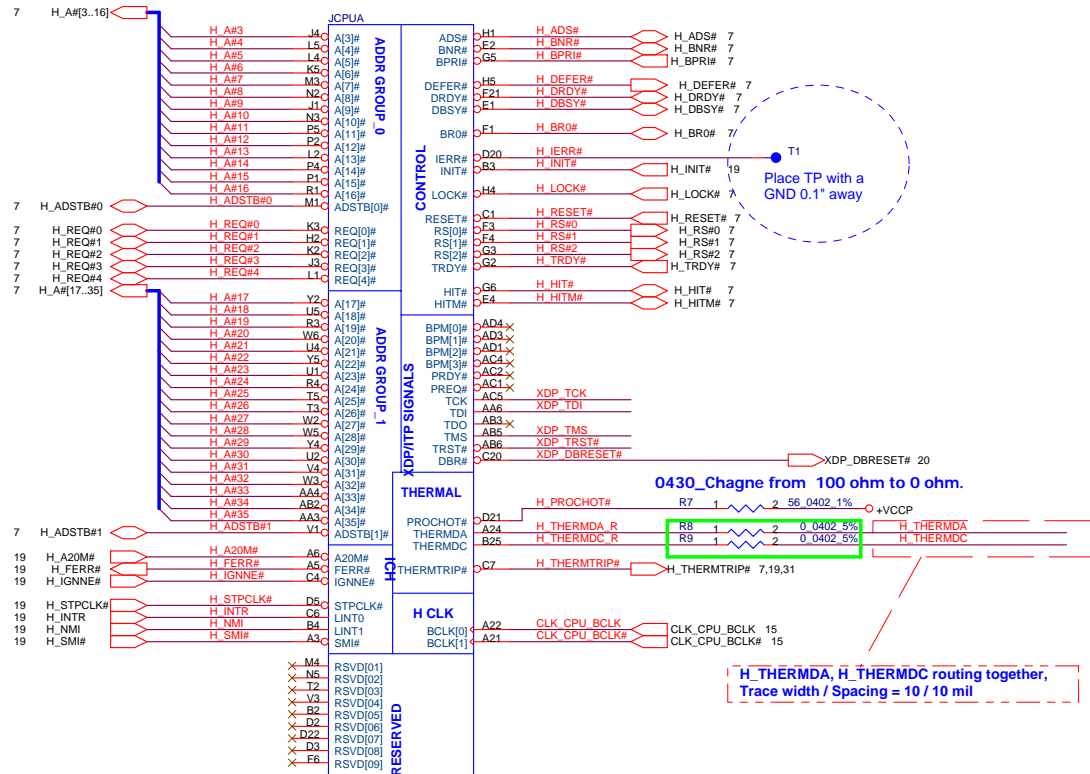
SMBUS Control Table

	SOURCE	INVERTER	Battery	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK Gen.	MINI CARD	LCD	Cap.board
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V _{CY}
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X
ESB_CLK ESB_DAT	KB926	X	X	X	X	X	X	X	X	V _{ENE}
DDC2_CLK DDC2_DAT	North Bridge	X	X	X	X	X	X	X	V	X
ICH_SMBCLK ICH_SMBDATA	South Bridge	X	X	X	X	V	V	V	X	X

I2C / SMBUS ADDRESSING

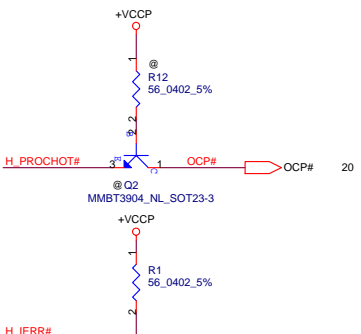
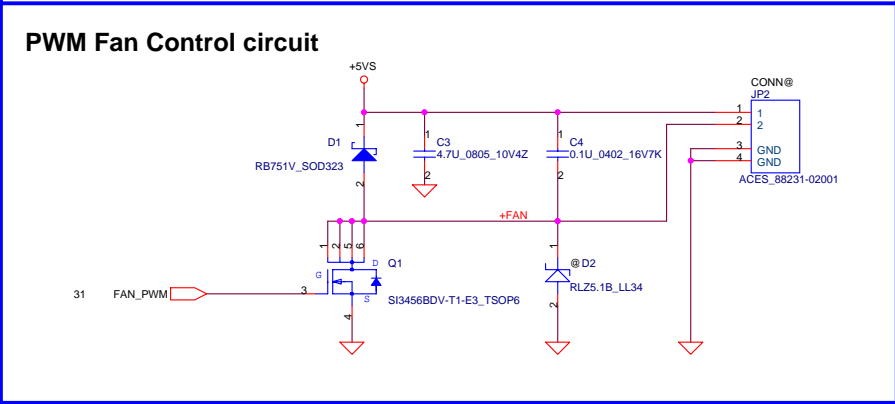
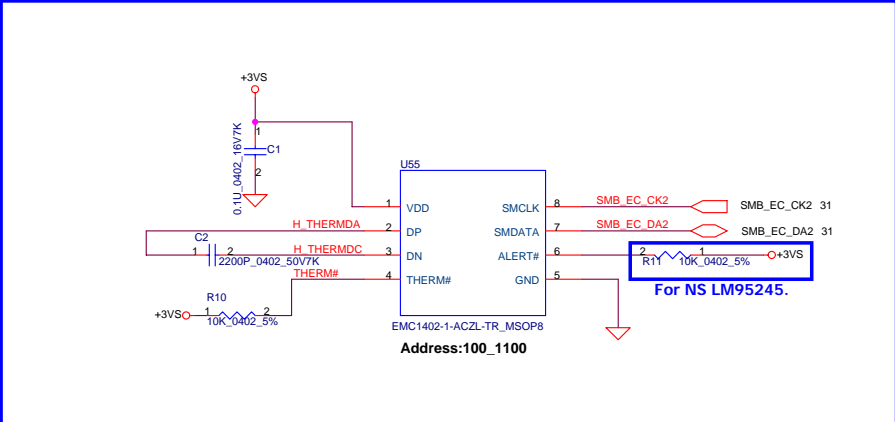
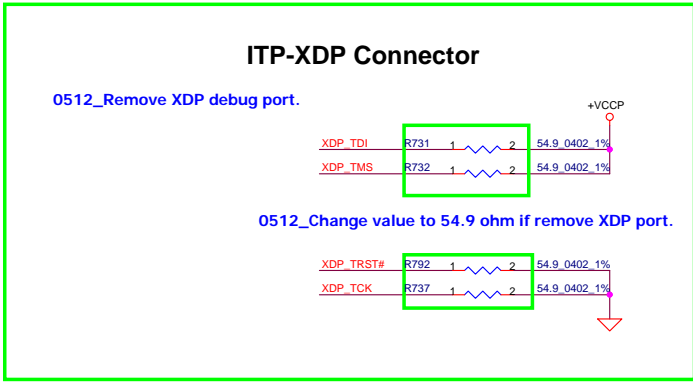
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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				Montevina Consumer Discrete		
				Date: Friday, May 23, 2008	Sheet	3 of 44

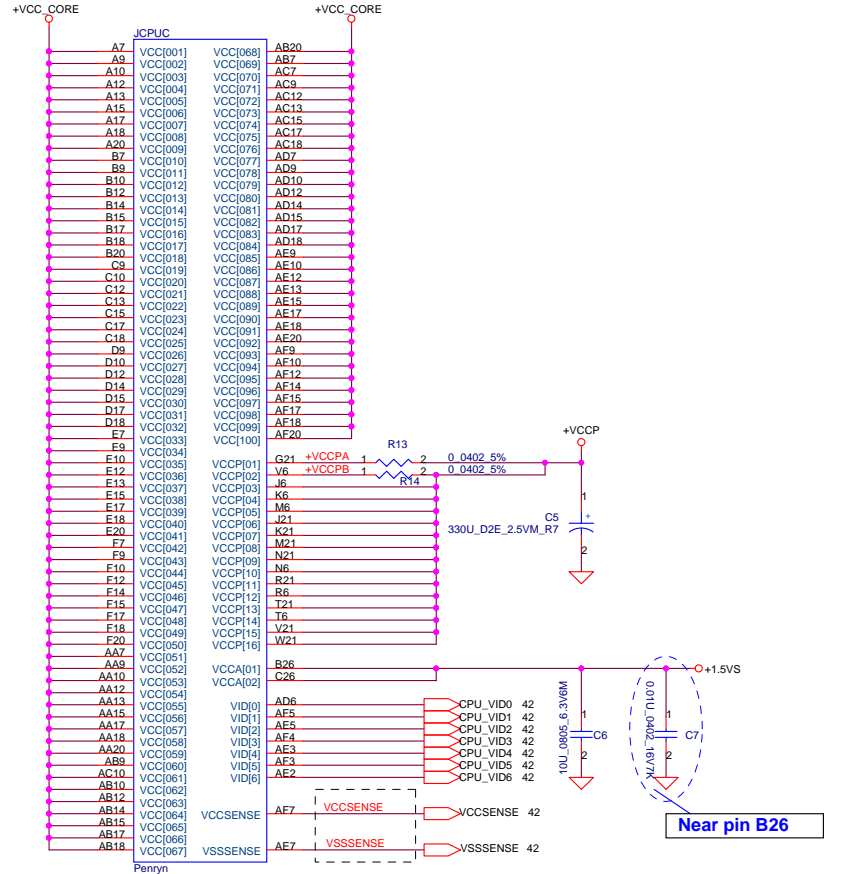
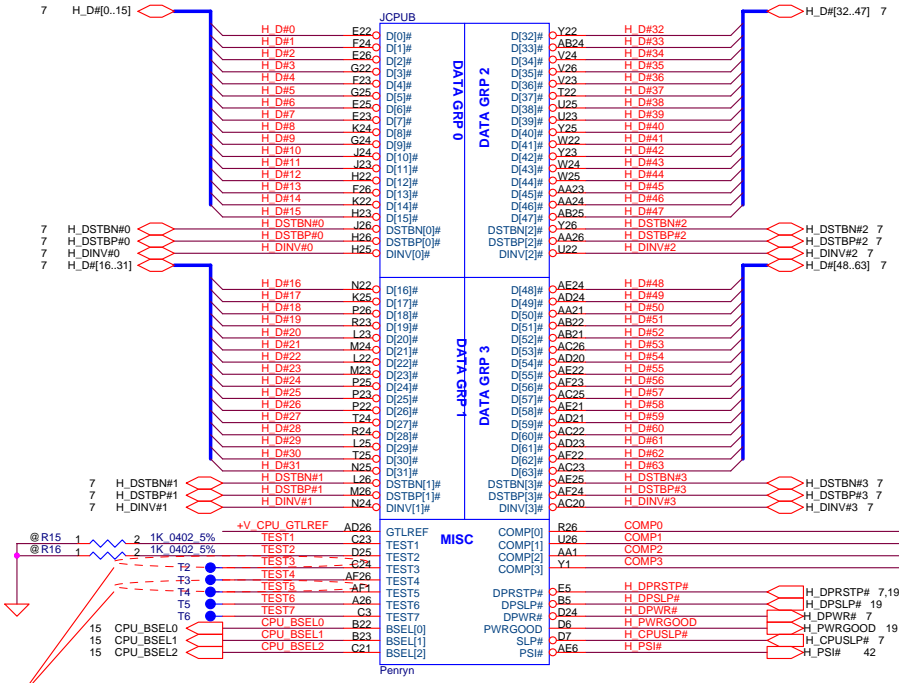


0430 Chagne from 100 ohm to 0 ohm.

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil



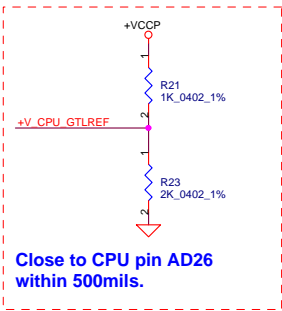
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				Montevina Consumer Discrete	0.3
				Date: Monday, May 26, 2008	Sheet 4 of 44



* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

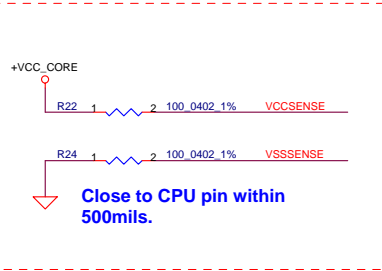
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



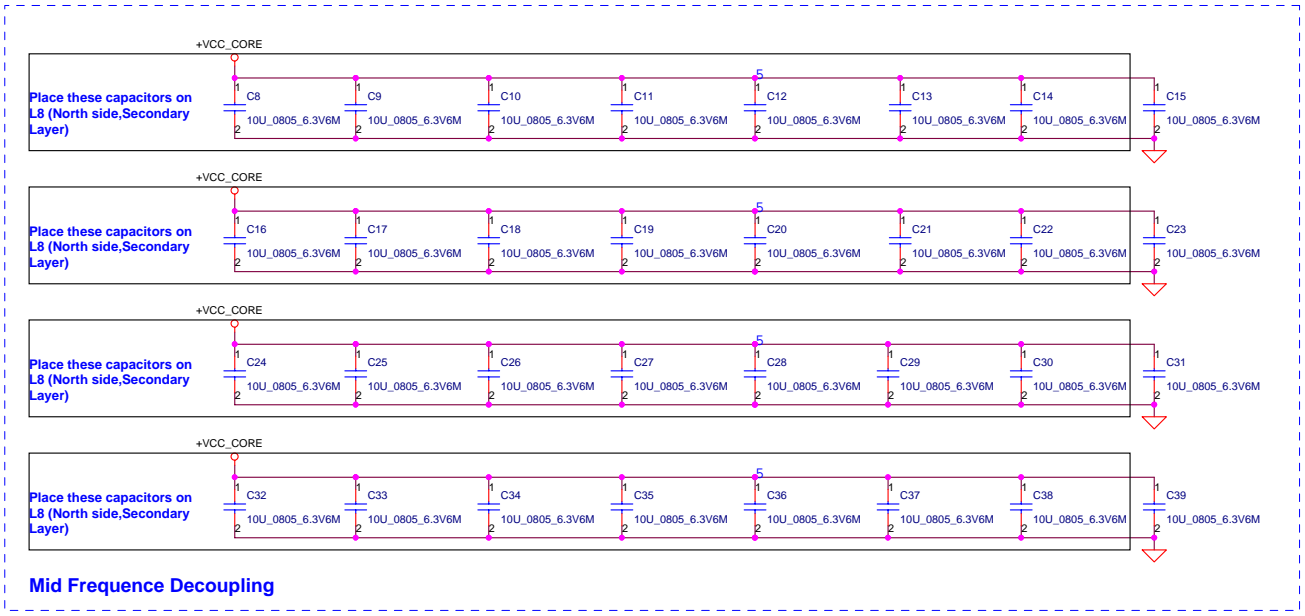
Close to CPU pin AD26 within 500mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.



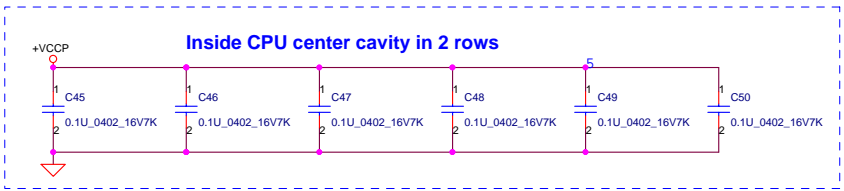
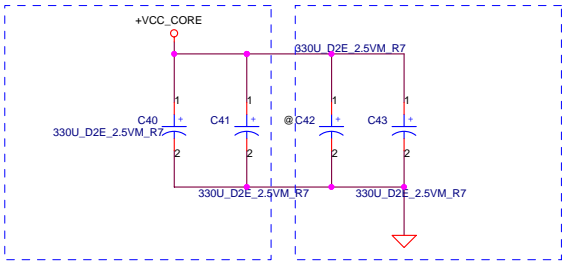
Close to CPU pin within 500mils.

JCPUID		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
AE2	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C2	VSS[023]	VSS[104]
C22	VSS[024]	VSS[105]
C25	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[030]	VSS[111]
D16	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
ER	VSS[037]	VSS[118]
E11	VSS[038]	VSS[119]
E14	VSS[039]	VSS[120]
E16	VSS[040]	VSS[121]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
E24	VSS[043]	VSS[124]
F5	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F2	VSS[050]	VSS[131]
F22	VSS[051]	VSS[132]
F25	VSS[052]	VSS[133]
G4	VSS[053]	VSS[134]
G1	VSS[054]	VSS[135]
G23	VSS[055]	VSS[136]
G26	VSS[056]	VSS[137]
H3	VSS[057]	VSS[138]
H6	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J5	VSS[062]	VSS[143]
J22	VSS[063]	VSS[144]
J25	VSS[064]	VSS[145]
K1	VSS[065]	VSS[146]
K4	VSS[066]	VSS[147]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L3	VSS[069]	VSS[150]
L6	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
L24	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]
		VSS[163]

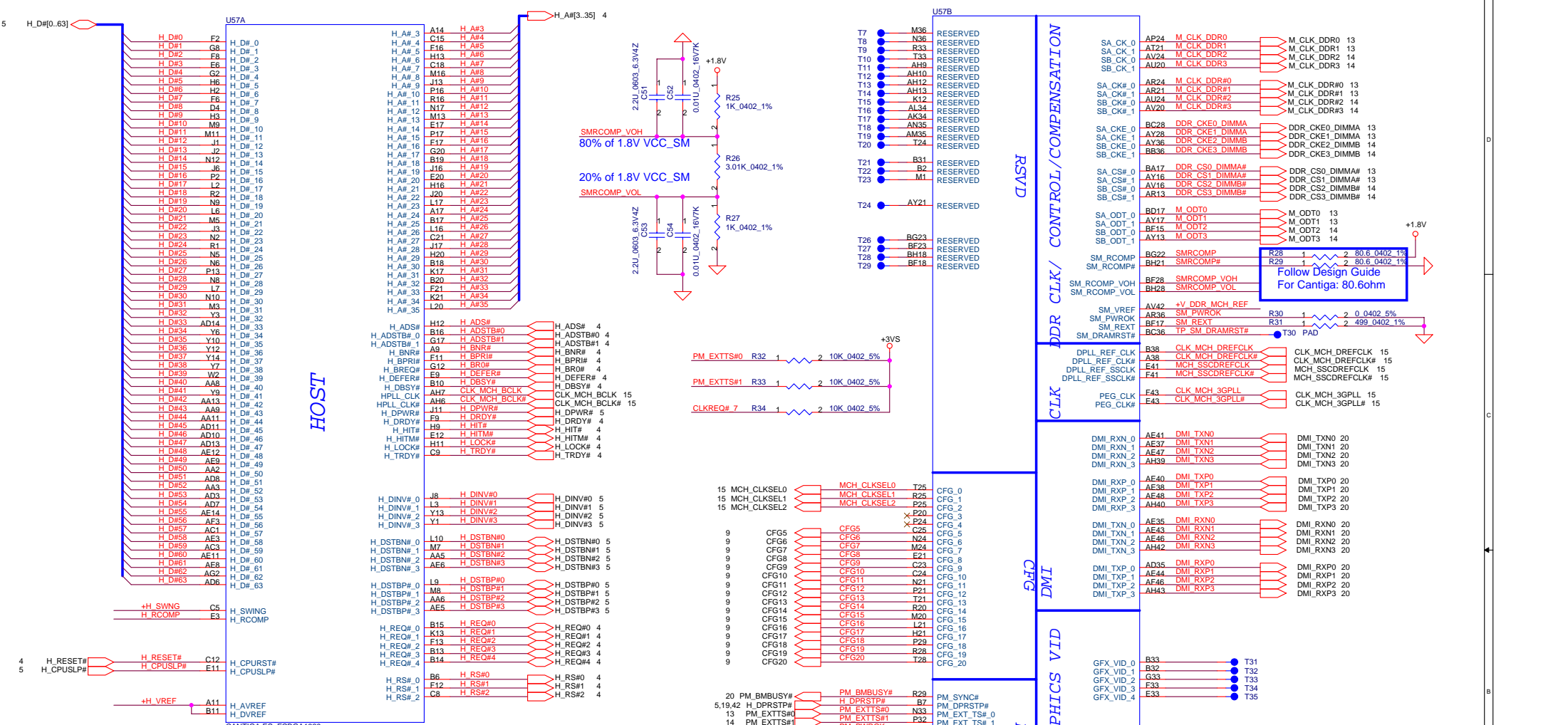


Mid Frequency Decoupling

Near CPU CORE regulator
ESR <= 1.5m ohm
Capacitor > 1980uF

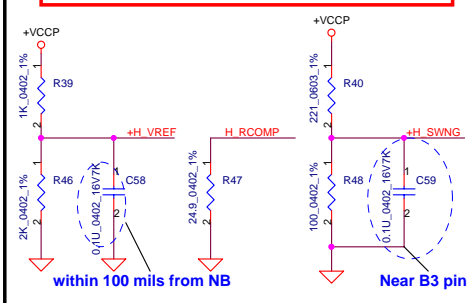


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				Montevina Consumer Discrete	0.3
Date: Monday, May 26, 2008				Sheet	6 of 44

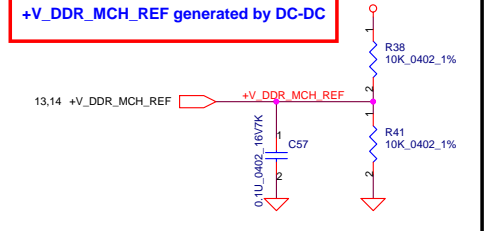


Layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

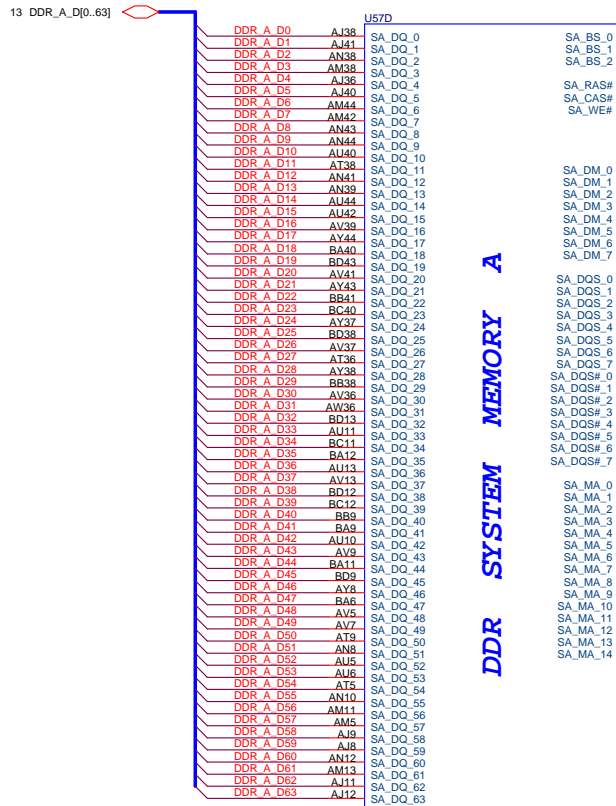
Layout Note:
H_RCAMP / H_VREF / H_SWNG trace width and spacing is 10/20



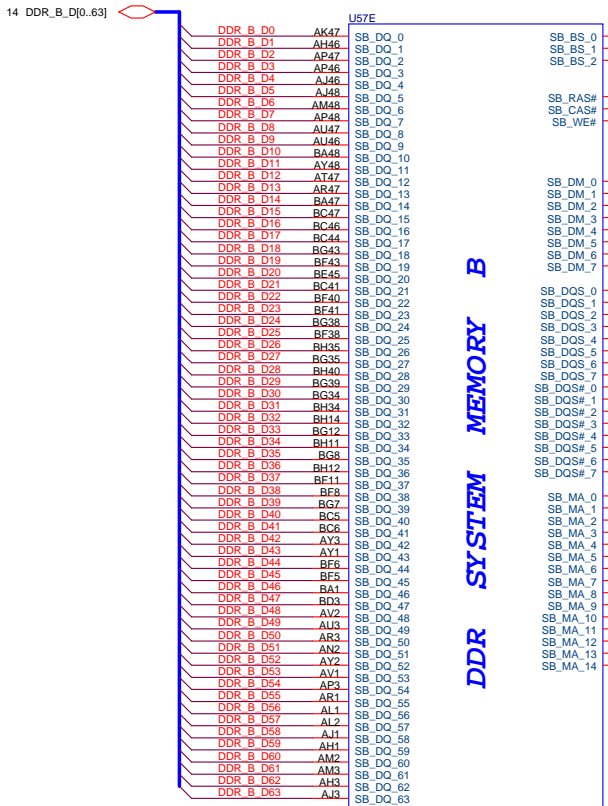
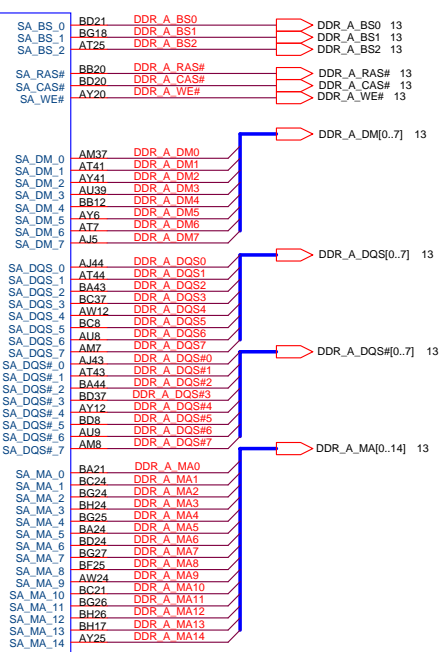
Layout Note:
V_DDR_MCH_REF trace width and spacing is 20/20



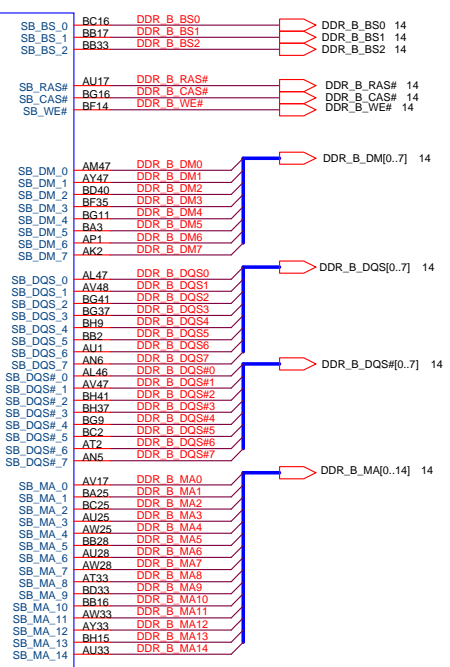
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Customer	Montevina Consumer Discrete	Document Number	Cantiga(1/6)-AGTL/DMI/DDR	Rev 0.3
Date	Friday, May 23, 2008	Sheet	7	of 44



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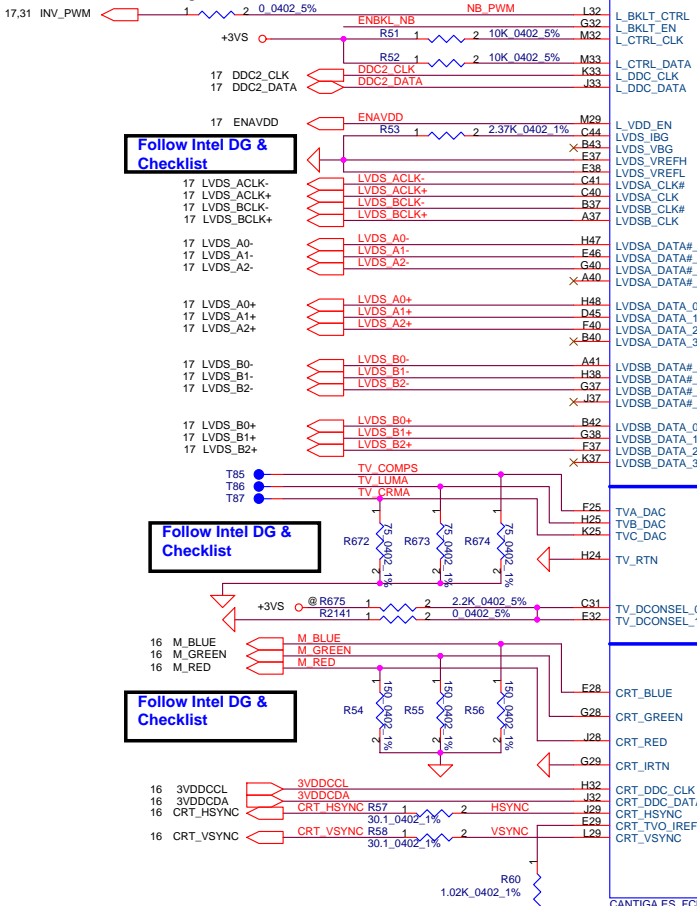


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Reserve for Intel DPST function.



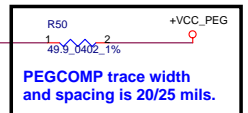
Follow Intel DG & Checklist

Follow Intel DG & Checklist

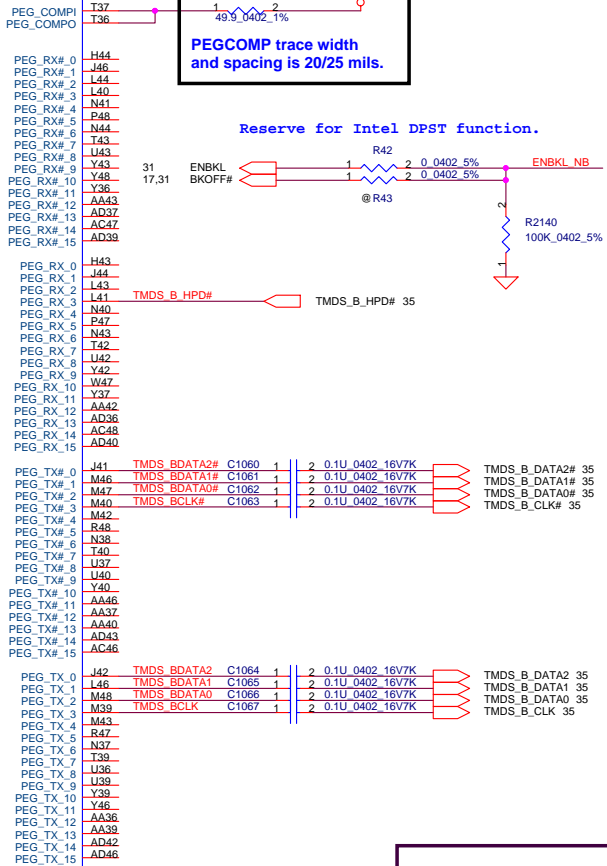
Follow Intel DG & Checklist

0430_Remove C1018-C1025 (Reserve for WWAN issue)

Solve 3G WWAN issue

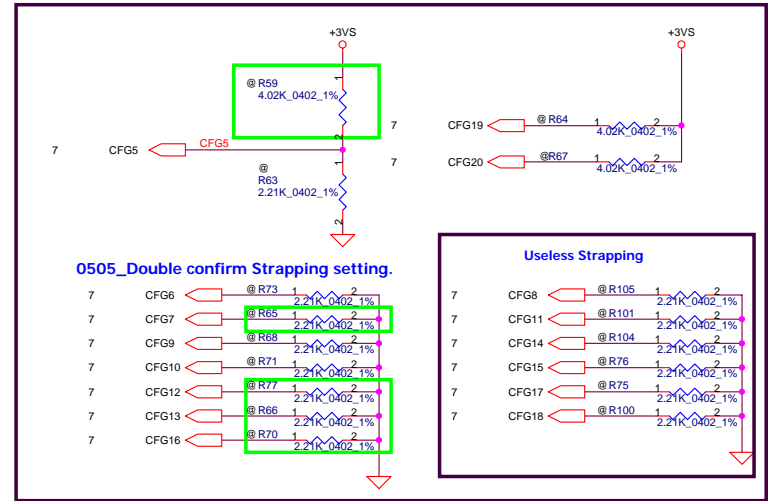


Reserve for Intel DPST function.



Strap Pin Table

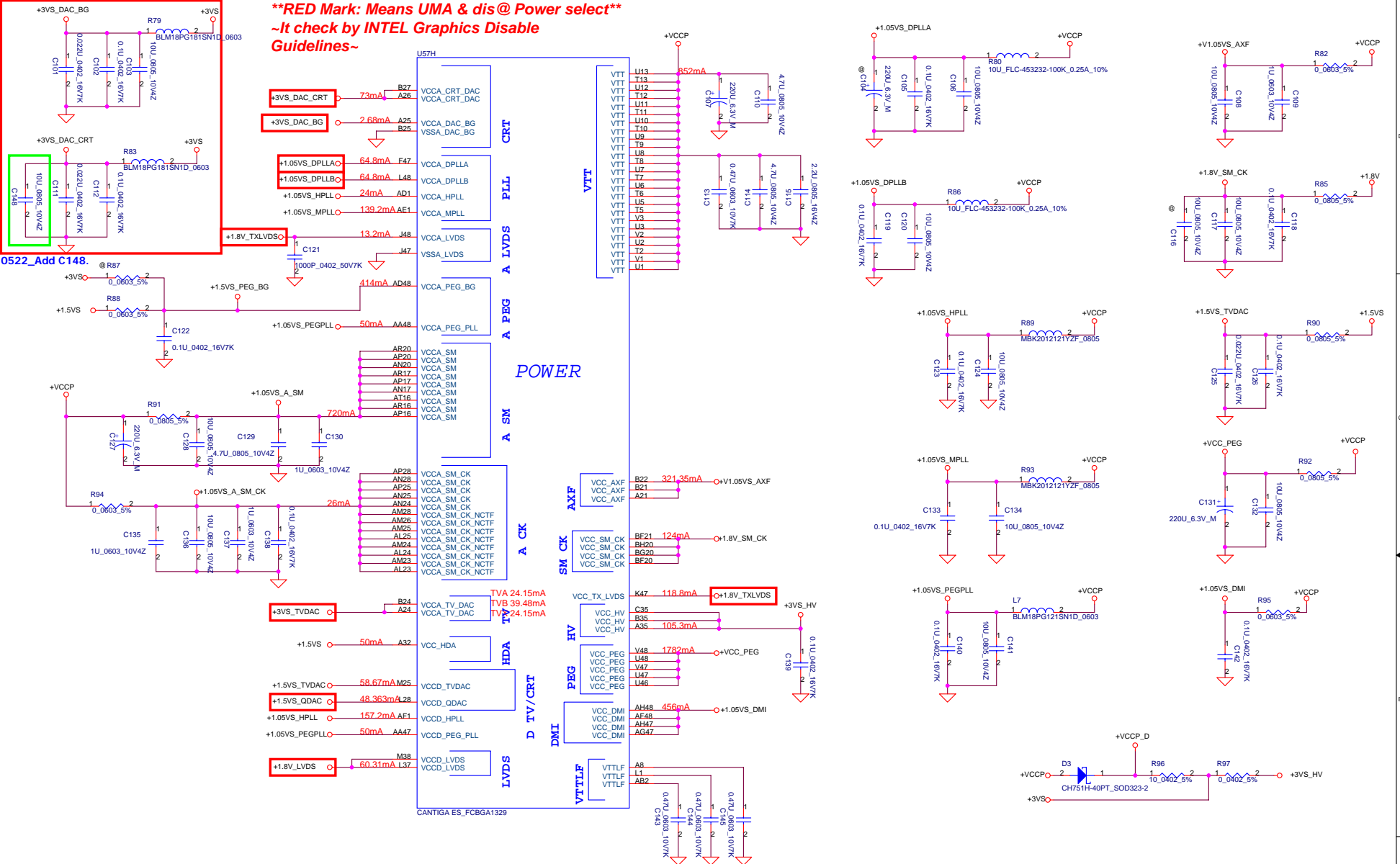
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane, 15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



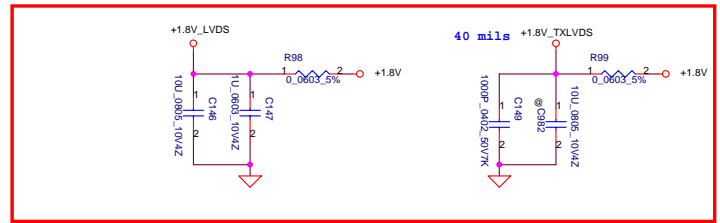
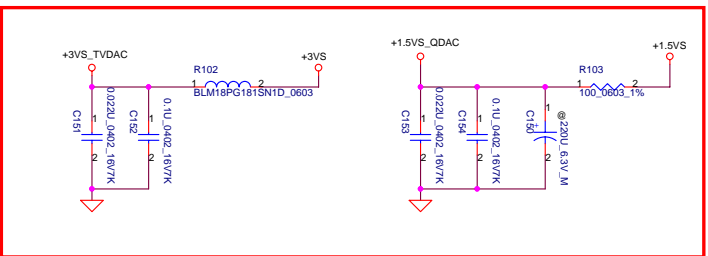
0505_Double confirm Strapping setting.

Useless Strapping

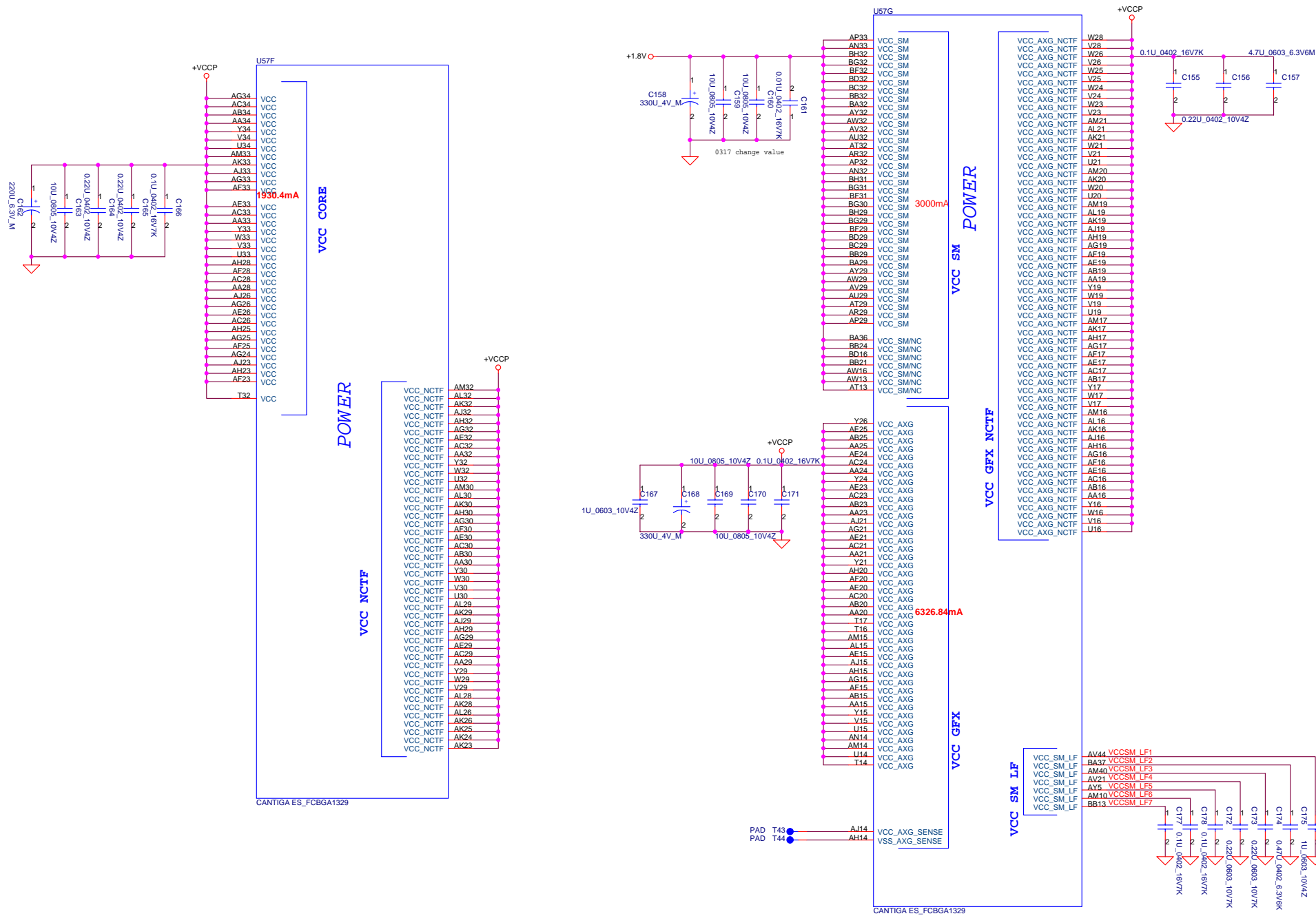
****RED Mark: Means UMA & dis@ Power select****
~It check by INTEL Graphics Disable Guidelines~



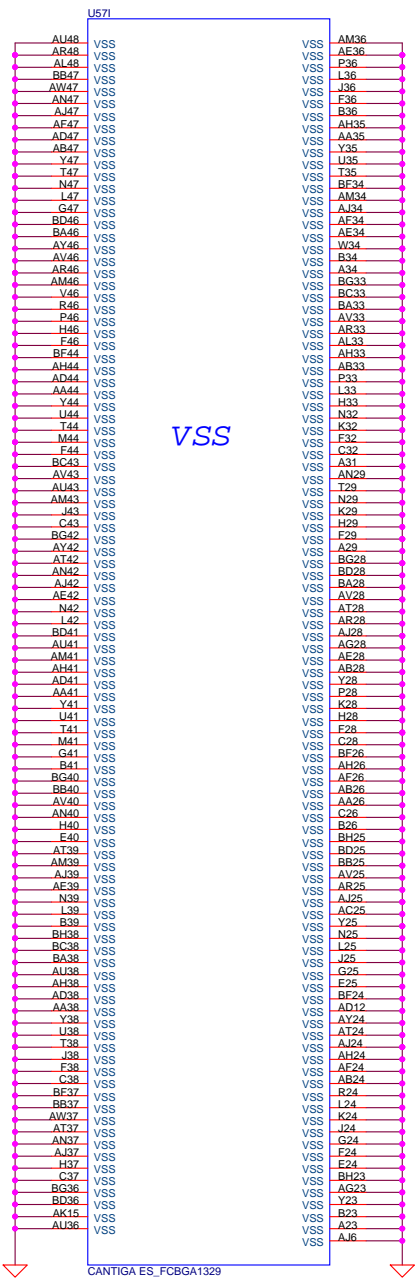
0522_Add C148.



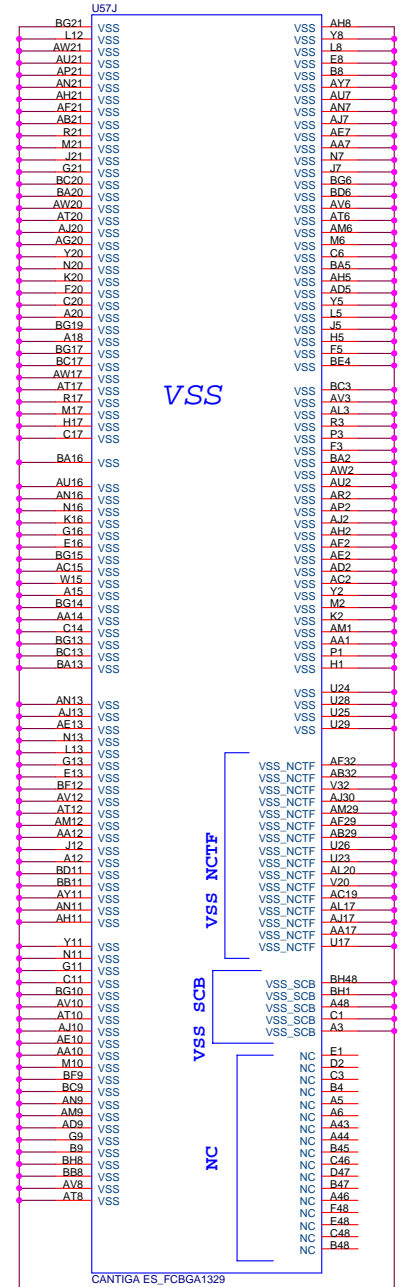
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Customer	Montevina Consumer Discrete	Document Number		Rev	0.3
Date	Friday, May 23, 2008	Sheet	10	of	44



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Date:	Friday, May 23, 2008	Sheet	11	of	44



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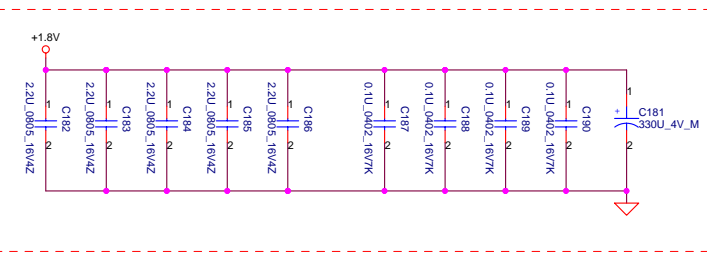


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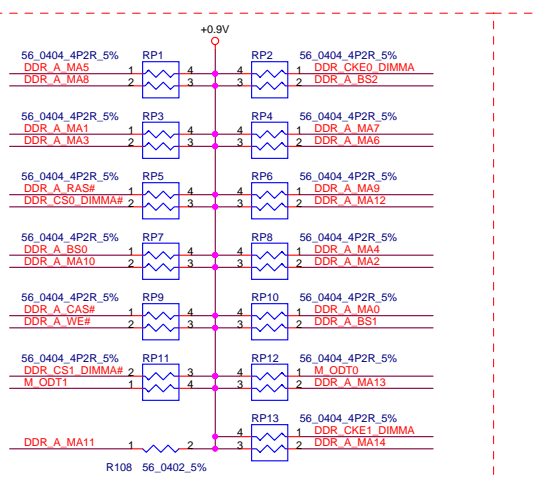
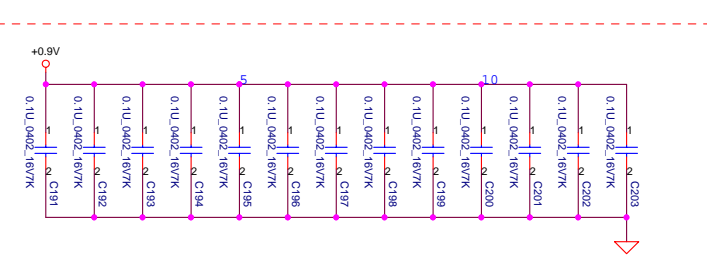
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				Montevina Consumer Discrete	0.3
				Date: Friday, May 23, 2008	Sheet 12 of 44



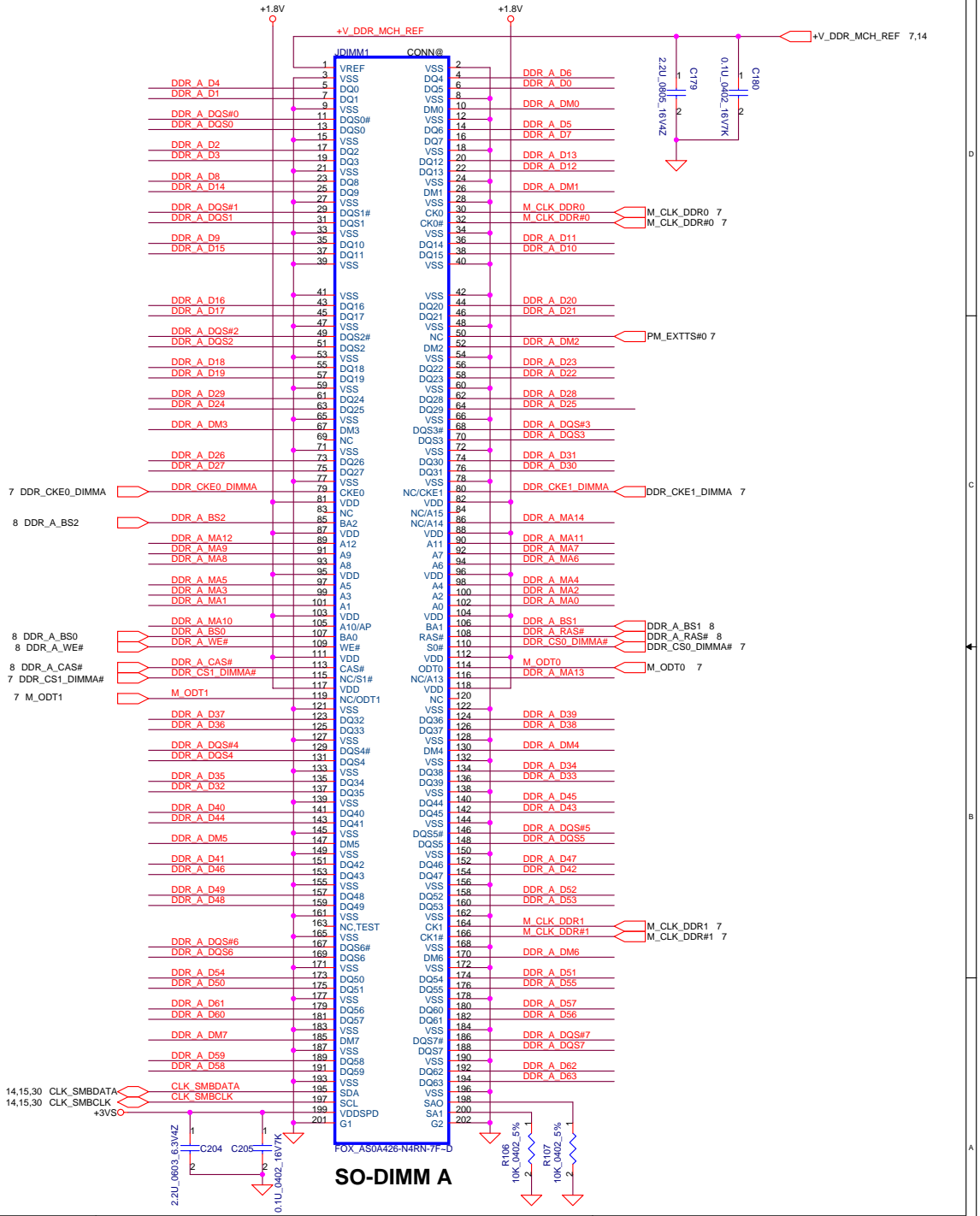
Layout Note:
Place near JDIMM1



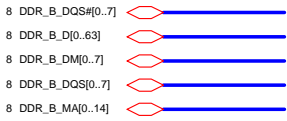
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



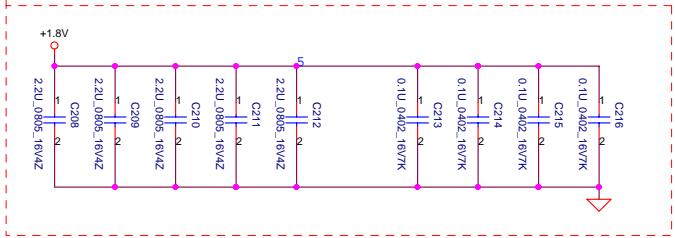
Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"



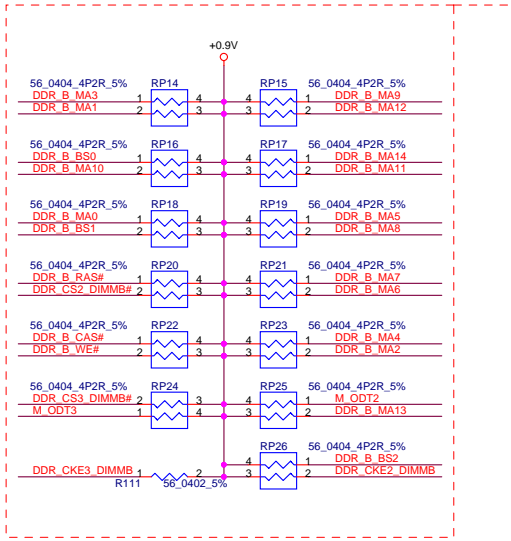
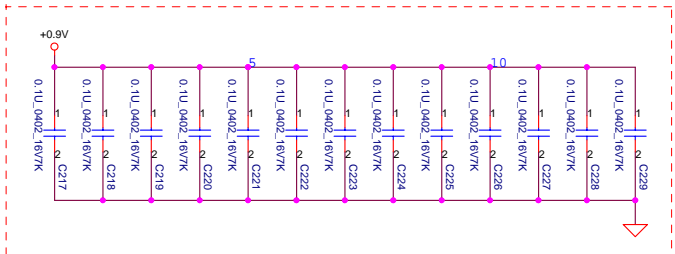
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Date:	Friday, May 23, 2008	Sheet	13 of 44



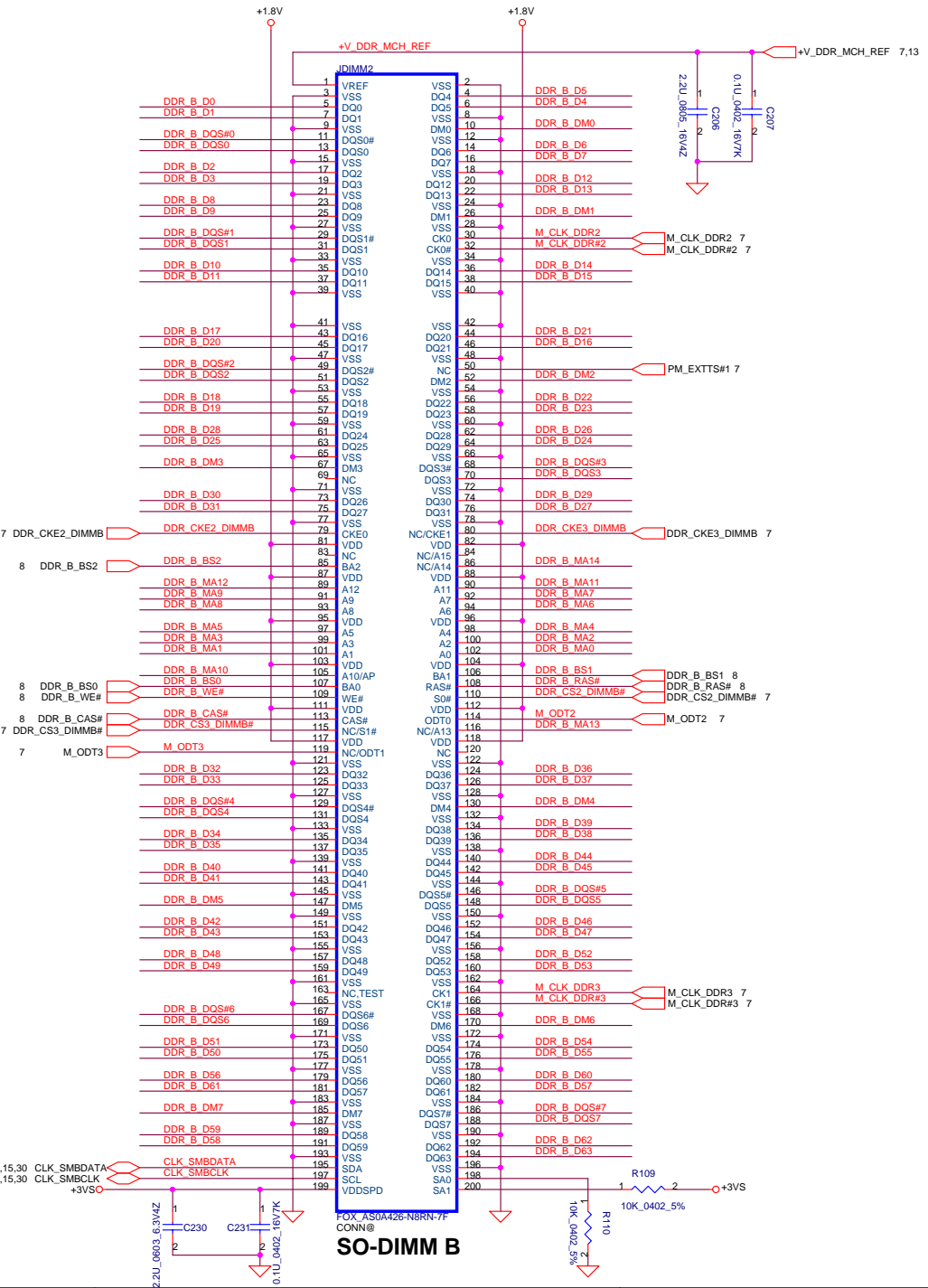
Layout Note:
Place near
JDIMM2



Layout Note:
Place one cap close to every 2
pullup
resistors terminated to +0.9VS



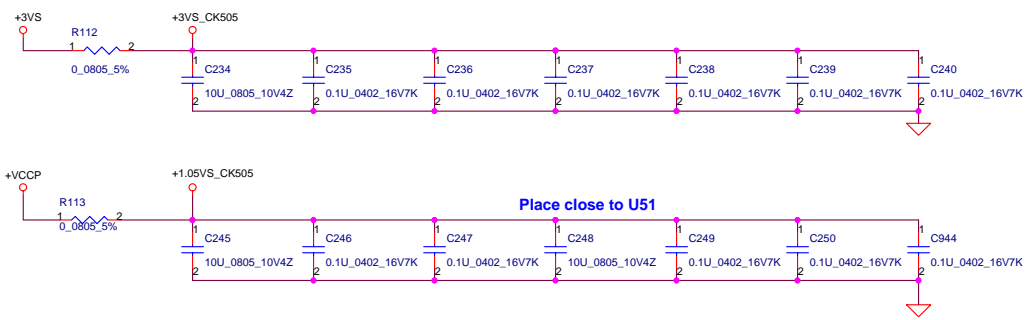
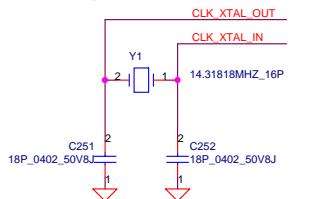
Layout Note:
Place these resistor
closely JP3, all
trace length Max=1.5"



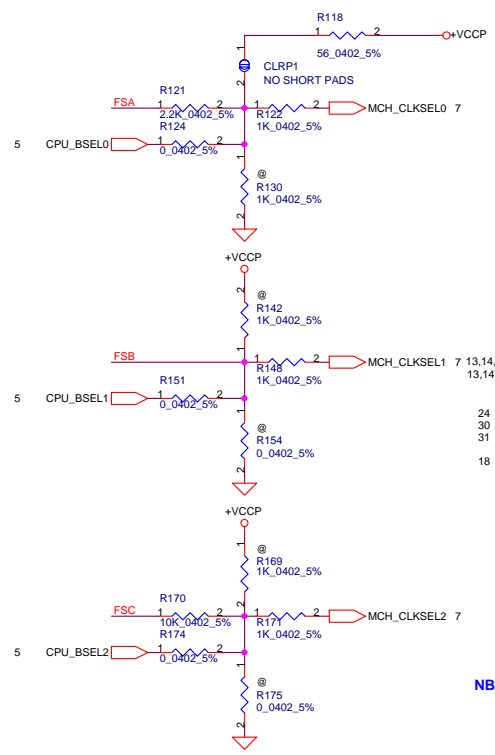
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Issued Date	2006/02/13	Deciphered Date	2006/03/10
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			Rev 0.3 Sheet 14 of 44

FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB	
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz	
0	0	0	266	100	33.3	14.318	96.0	48.0	
0	0	1	133	100	33.3	14.318	96.0	48.0	
0	1	0	200	100	33.3	14.318	96.0	48.0	
0	1	1	166	100	33.3	14.318	96.0	48.0	
1	0	0	333	100	33.3	14.318	96.0	48.0	
1	0	1	100	100	33.3	14.318	96.0	48.0	
1	1	0	400	100	33.3	14.318	96.0	48.0	
1	1	1	Reserved						

Routing the trace at least 10mil

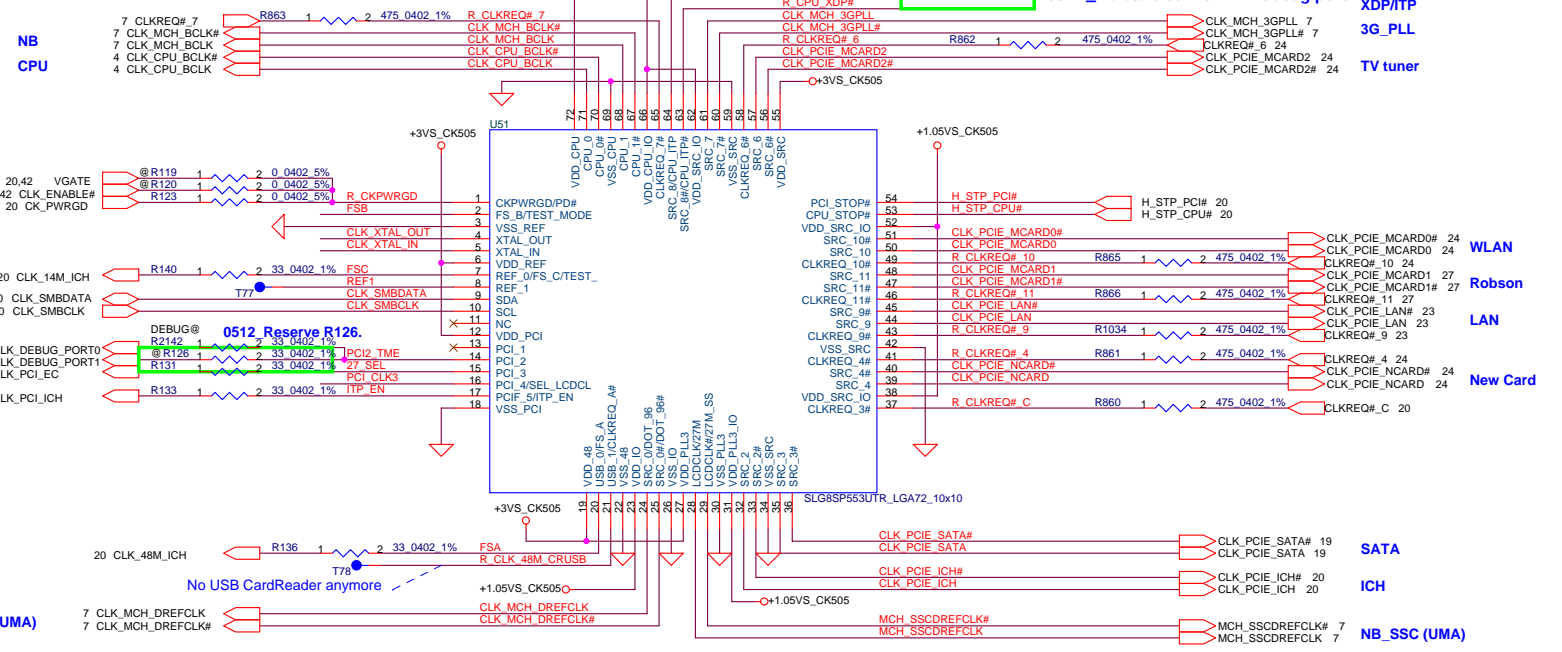


Place close to U51



NB CPU

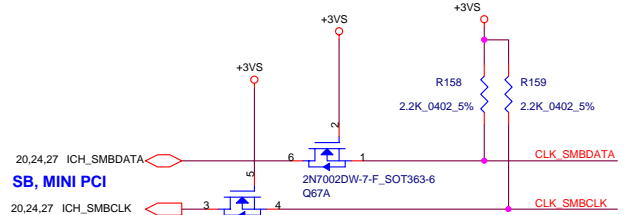
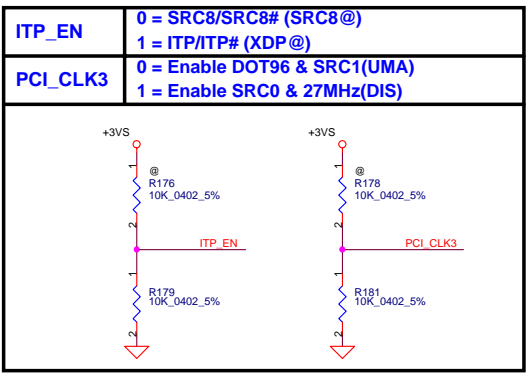
NB (UMA)



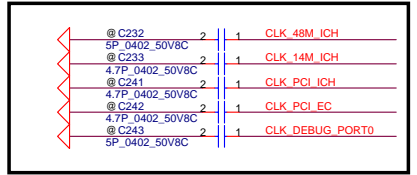
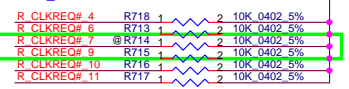
No USB CardReader anymore

0512 Reserve R126.

0512_Delete clock for XDP debug port.

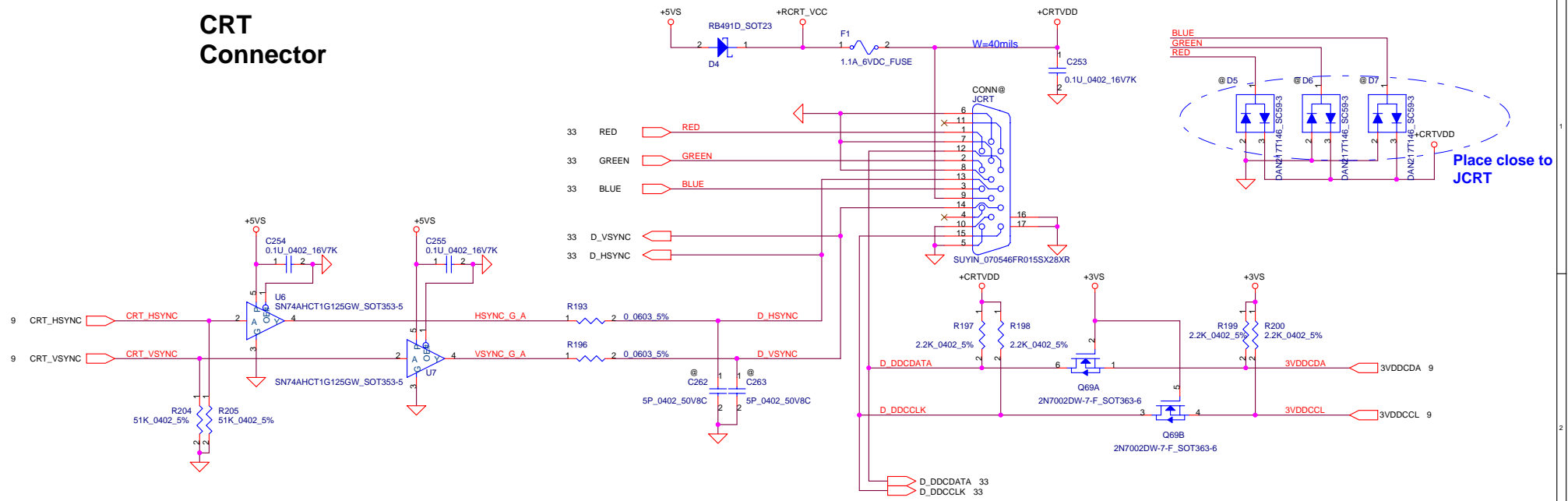


0507 Reserve R714.



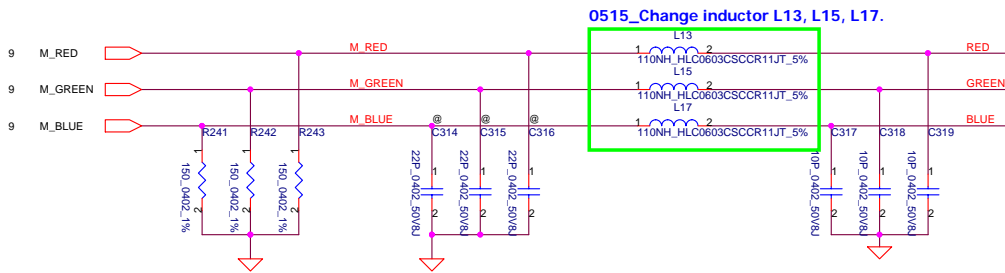
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Issued Date	2006/02/13	Deciphered Date	2006/03/10
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<p style="text-align: right;">Compal Electronics, Inc. Clock Generator CK505</p>			<p>Document Number Montevina Consumer Discrete</p>
Date:	Friday, May 23, 2008	Sheet	15 of 44

CRT Connector

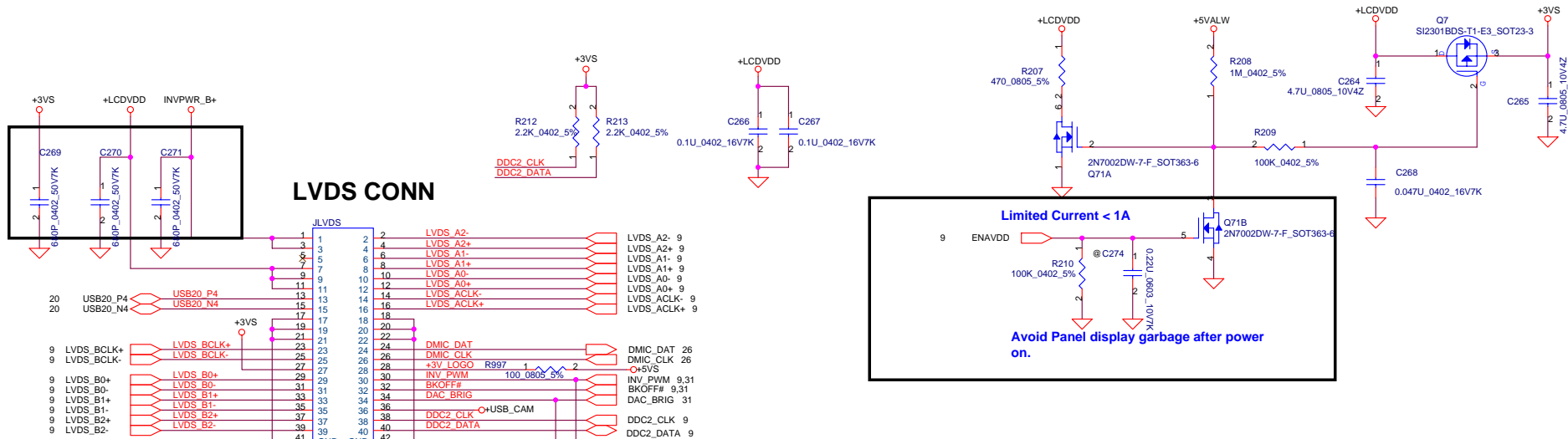


CRT Termination/EMI Filter

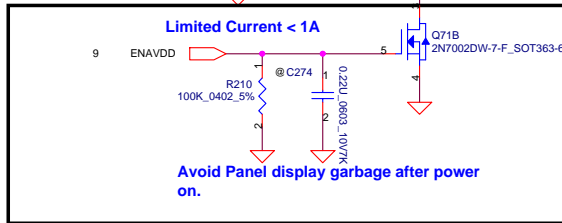
Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.



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				Montevina Consumer Discrete	0.3
Date: Friday, May 23, 2008				Sheet	16 of 44



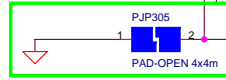
LVDS CONN



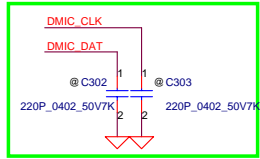
Limited Current < 1A

Avoid Panel display garbage after power on.

0521_Add PJP305 to sparate GND.

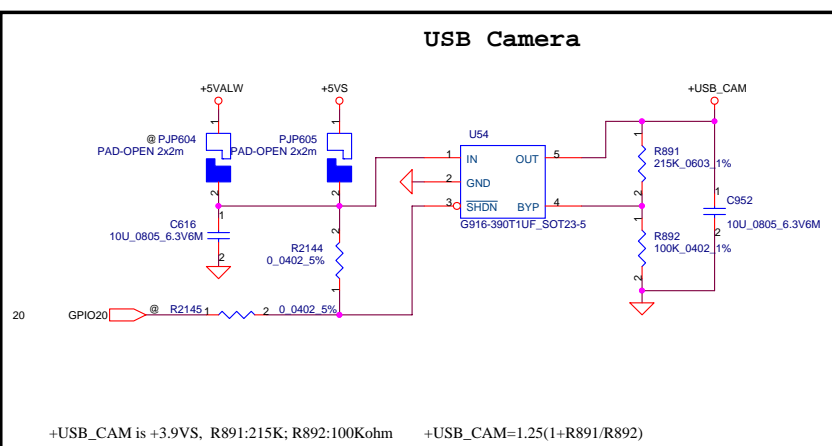
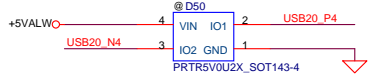
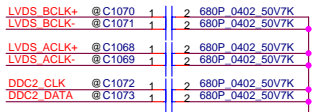
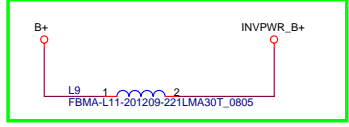


Must close JLVDSpin 24, 26



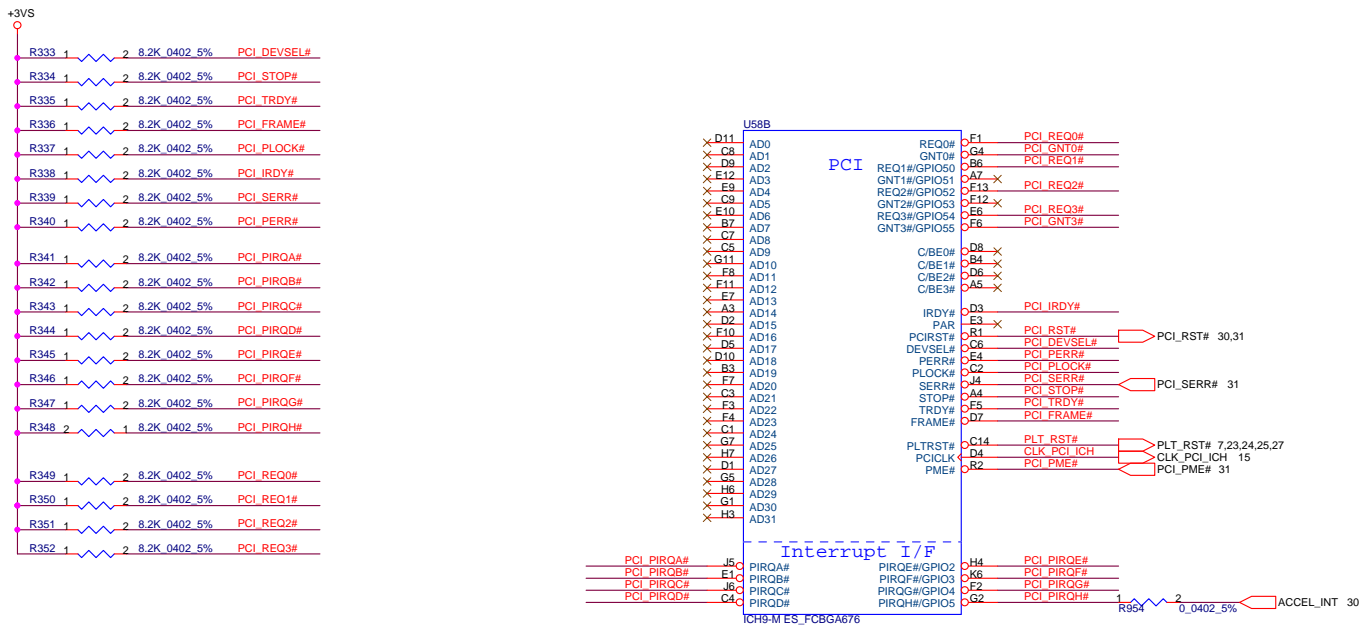
0509_reserve C302 and C303.

0521_Delete L8.



+USB_CAM is +3.9VS, R891:215K; R892:100Kohm +USB_CAM=1.25(1+R891/R892)

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				Montevina Consumer UMA	0.3
Date: Friday, May 23, 2008				Sheet	17 of 44



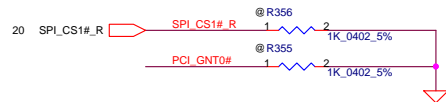
A16 swap override Strap

PCI_GNT3# Low= A16 swap override Enable
High= Default *

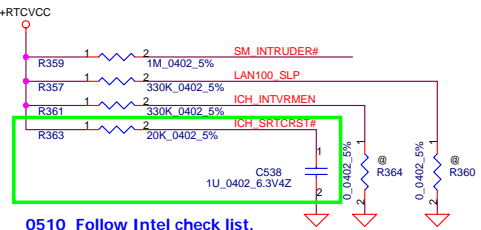


Boot BIOS Strap

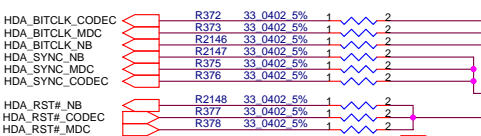
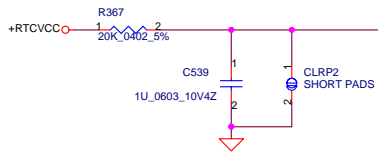
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



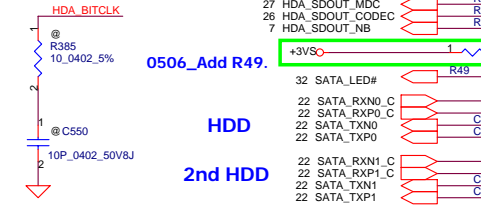
ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



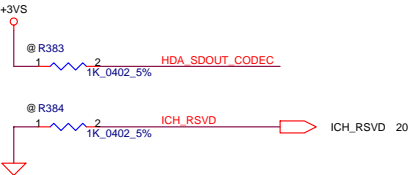
0510_Follow Intel check list.



0506_Add R49.

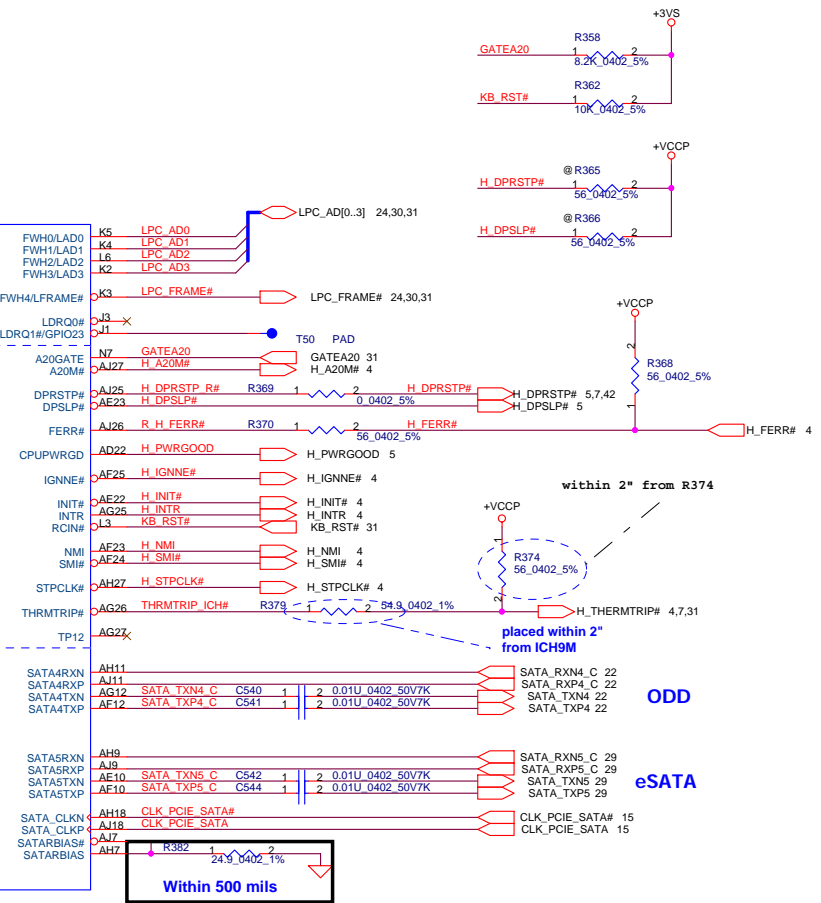
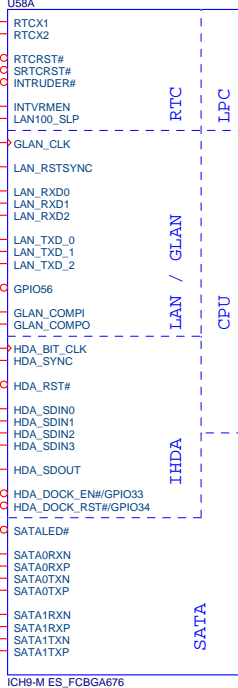
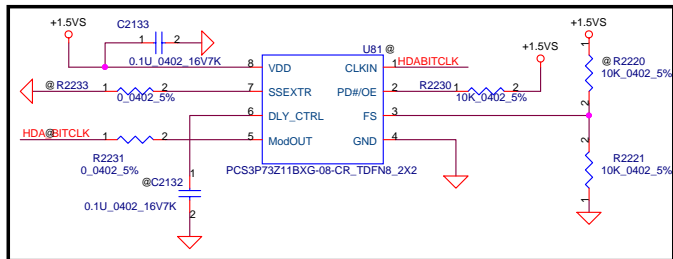
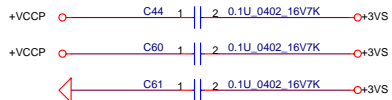


XOR CHAIN ENTRANCE STRAP:RSVD



ICH_RSVD	HDA_SDOUT_CODEC
0	0
0	1
1	0
1	1

For HDA_BITCLK_NB crossmoat issue



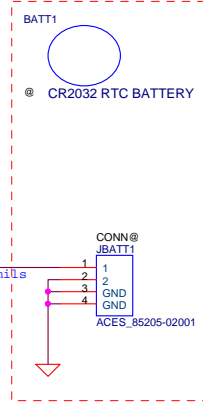
Within 500 mils

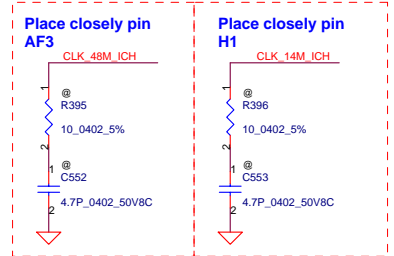
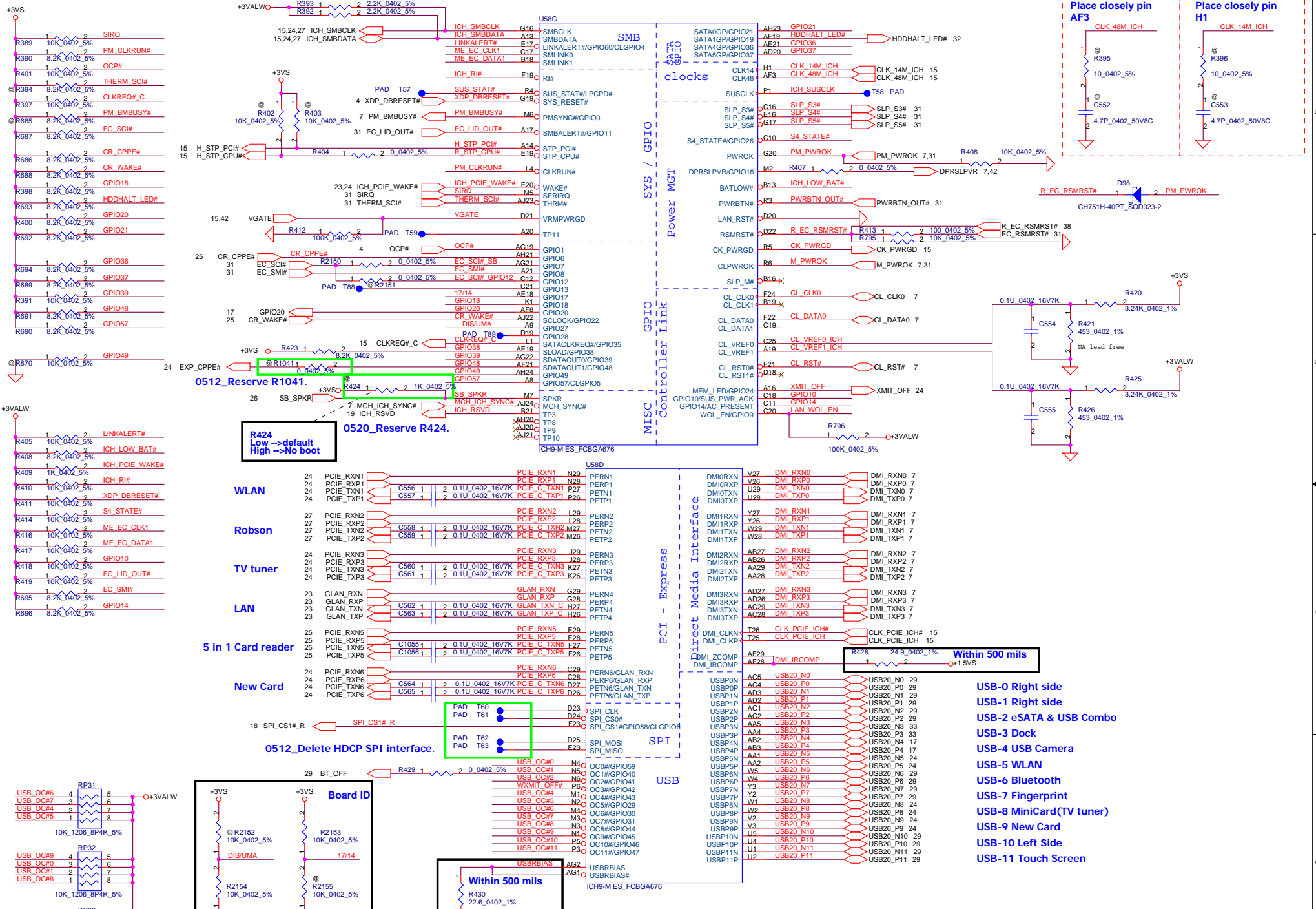
within 2" from R374

placed within 2" from ICH9M

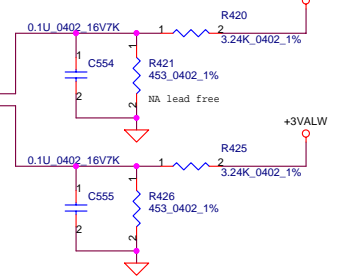
ODD

eSATA



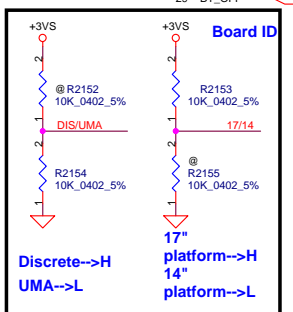


R_EC_RSMRST# 1 D86 2 PM_PWROK CH751H-40PT_S0D323-2

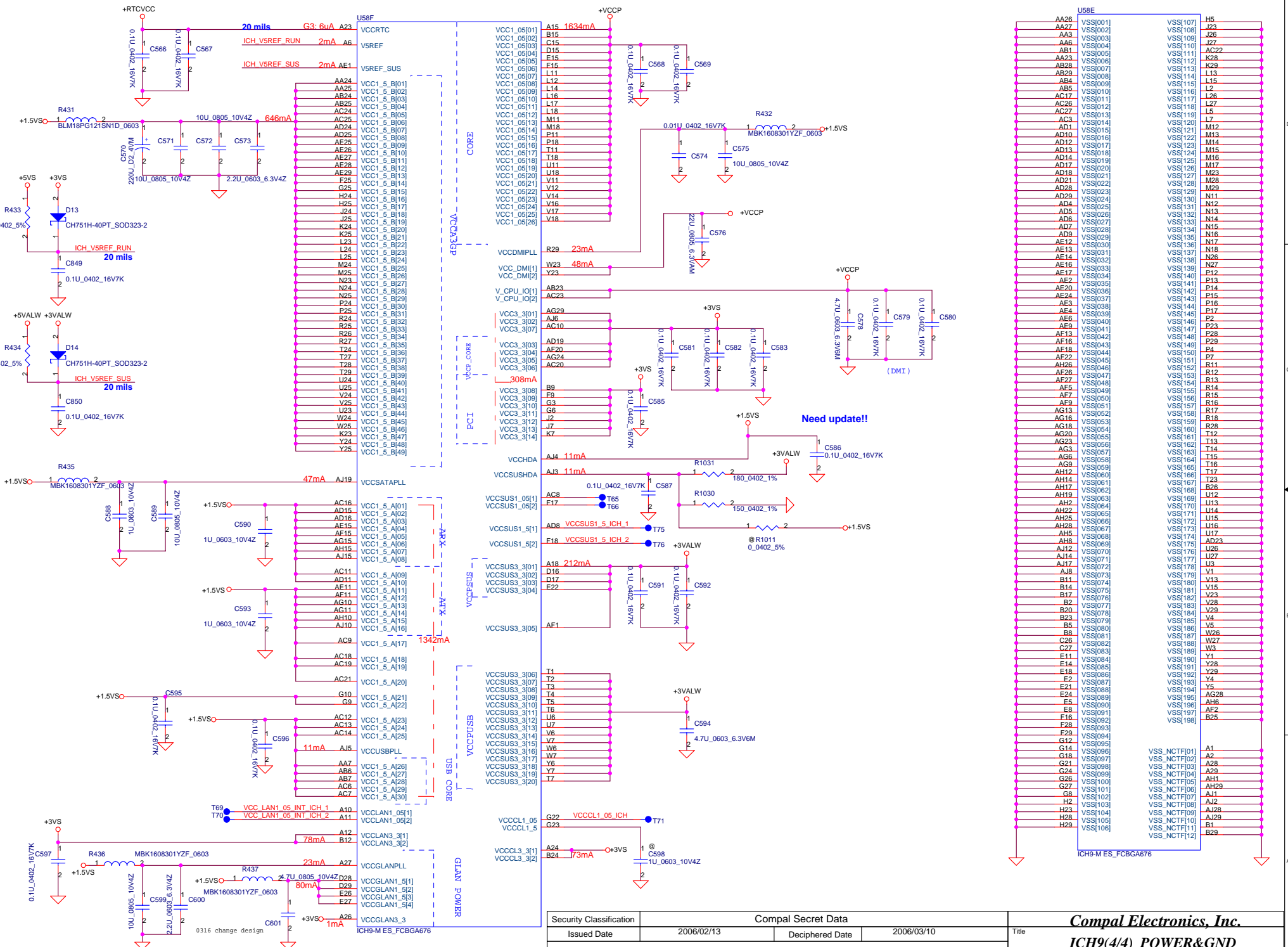


R424 Low -> default High -> No boot

R428 24.9 0.402 1% Within 500 mils

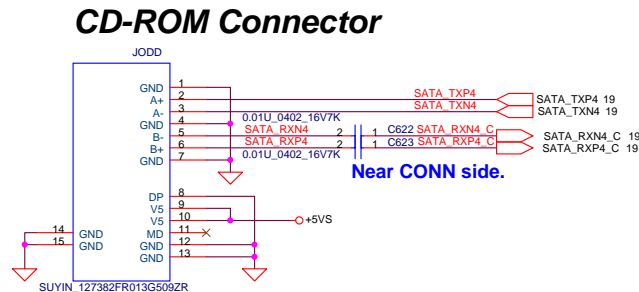
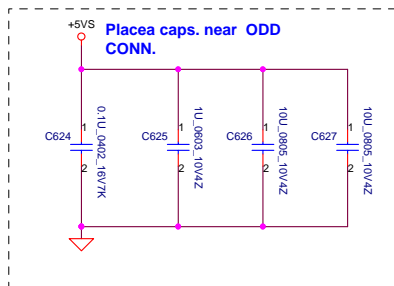
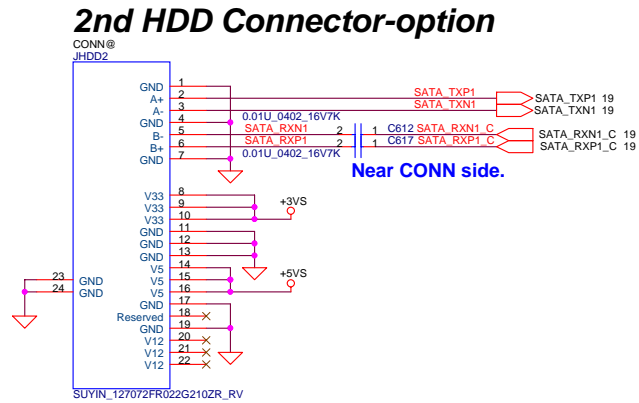
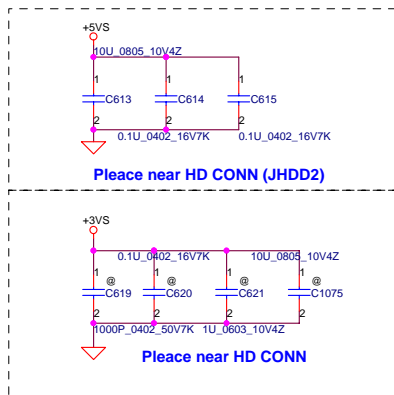
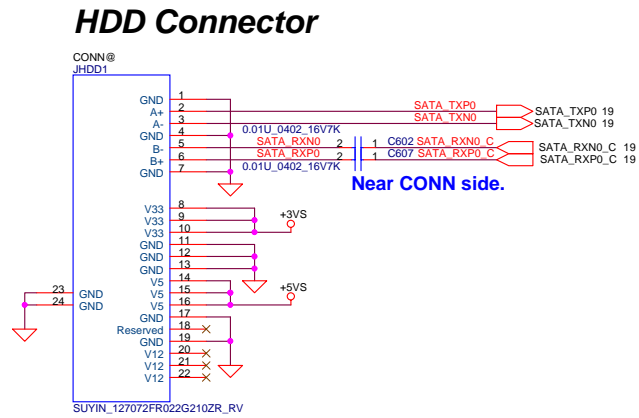
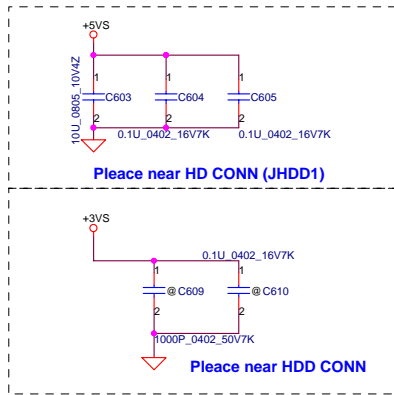


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Document Number	Customer	Rev	0.3	<p>ICH9(3/4) DMI,USB,GPIO,PCIE</p> <p>Montevina Consumer Discrete</p>	
Date:	Friday, May 23, 2008	Sheet	20	of 44	



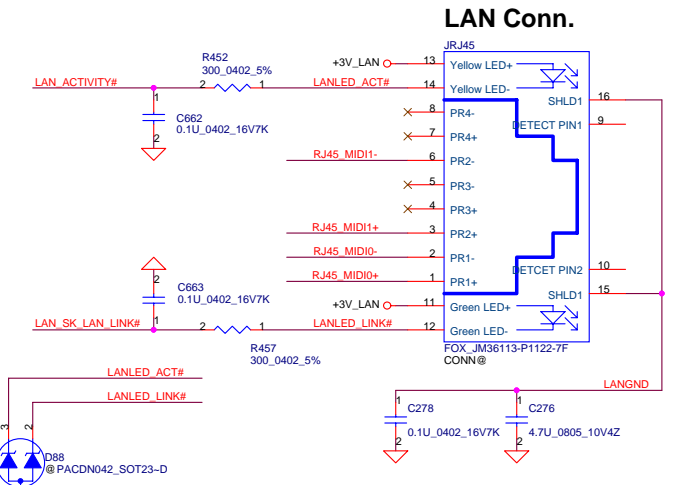
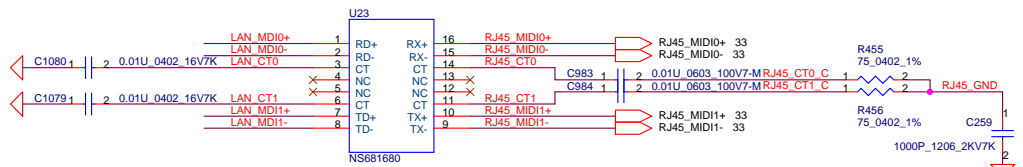
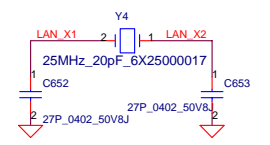
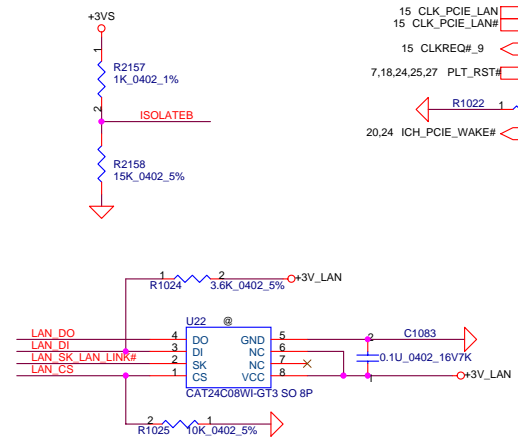
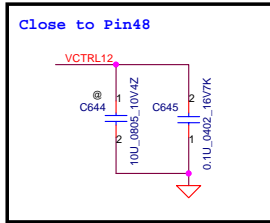
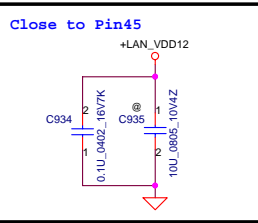
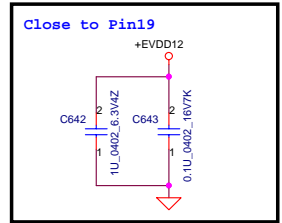
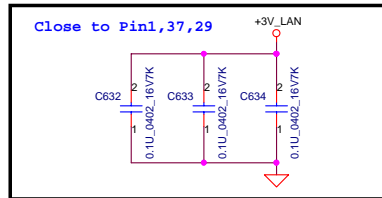
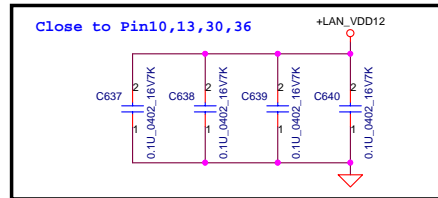
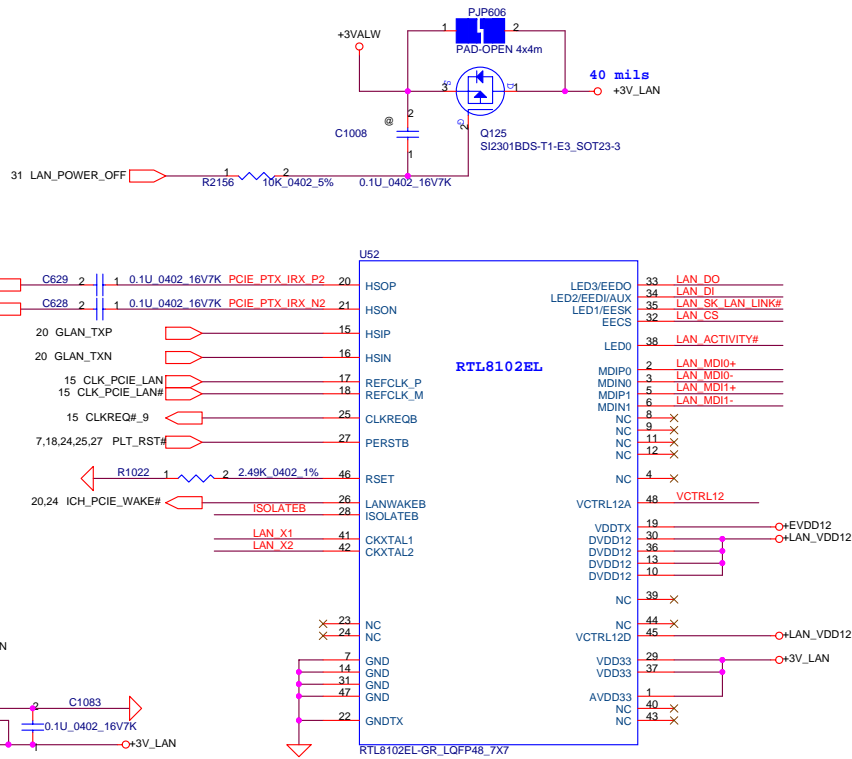
U8E		H5	
AA26	VSS1001	VSS107	H5
AA27	VSS1002	VSS108	J23
AA3	VSS1003	VSS109	J26
AA6	VSS1004	VSS110	J27
AA23	VSS1005	VSS111	AC22
AB1	VSS1006	VSS112	K28
AB28	VSS1007	VSS113	K29
AB29	VSS1008	VSS114	L13
AB5	VSS1009	VSS115	L15
AB6	VSS1010	VSS116	L2
AC17	VSS1011	VSS117	L26
AC26	VSS1012	VSS118	L27
AC27	VSS1013	VSS119	L7
AC3	VSS1014	VSS120	M12
AD1	VSS1015	VSS121	M13
AD10	VSS1016	VSS122	M14
AD12	VSS1017	VSS123	M15
AD13	VSS1018	VSS124	M16
AD14	VSS1019	VSS125	M17
AD17	VSS1020	VSS126	M23
AD18	VSS1021	VSS127	M24
AD21	VSS1022	VSS128	M25
AD22	VSS1023	VSS129	M29
AD28	VSS1024	VSS130	N11
AD29	VSS1025	VSS131	N12
AD4	VSS1026	VSS132	N13
AD5	VSS1027	VSS133	N14
AD6	VSS1028	VSS134	N15
AD7	VSS1029	VSS135	N16
AD9	VSS1030	VSS136	N17
AE1	VSS1031	VSS137	N18
AE13	VSS1032	VSS138	N26
AE16	VSS1033	VSS139	N27
AE17	VSS1034	VSS140	P12
AE2	VSS1035	VSS141	P13
AE24	VSS1036	VSS142	P14
AE3	VSS1037	VSS143	P15
AE4	VSS1038	VSS144	P17
AE6	VSS1039	VSS145	P2
AE9	VSS1040	VSS146	P23
AE10	VSS1041	VSS147	P28
AE16	VSS1042	VSS148	P29
AE18	VSS1043	VSS149	P4
AE20	VSS1044	VSS150	P5
AE22	VSS1045	VSS151	P7
AE23	VSS1046	VSS152	R11
AE26	VSS1047	VSS153	R12
AE27	VSS1048	VSS154	R13
AE28	VSS1049	VSS155	R14
AE7	VSS1050	VSS156	R15
AG3	VSS1051	VSS157	R16
AG13	VSS1052	VSS158	R17
AG16	VSS1053	VSS159	R18
AG18	VSS1054	VSS160	R28
AG20	VSS1055	VSS161	T12
AG23	VSS1056	VSS162	T13
AG3	VSS1057	VSS163	T14
AG6	VSS1058	VSS164	T15
AG10	VSS1059	VSS165	T16
AH12	VSS1060	VSS166	T17
AH14	VSS1061	VSS167	T23
AH17	VSS1062	VSS168	B26
AH19	VSS1063	VSS169	U13
AH22	VSS1064	VSS170	U14
AH23	VSS1065	VSS171	U15
AH25	VSS1066	VSS172	U16
AH28	VSS1067	VSS173	U17
AH5	VSS1068	VSS174	AD23
AH8	VSS1069	VSS175	U26
AJ12	VSS1070	VSS176	U27
AJ14	VSS1071	VSS177	U2
AJ17	VSS1072	VSS178	V1
AJ8	VSS1073	VSS179	V13
B11	VSS1074	VSS180	V15
B14	VSS1075	VSS181	V23
B17	VSS1076	VSS182	V28
B2	VSS1077	VSS183	V29
B20	VSS1078	VSS184	V4
B23	VSS1079	VSS185	V5
B5	VSS1080	VSS186	W26
B8	VSS1081	VSS187	W27
C26	VSS1082	VSS188	W3
C27	VSS1083	VSS189	Y1
E11	VSS1084	VSS190	Y2
E18	VSS1085	VSS191	Y28
E19	VSS1086	VSS192	Y29
E2	VSS1087	VSS193	Y4
E21	VSS1088	VSS194	Y5
E24	VSS1089	VSS195	AG28
E5	VSS1090	VSS196	AH6
E8	VSS1091	VSS197	AF2
F18	VSS1092	VSS198	B25
F28	VSS1093	VSS199	A1
F29	VSS1094	VSS200	A2
G12	VSS1095	VSS201	A28
G14	VSS1096	VSS202	A29
G18	VSS1097	VSS203	AH1
G21	VSS1098	VSS204	AH29
G24	VSS1099	VSS205	AJ1
G26	VSS1100	VSS206	AJ2
G27	VSS1101	VSS207	AJ28
G8	VSS1102	VSS208	B1
H2	VSS1103	VSS209	B29
H23	VSS1104	VSS210	
H28	VSS1105	VSS211	
H29	VSS1106	VSS212	

Security Classification	Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Compal Electronics, Inc.
ICH9(4/4) POWER&GND				
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Date:	Friday, May 23, 2008	Document Number:	Montevina Consumer Discrete	Rev 0.3
		Sheet	21	of 44



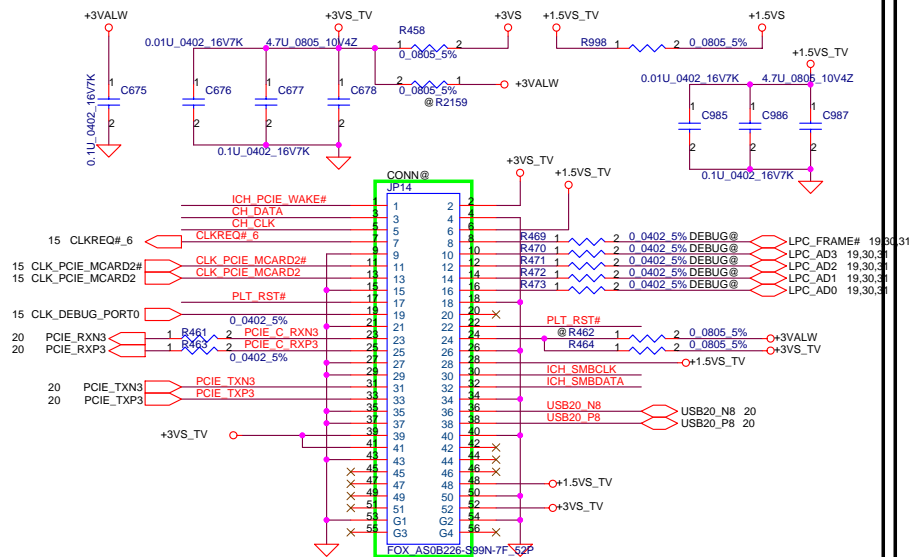
PCB 03W LA-4081P REV0 MB UMA

Security Classification	Compal Secret Data			Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	HDD & CDROM	
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				Montevina Consumer Discrete	0.3
Date: Friday, May 23, 2008				Sheet	22 of 44



Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2006/10/26	Deciphered Date	2007/06/30	88E8042 10/100 LAN	
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Date:	Friday, May 23, 2008	Sheet	23	of	44

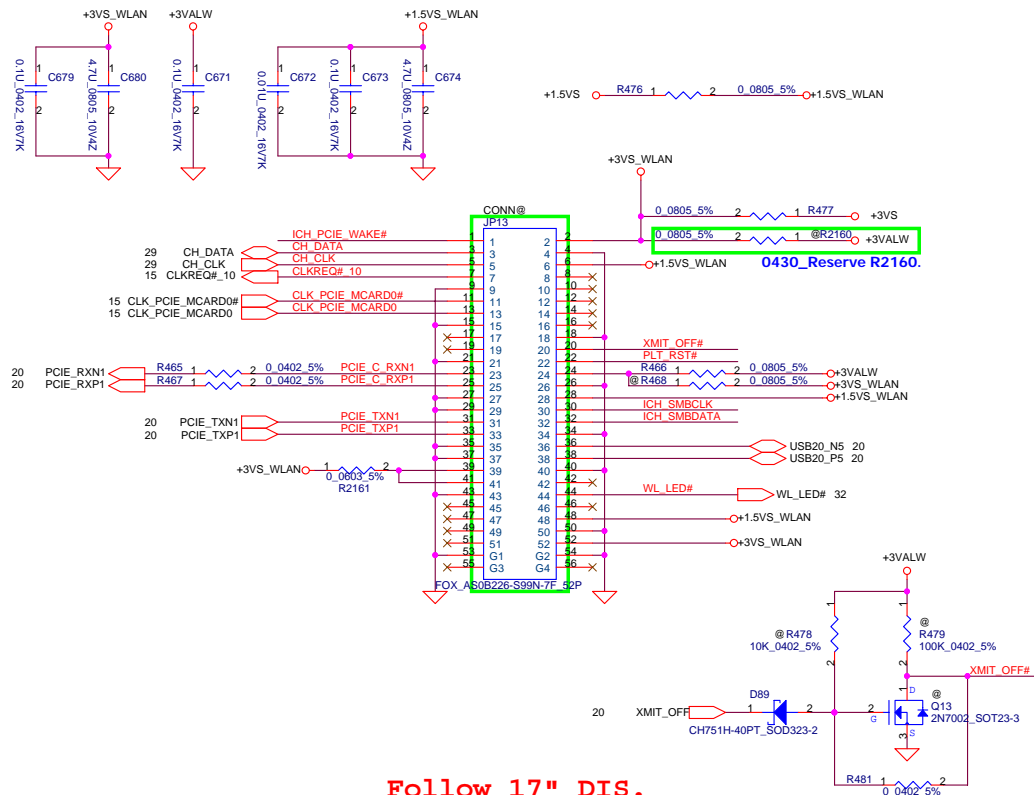
Mini Card 0--TV tuner



Follow 17" DIS.

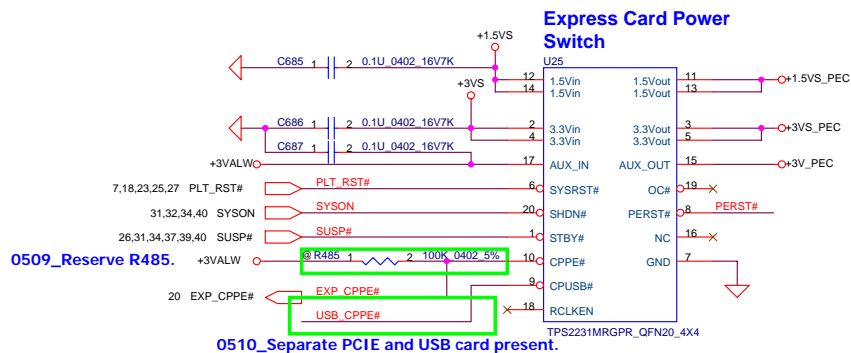
Power Rail	Voltage Tolerance	Primary		Auxiliary
		Peak (Max) mA	Normal (Max) mA	Normal (Max) mA
+3.3V	+/- 9%	1000	750	N/A
3.3Vaux	+/- 9%	330	250	250 (Wake Enable) 5 (Wake Disable)
+1.5V	+/- 5%	500	375	N/A

Mini Card 2---WLAN



Follow 17" DIS.

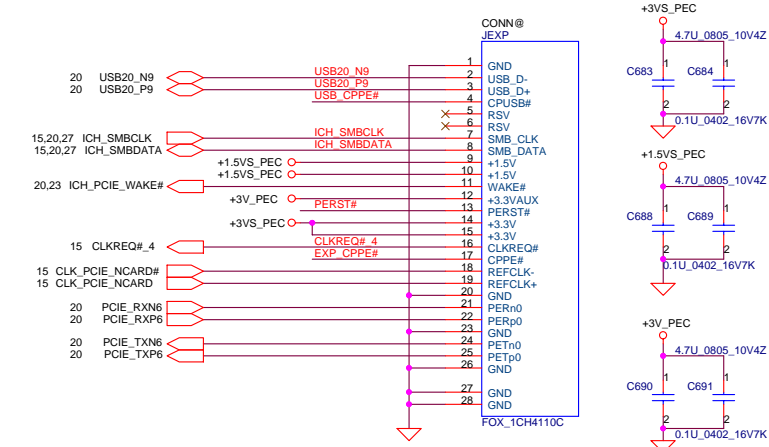
New Card

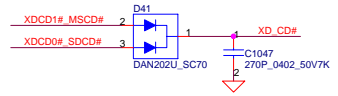
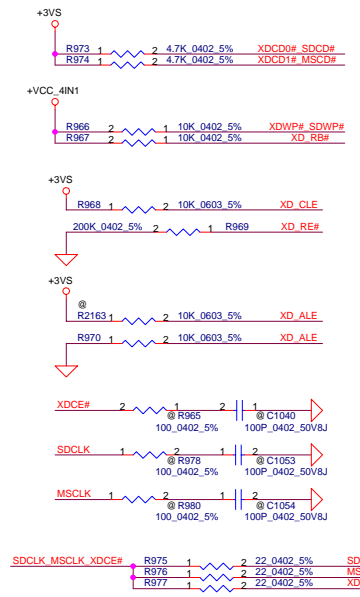


internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

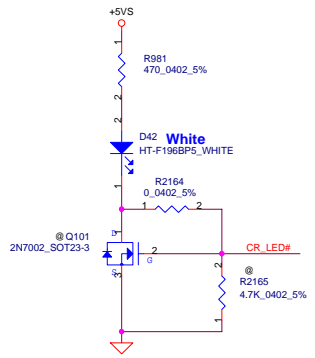
Follow 17" DIS.

Near to Express Card slot.

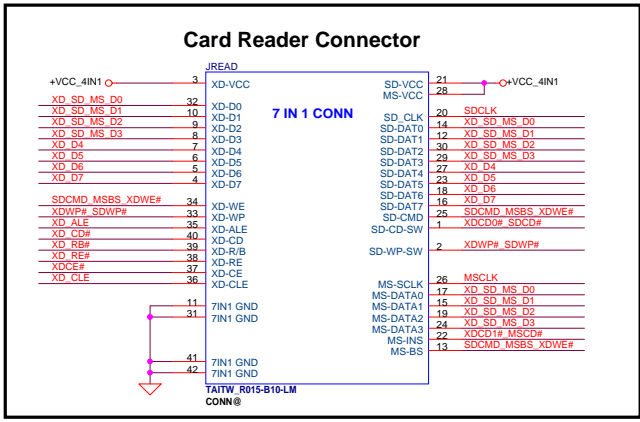
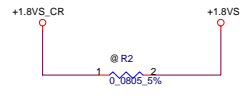
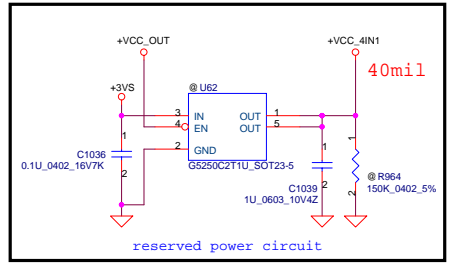
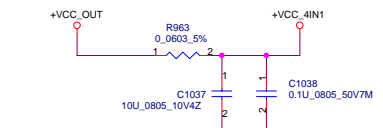
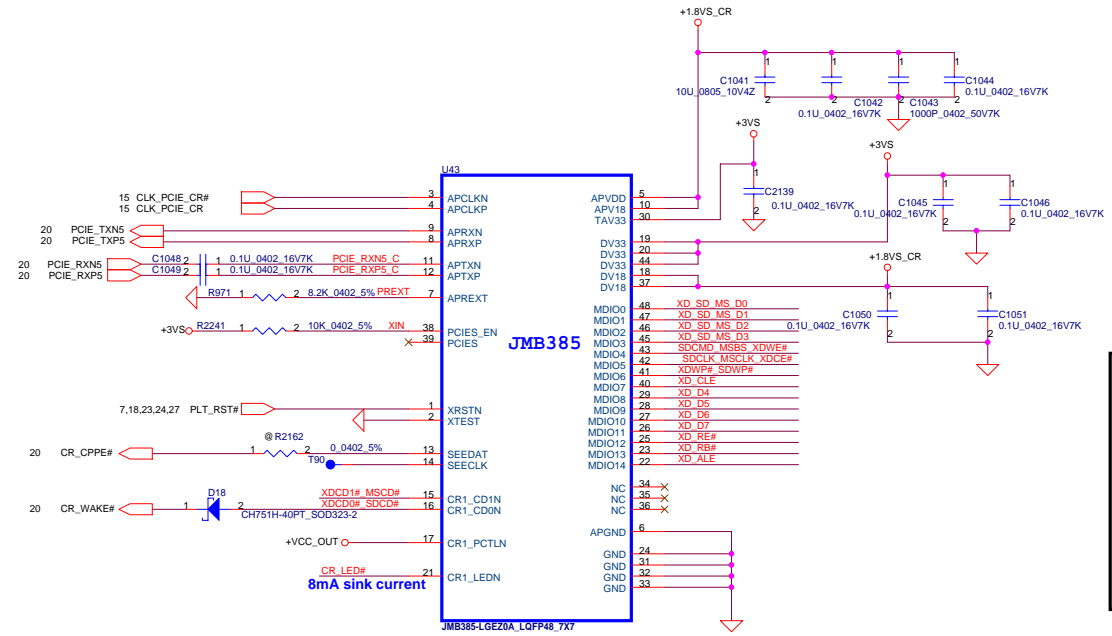




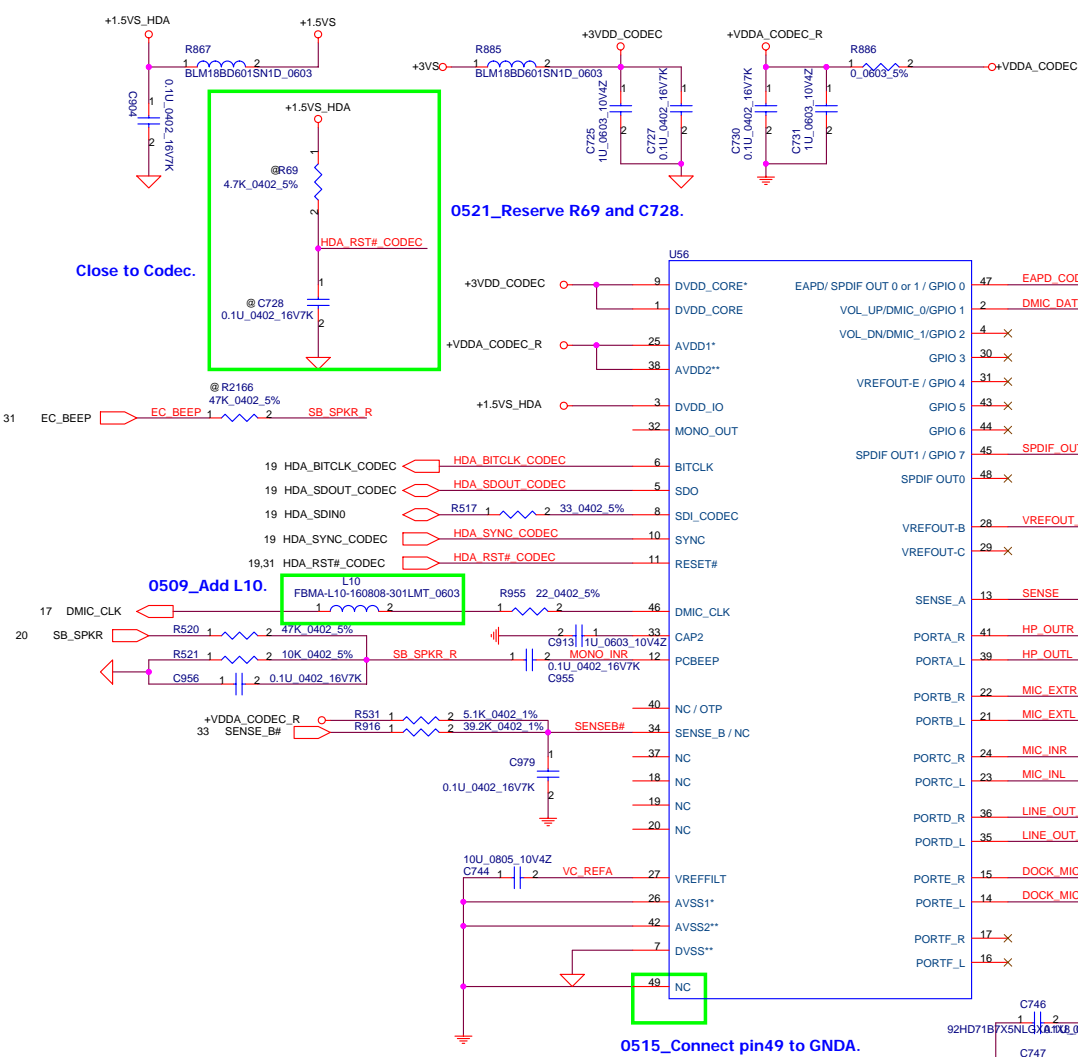
White LED: VF=3V, IF = 5mA, Res = 56ohm



01/03 Change Cardreader LED control
02/13 Direct driver LED



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Issued Date	2007/08/28	Deciphered Date	2006/10/06	2007/08/28
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Size	Custom	Rev	0.3	

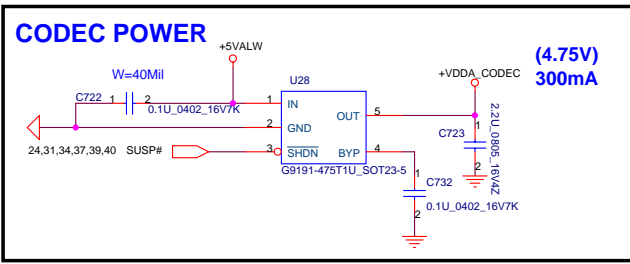


Close to Codec.

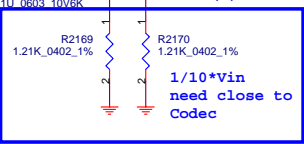
0521_Reserve R69 and C728.

0509_Add L10.

0515_Connect pin49 to GNDa.



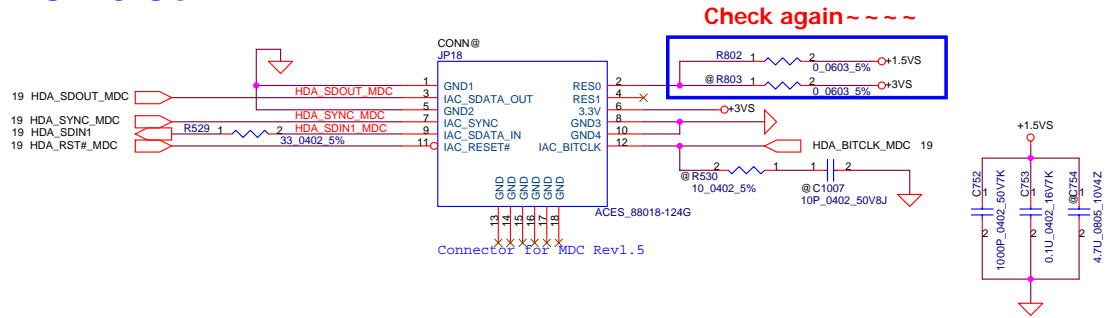
0519_Change right part number for 39.2K ohm.



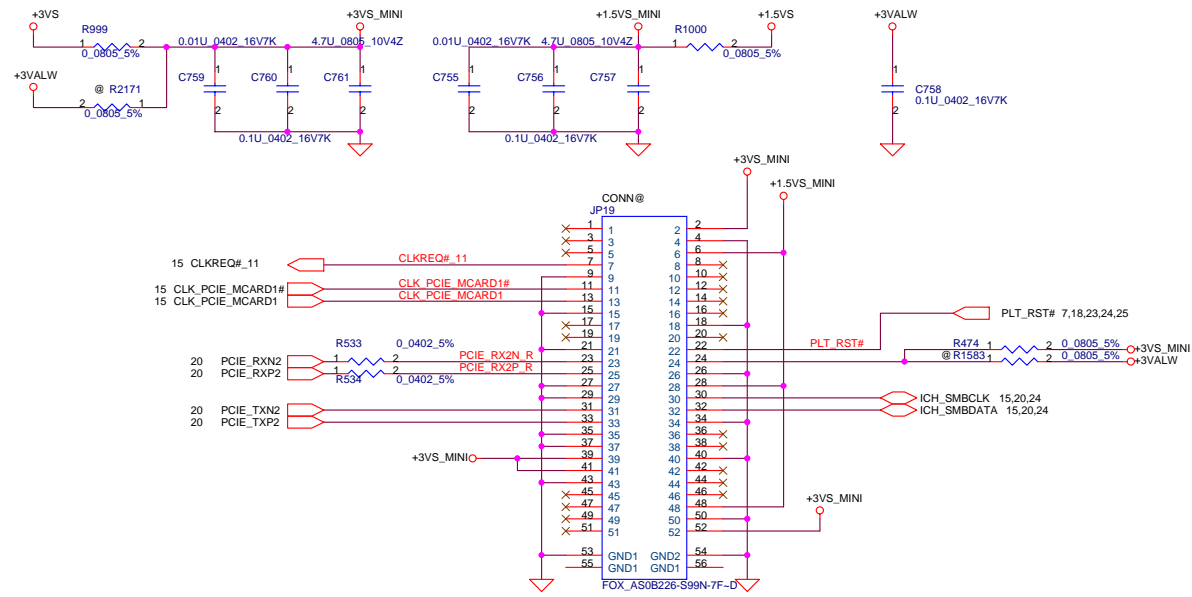
SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

Security Classification	Compal Secret Data		Title
Issued Date	2006/10/26	Deciphered Date	2006/07/26
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Date:	Monday, May 26, 2008	Sheet	26 of 44

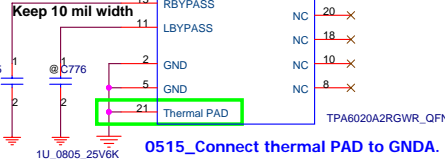
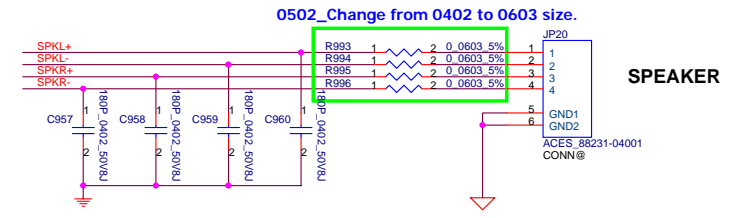
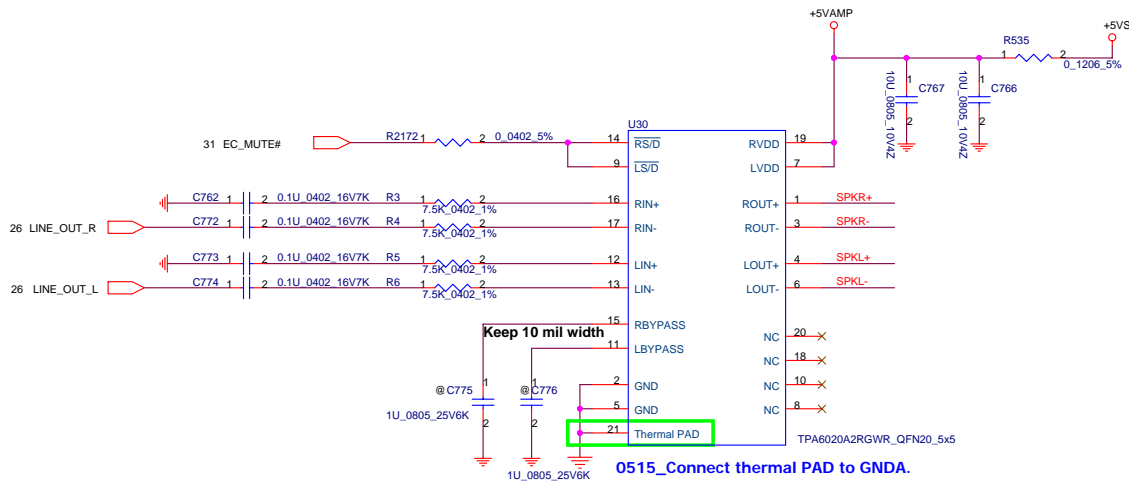
MDC 1.5 Conn.



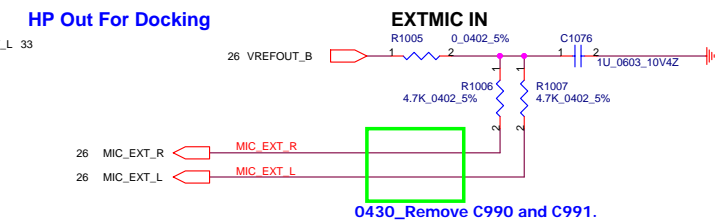
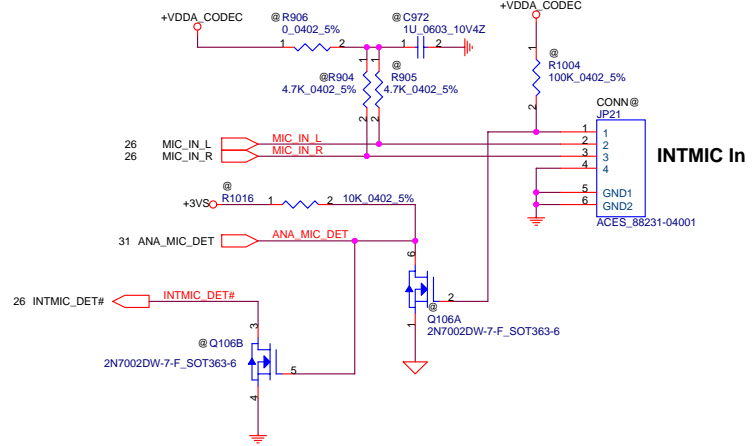
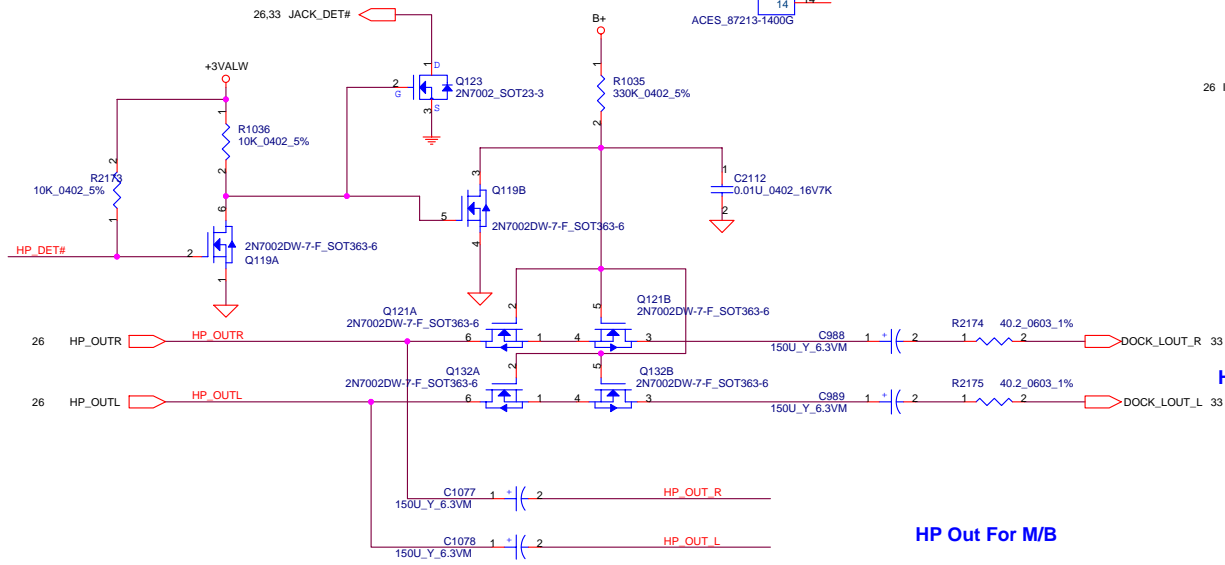
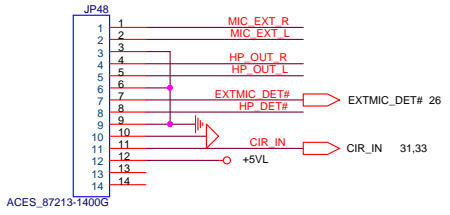
Mini Card 1---Robson



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Issued Date	2006/10/26	Deciphered Date	2006/07/26	MDC 1.5 & Robson	
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				Montevina Consumer Discrete	0.3
Date: Friday, May 23, 2008				Sheet	27 of 44

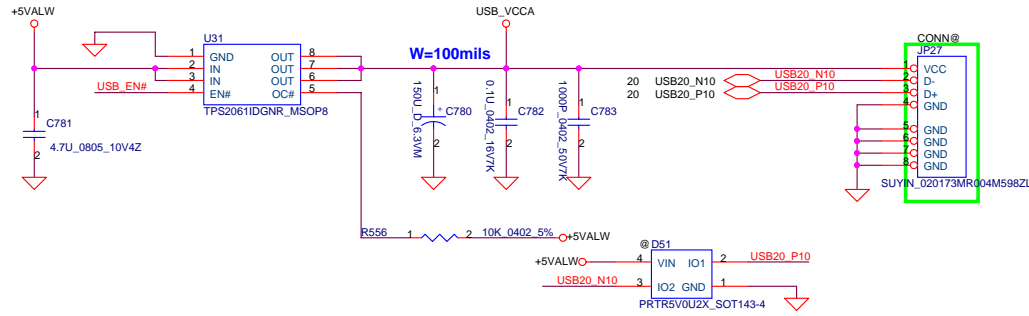


Audio & USB board conn

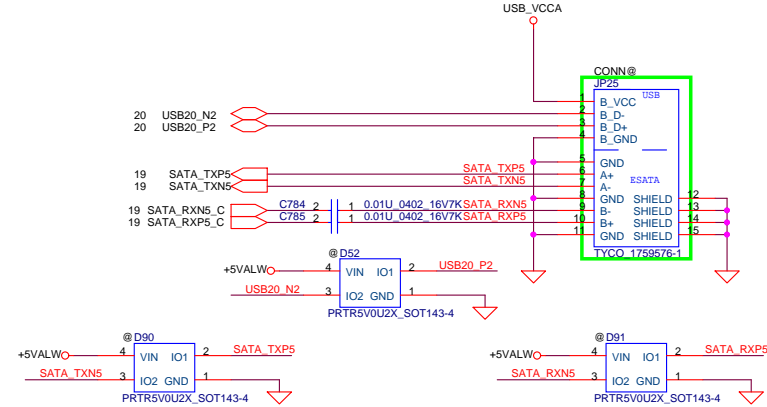


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Issued Date	2006/10/26	Deciphered Date	2006/07/26	AMP & Audio Jack	
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Document Number	Montevina Consumer Discrete			Rev	0.3
Date:	Monday, May 26, 2008	Sheet	28	of	44

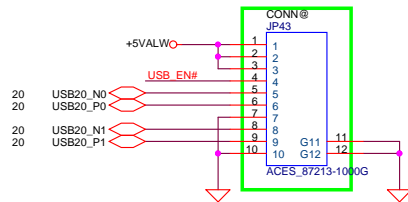
Left side USB CONNECTOR



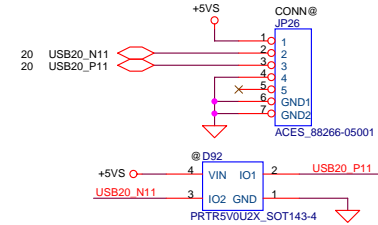
Left side eSATA/USB combination Connector



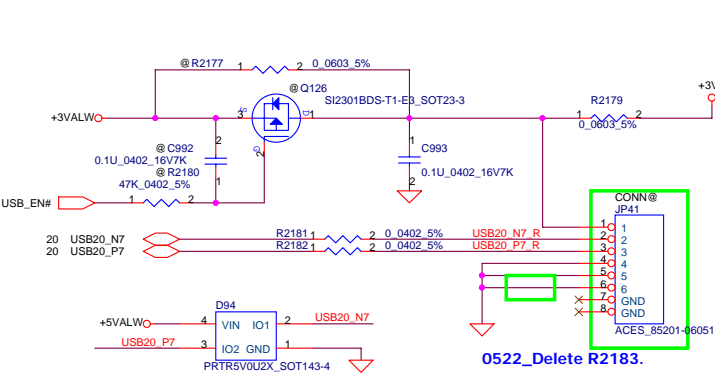
USB cable connector for Right side



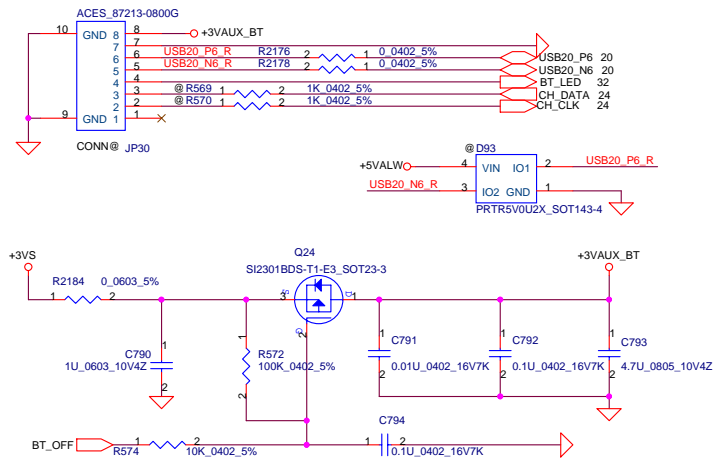
Touch screen connector



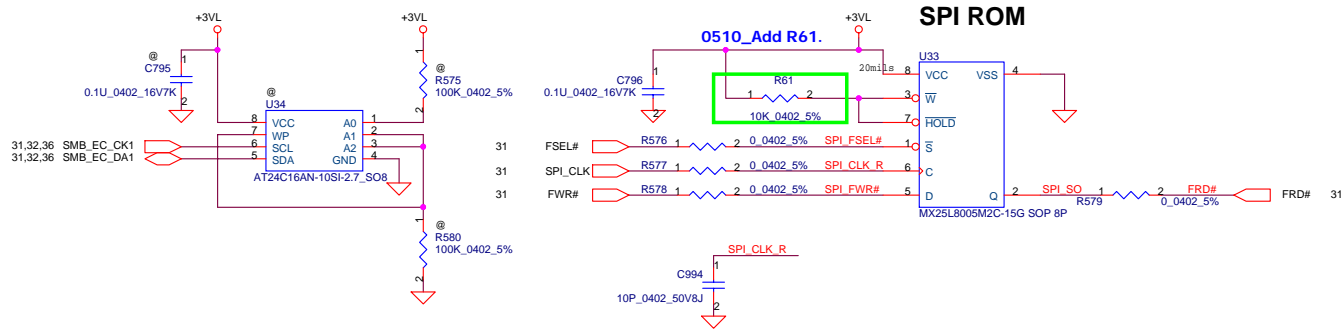
Finger printer



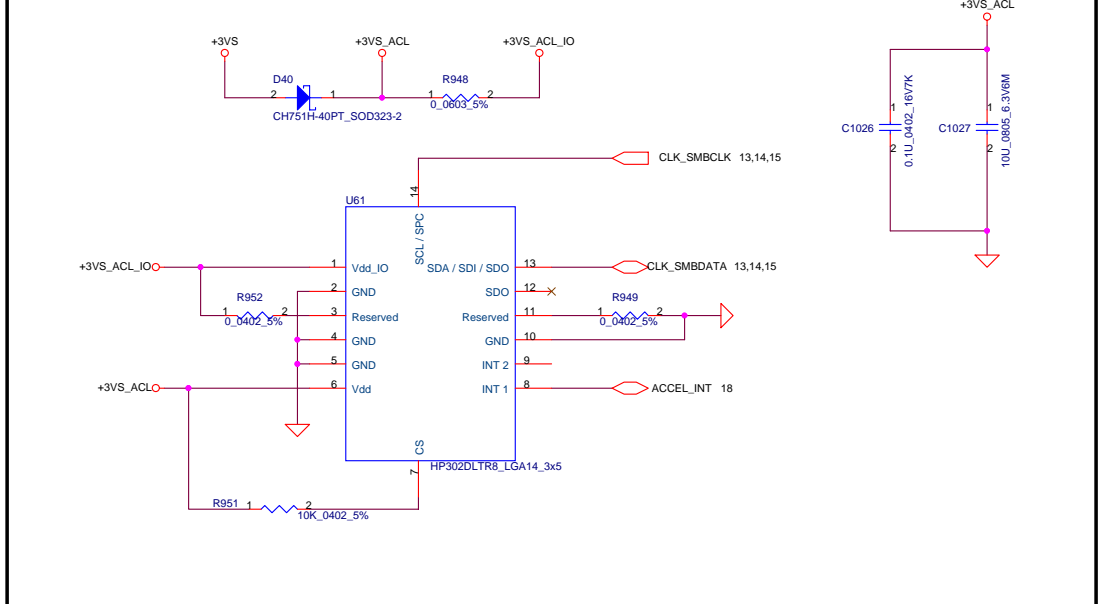
BT Connector



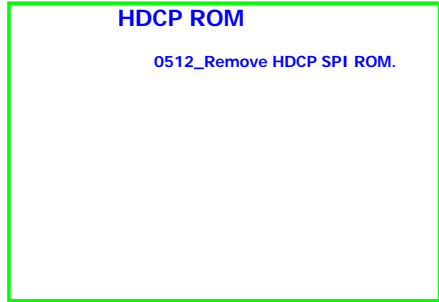
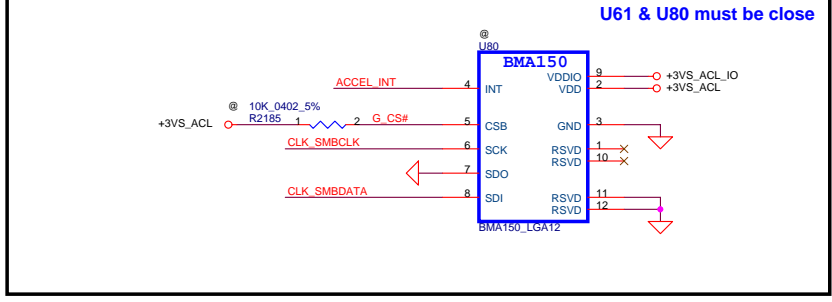
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Rev	0.3	Sheet	29 of 44



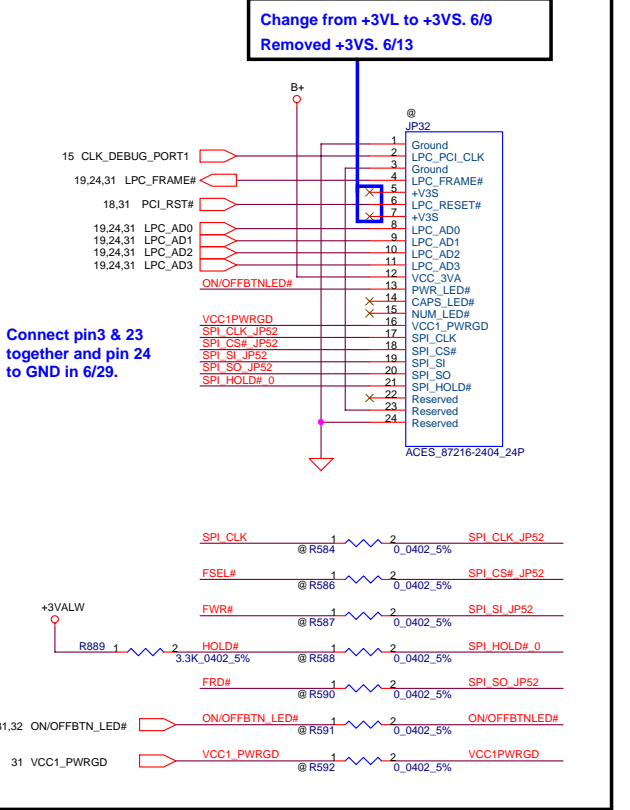
Accelerometer-1



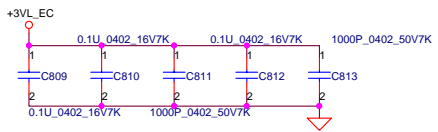
Accelerometer-2



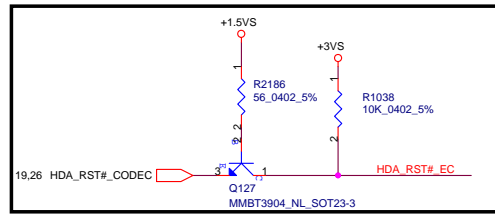
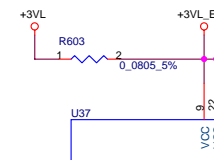
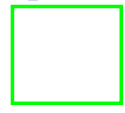
LPC debug port



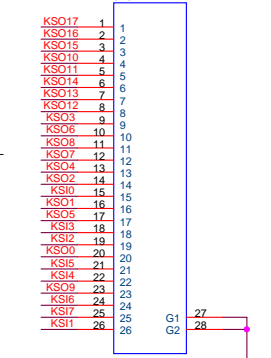
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Issued Date	2006/02/13	Deciphered Date	2006/07/26	BIOS ROM	
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				Date:	Friday, May 23, 2008
				Sheet	30 of 44



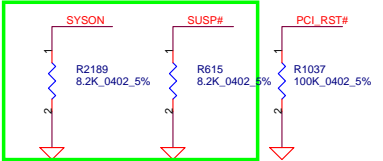
0512_Remove C1009.



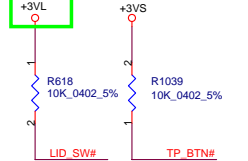
17" INT_KBD CONN.(TYPE "D" KB)



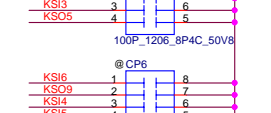
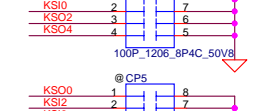
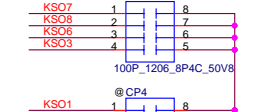
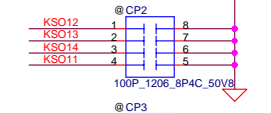
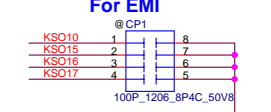
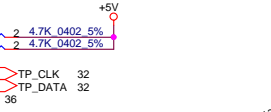
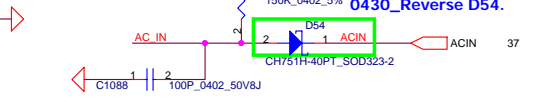
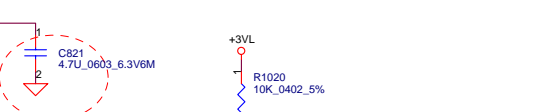
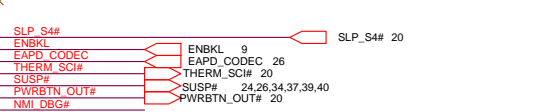
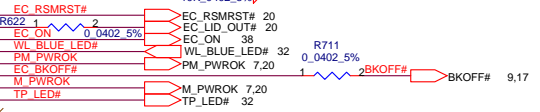
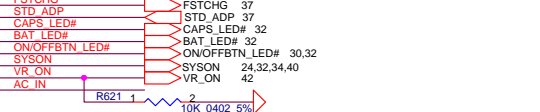
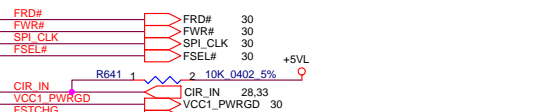
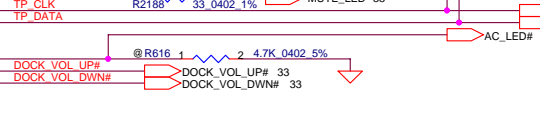
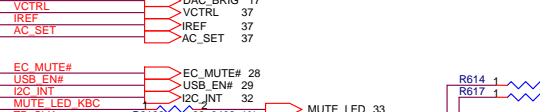
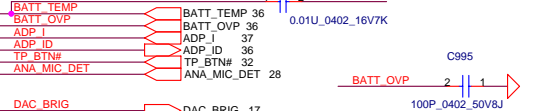
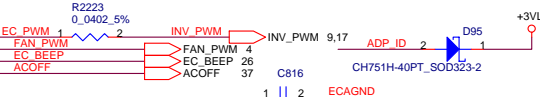
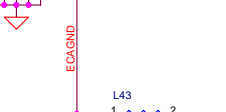
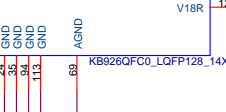
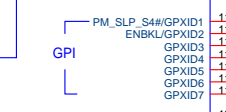
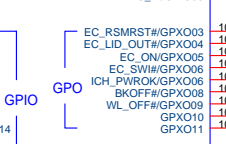
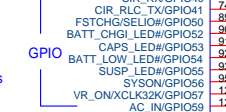
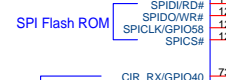
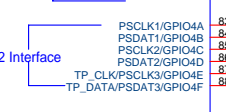
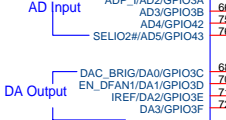
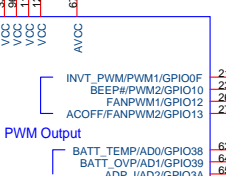
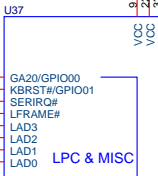
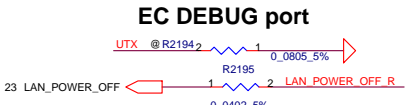
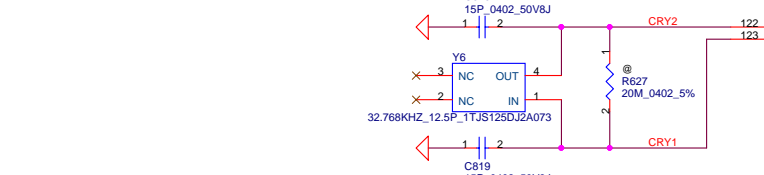
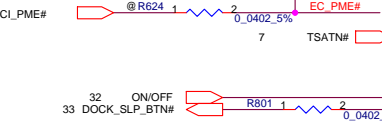
0430_Change from 100K ohm to 8.2K ohm.



0502_Change from +3VALW to +3VL.

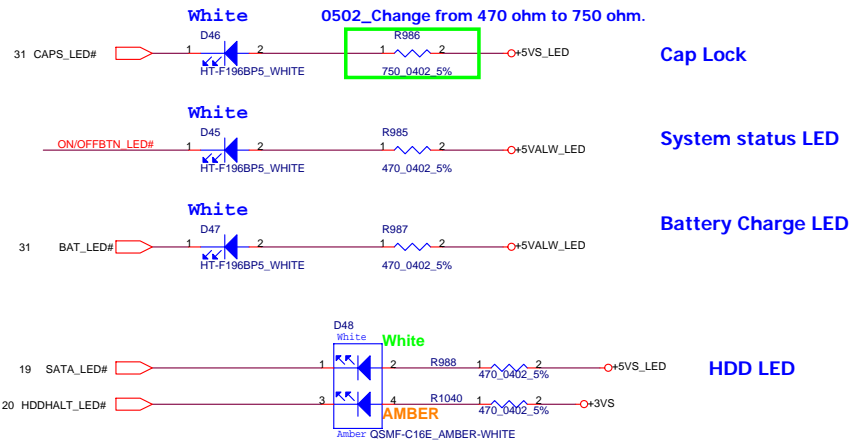


0430_Change from +3VL to +3VALW.



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Document Number	Montevina Consumer Discrete		Date	Friday, May 23, 2008
Sheet	31	of	44	

LED



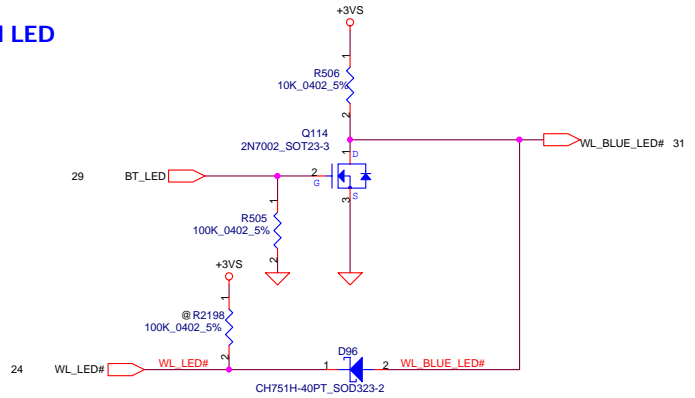
Cap Lock

System status LED

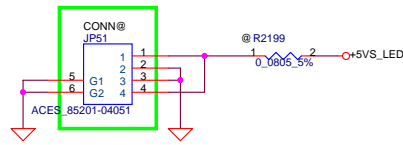
Battery Charge LED

HDD LED

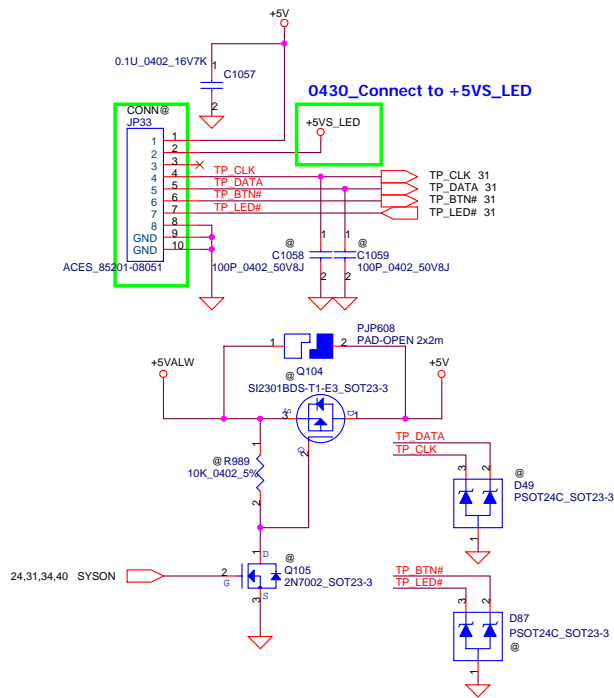
Mini-PCIE Card LED



K/B backlight

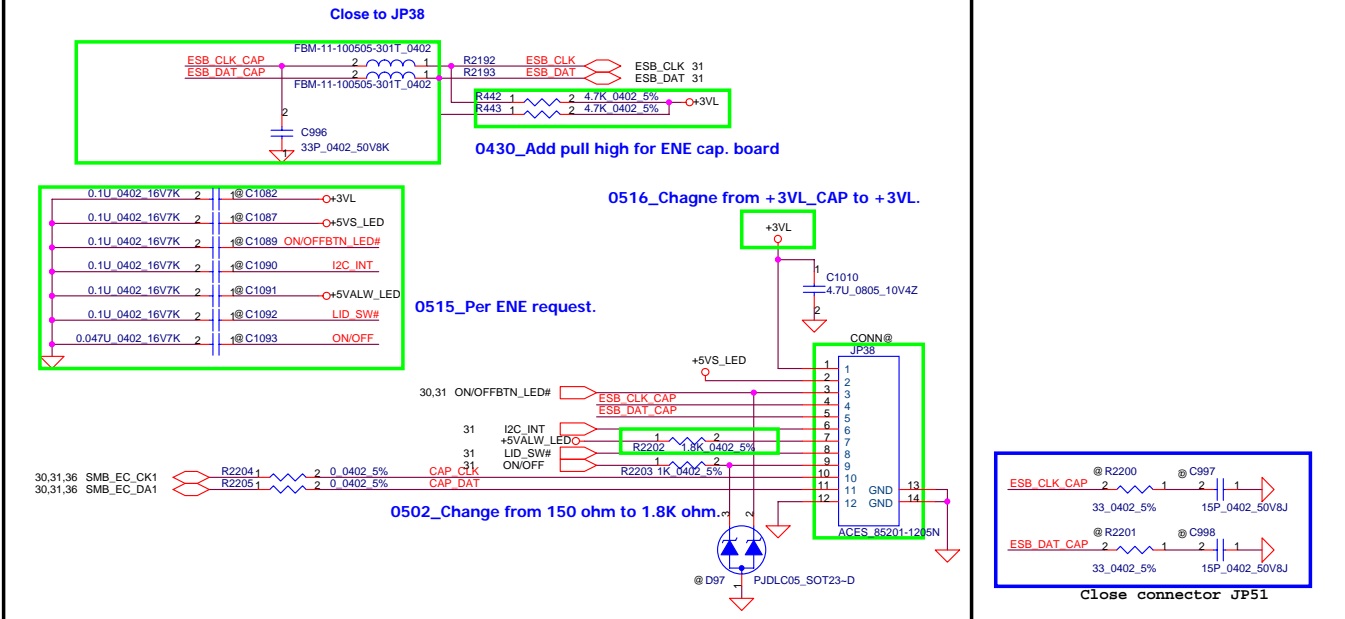


T/P Board (Include T/P_ON/OFF)



0430_Connect to +5VS_LED

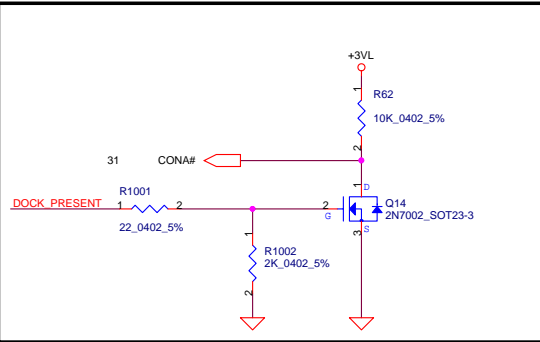
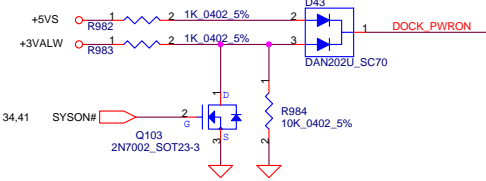
SWITCH BOARD.



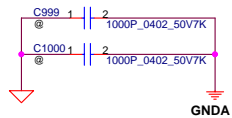
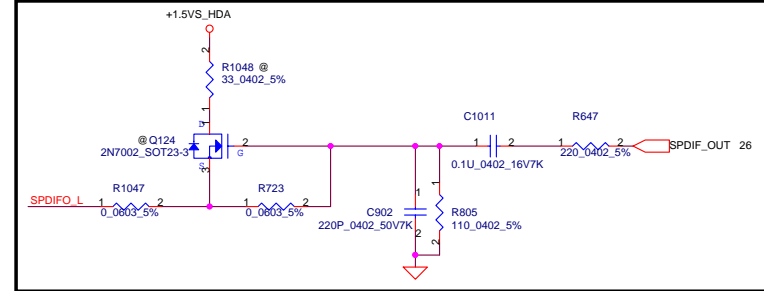
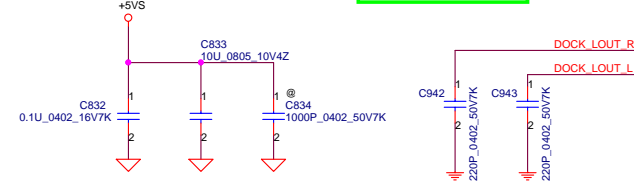
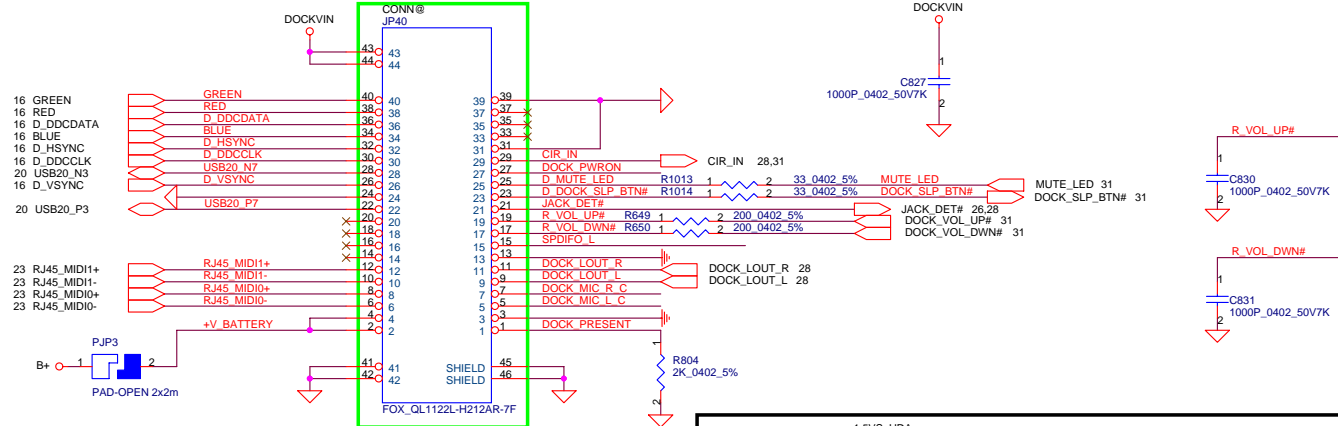
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Issued Date	2006/02/13	Deciphered Date	2006/07/26	Document Number	KBD, ON/OFF, SW, CIR	
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				Sheet	32	of 44

DOCK_PWR_ON Spec

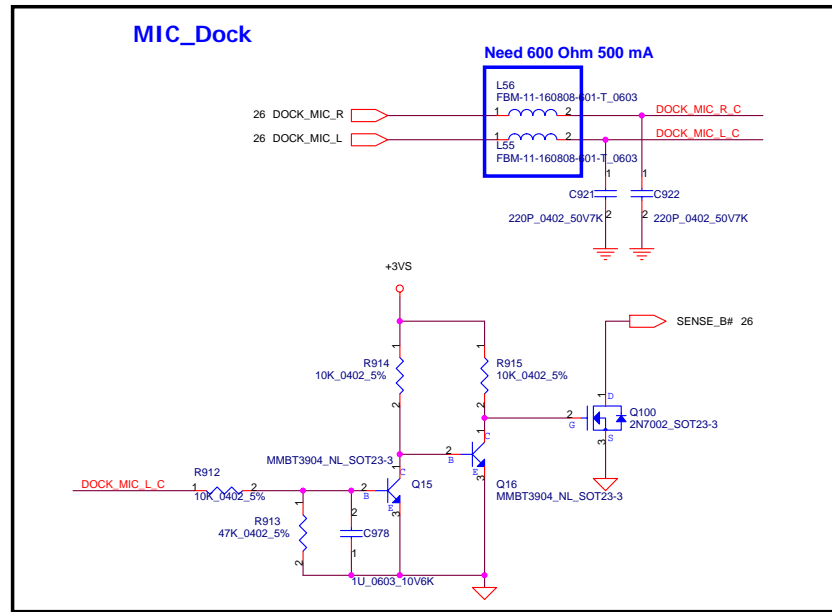
0V = Notebook S4/S5, Dock off
 2.5V = Notebook S3, Dock on
 4V = Notebook S0, Dock on



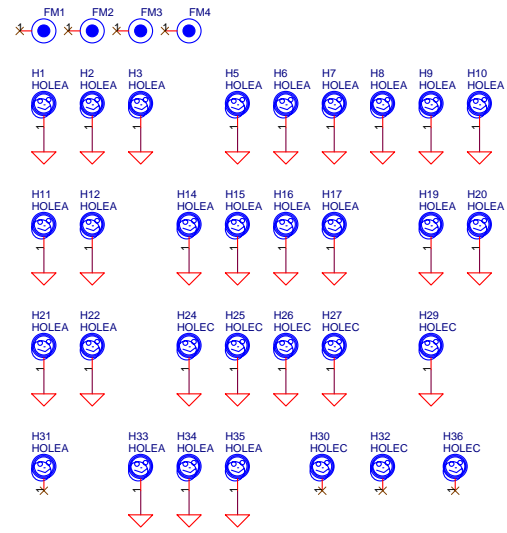
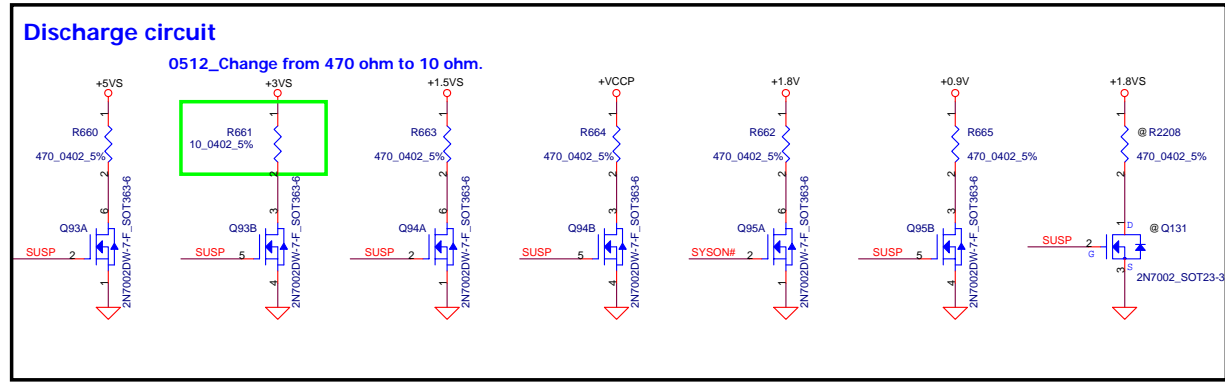
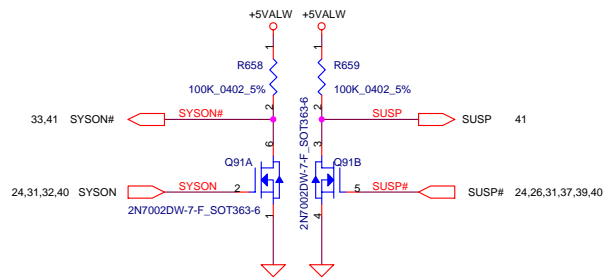
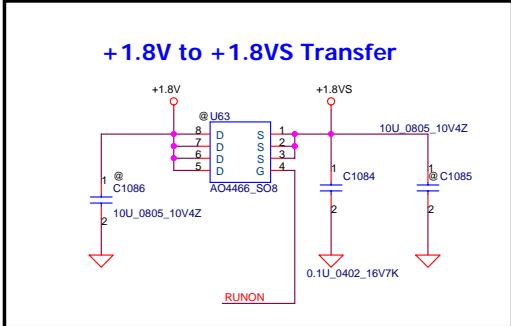
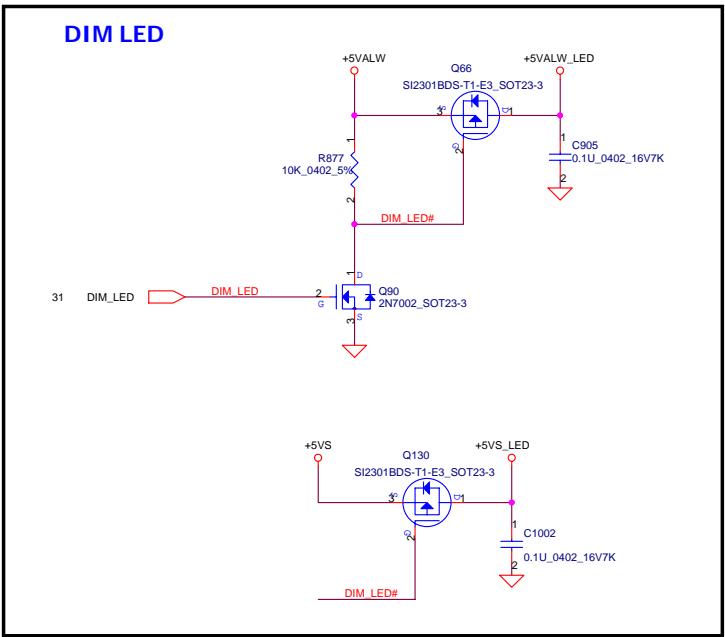
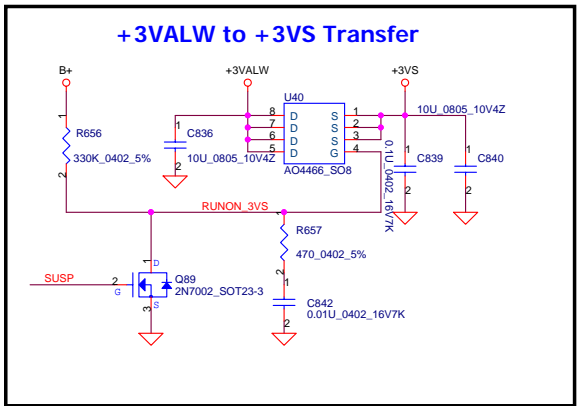
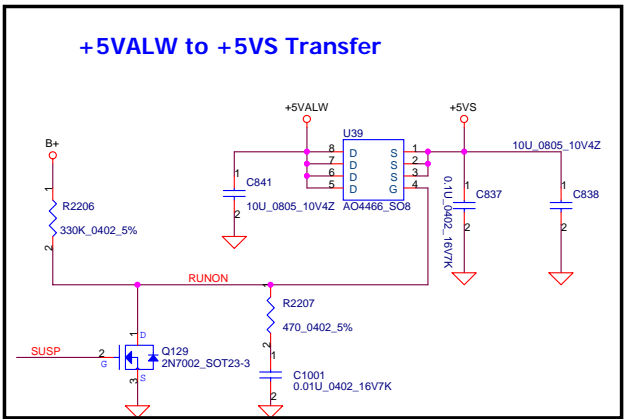
Atlas/ Saturn Dock



MIC_Dock

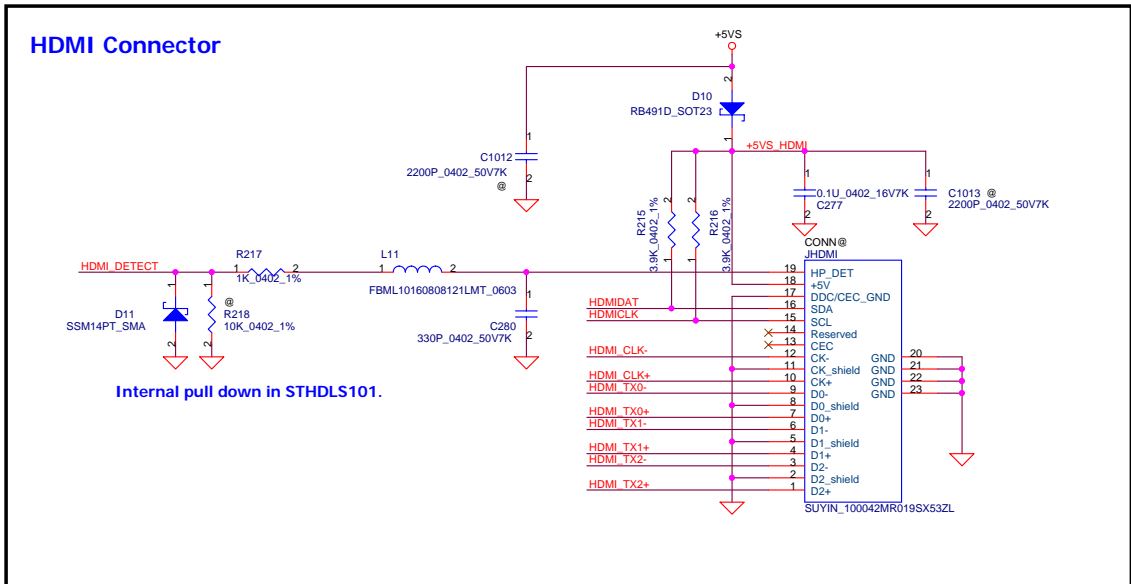
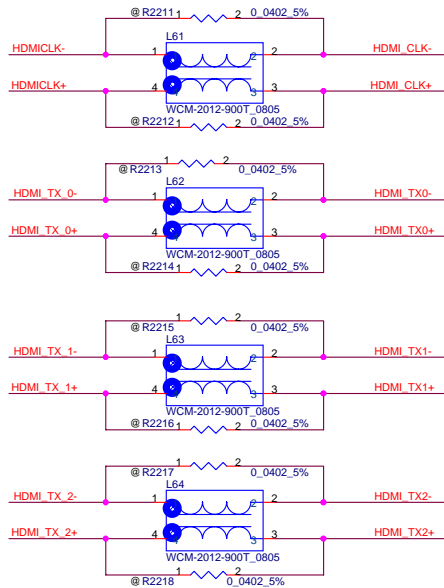
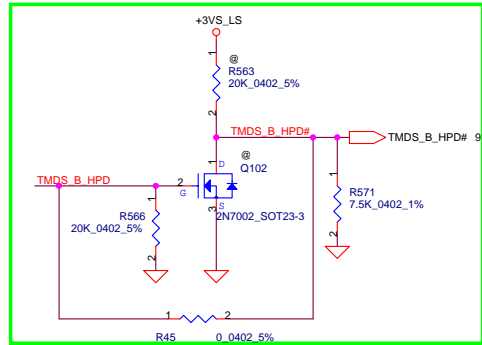
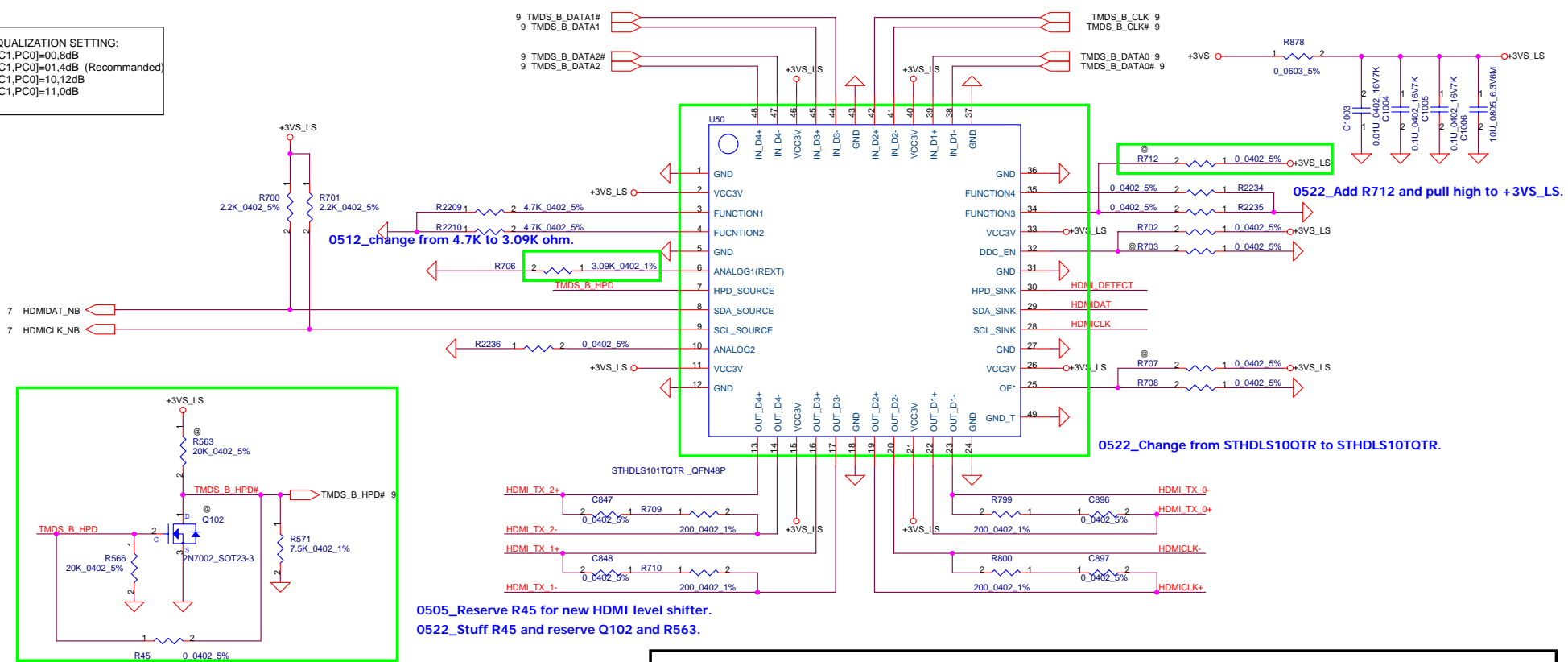


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Date:	Friday, May 23, 2008	Sheet	33	of 44

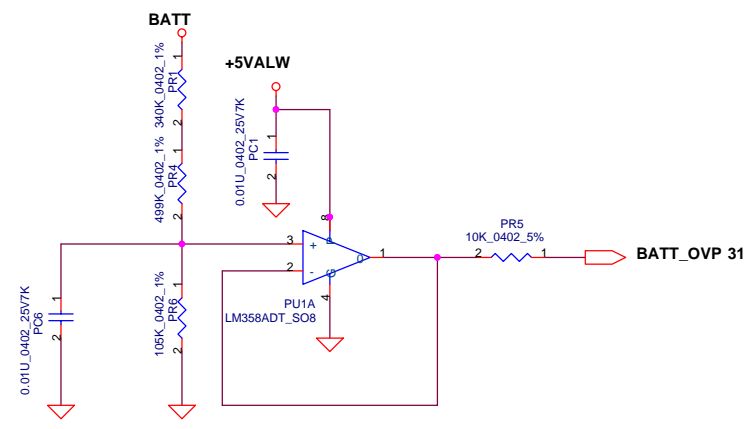
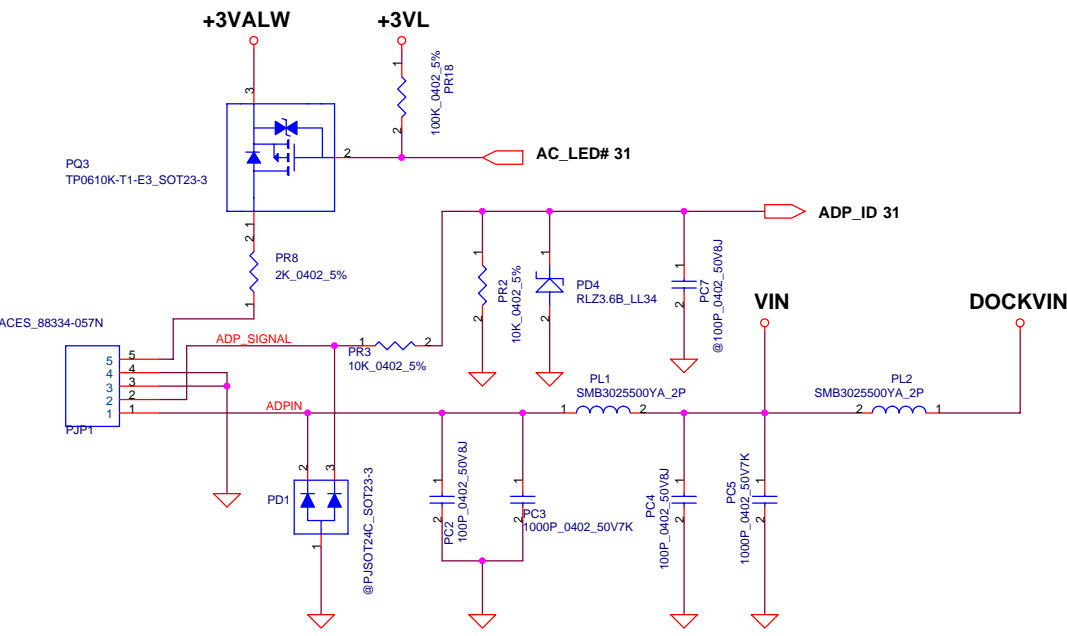


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Date:	Friday, May 23, 2008	Sheet	34	of	44	Rev 0.3

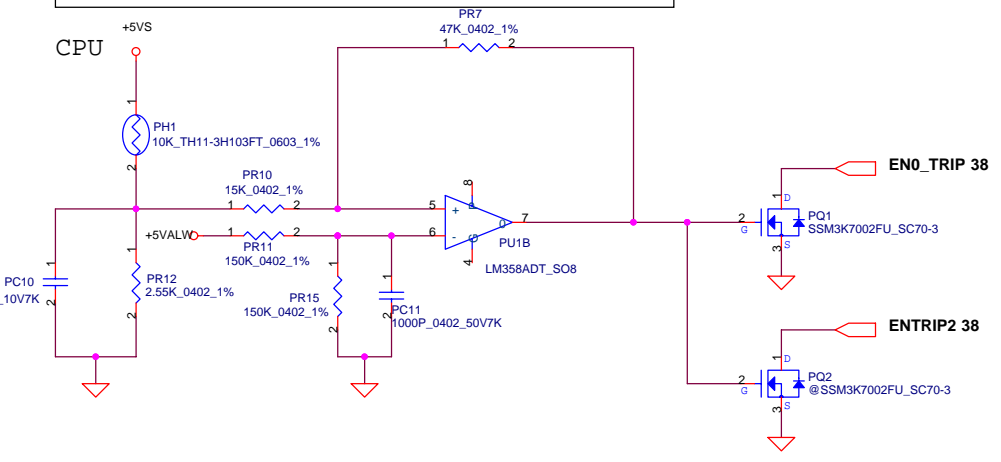
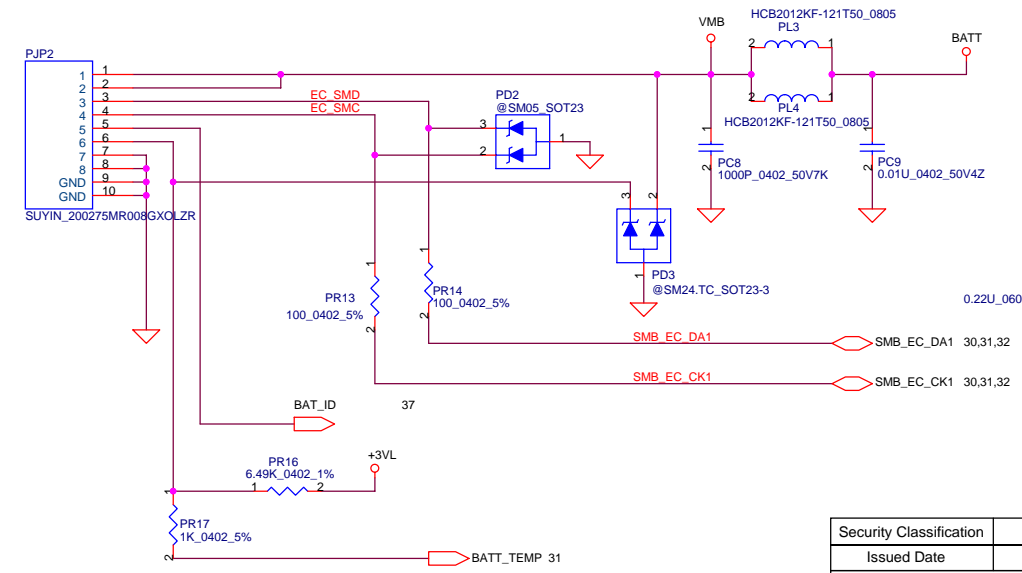
EQUALIZATION SETTING:
 [PC1,PC0]=00,8dB
 [PC1,PC0]=01,4dB (Recommended)
 [PC1,PC0]=10,12dB
 [PC1,PC0]=11,0dB



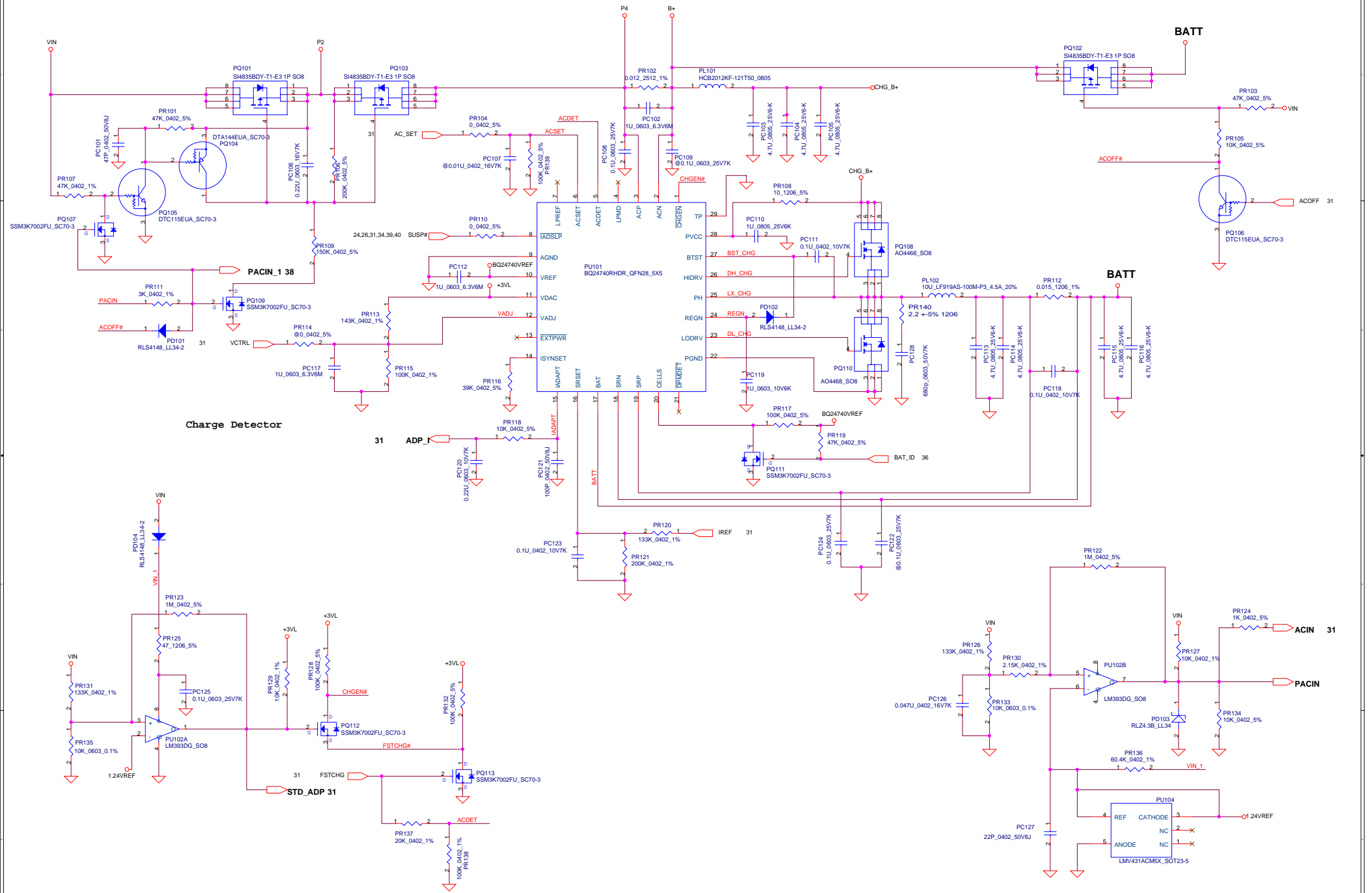
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Issued Date	2006/02/13	Deciphered Date	2006/03/10	HDMI LS & Conn.	
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Date:	Friday, May 23, 2008	Sheet	35 of 44		



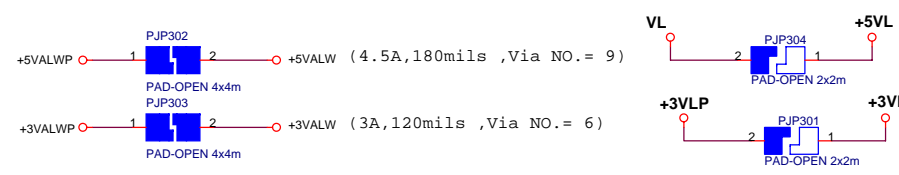
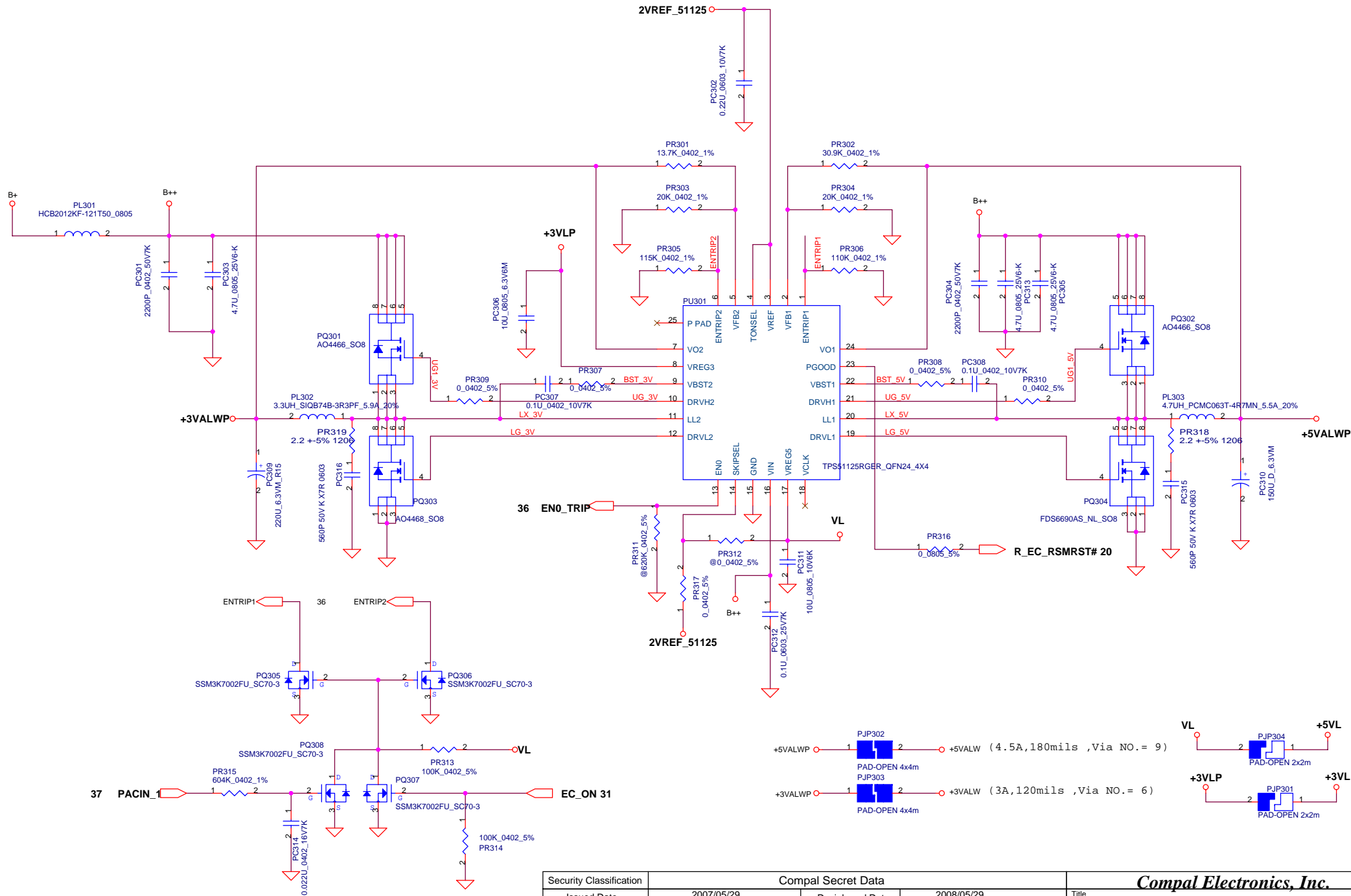
PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 47 +/-3 degree C



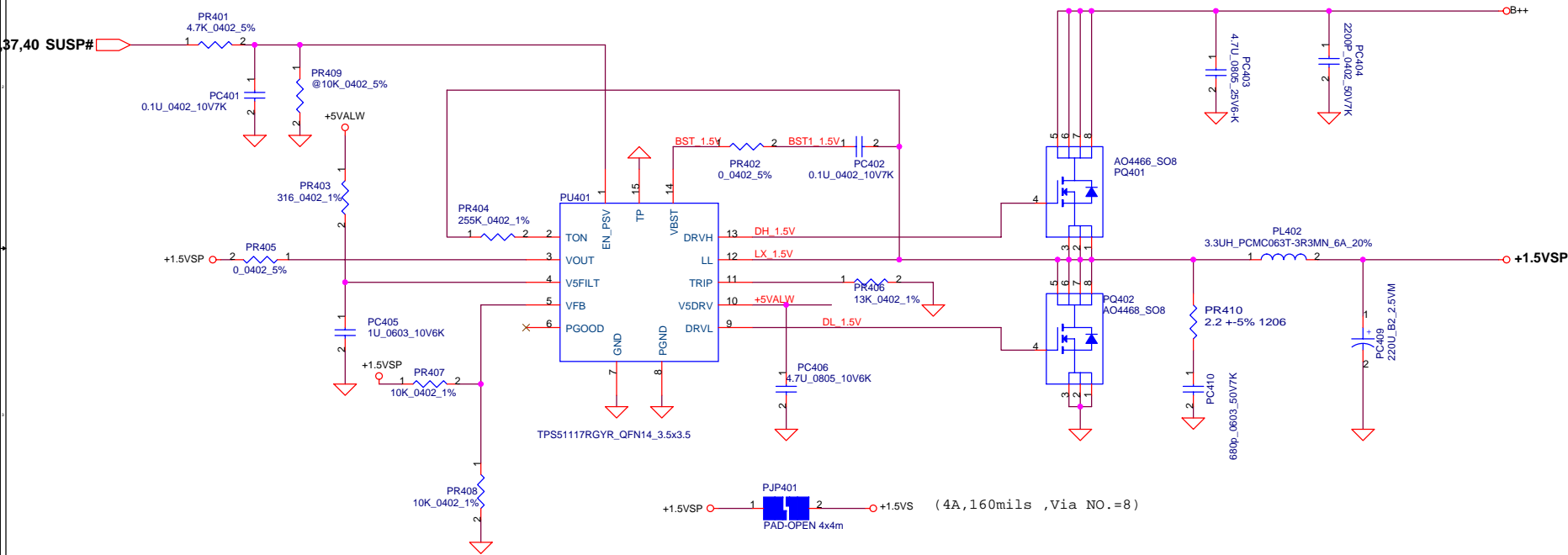
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2007/05/29	Deciphered Date	2008/05/29	Title	DC Connector/CPU OTP
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Size	Document Number	Date	Friday, May 23, 2008	Sheet	36 of 44
	Montevina Consumer Discrete	Rev	0.3		



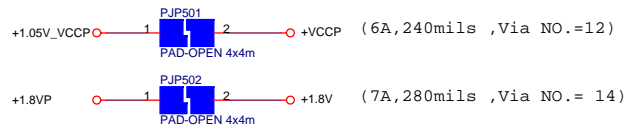
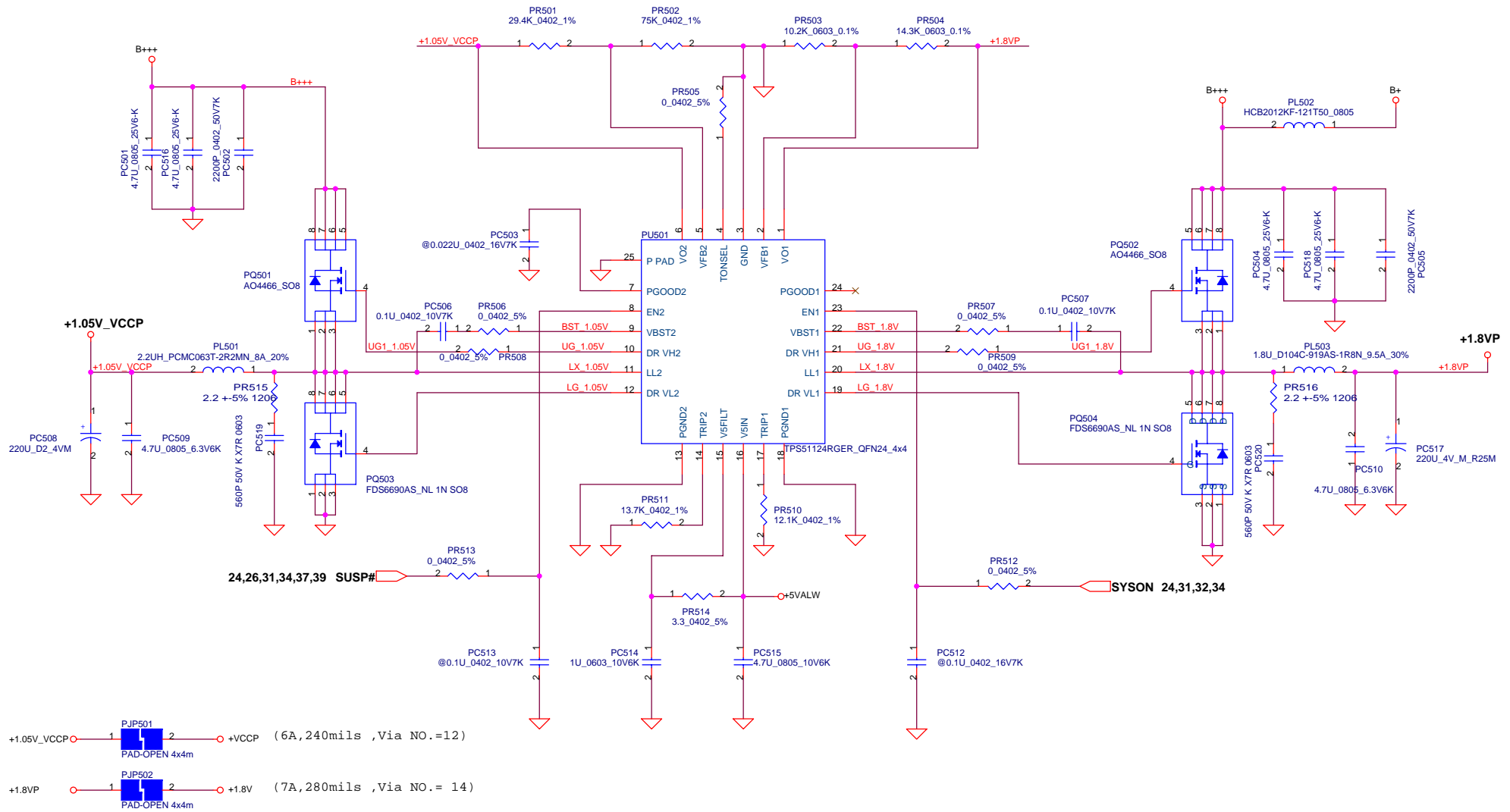
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Issued Date	2007/05/29	Deciphered Date	2008/05/29	Charger	
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Size	Document Number	Montevina Consumer Discrete		Rev	0.3
Date:	Friday, May 23, 2008	Sheet	37	of 44	



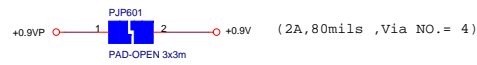
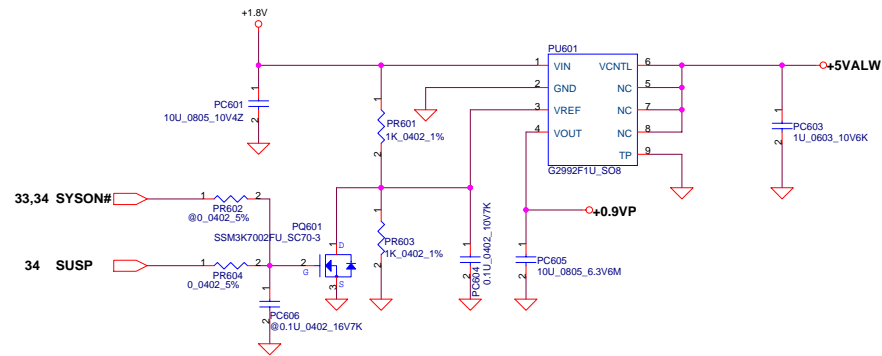
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Date: Friday, May 23, 2008				Sheet 38	of 44



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Date: Friday, May 23, 2008				Sheet 39	of 44



Security Classification		Compal Secret Data		Title	
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				Montevina Consumer Discrete	0.3
Date: Friday, May 23, 2008				Sheet	40 of 44



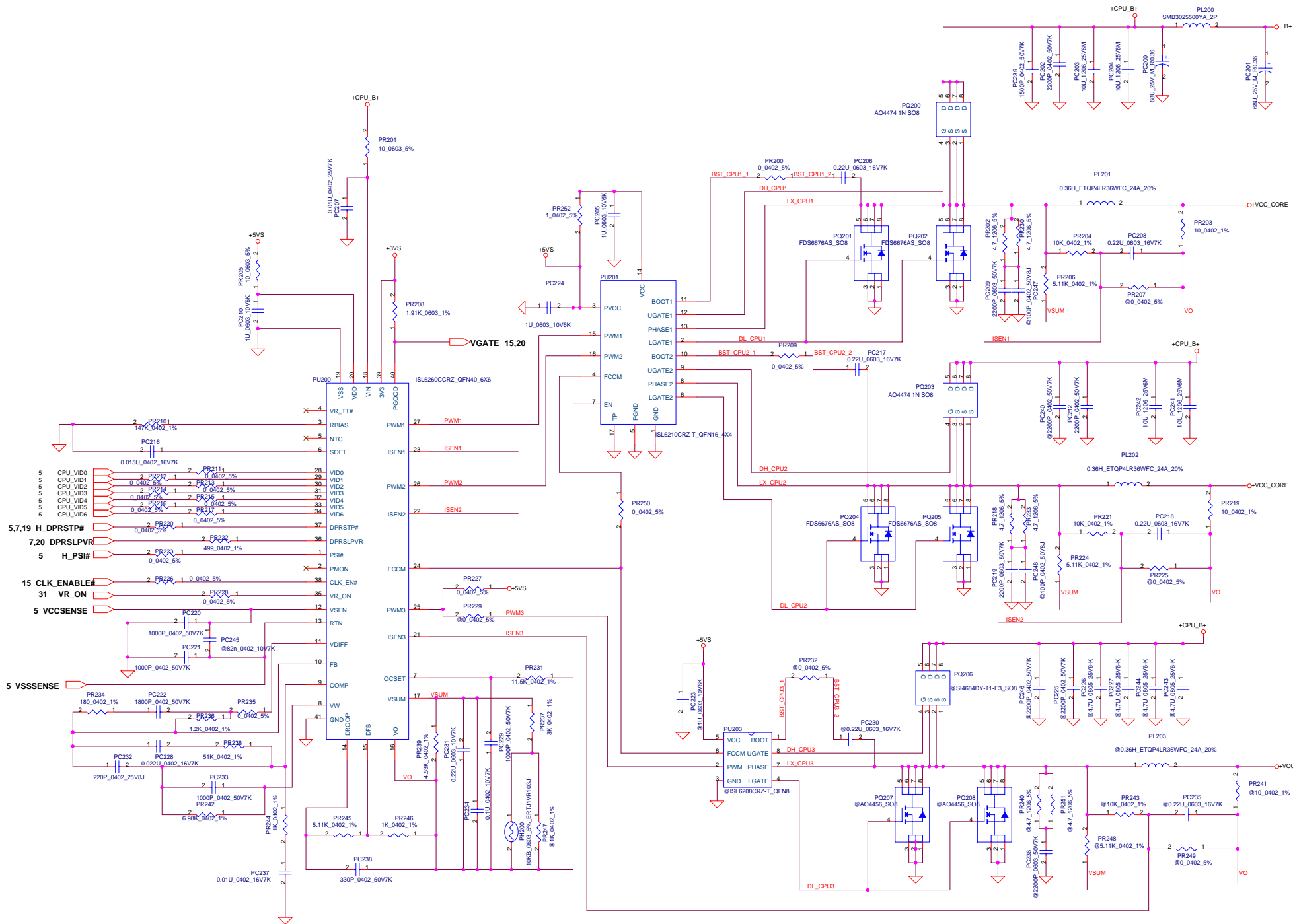
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Date: Friday, May 23, 2008				Sheet	41 of 44

Compal Electronics, Inc.

0.9VP

Montevina Consumer Discrete

Date: Friday, May 23, 2008 Sheet 41 of 44



5

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Title		
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Size	Document Number	Rev
A	<Doc>	0.3
Date:	Friday, May 23, 2008	Sheet 43 of 44

5

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1

Item	PAGE	Fixed Issue	Request by	Modify List	Date	Note
01	04	System thermal shutdown when use NS thermal sensor	HW	Change R8 and R9 from 100 ohm to 0 ohm. Comfirm with SMSC this change is no risk for EMC1402.	0430	SI --> PV
02	31	Follow JAK00 DIS design	HW	Change R2189 and R615 from 100K ohm to 8.2K ohm.	0430	SI --> PV
03	31	Follow JAK00 DIS design	HW	Change EC_PME# pull high power rail from +3VL to +3VALW.	0430	SI --> PV
04	31	Solve AC LED always light even without AC adapter.	HW	Reverse D54 for AC_IN.	0430	SI --> PV
05	32	Solve T/P LED always light even power off.	HW	Change T/P LED power rail from +5VALW_LED to +5VS_LED.	0430	SI --> PV
06	24	Solve +3VS/+5VS has leakage power when S5 and S3.	HW	Reseve R2160.	0430	SI --> PV
07	09	Remove useless component because JAK00 do not support WWAN.	HW	Remove C1018~C1025.	0430	SI --> PV
08	28	Remove useless component.	HW	Remove C990 and C991 (1uF_0603).	0430	SI --> PV
09	31	For ENE cap. board.	HW	Add R442 and R443.	0430	SI --> PV
10	32	Fine-tune LED brightness (Power LED and Cap Lock LED).	HW	Change R2202 to 1.8K ohm and R986 to 750 ohm.	0502	SI --> PV
11	31	To avoid Lid function abnormal when battery mode only.	HW	Chagne Lid Switch power rail from +3VALW to +3VL.	0502	SI --> PV
12	28	Reserve 0603 package if EMI need to stuff bead.	HW	Change from 0402 to 0603 size.	0502	SI --> PV
13	35	To match ST new chipset (internal Hot Plug inverse circuit).	HW	Reserve R45.	0505	SI --> PV
14	09	Double confirm NB strapping setting with CRB. it can solve flash display.	HW	Change R70 to pull low ; reserve R65 ; reserve R66, R77 (reserve R66, R77 to solve flash display)	0505	SI --> PV
15	19	Follow Intel design guild, add pull high 10k ohm for SATA_LED#	HW	Add R49 and pull high to +3VS.	0505	SI --> PV
16	15	Reserve R714 because already pull high near North Bridge.	HW	Reserve R714.	0505	SI --> PV
17	24	Solve +3VS power leakage when S3/S4/S5.	HW	Reserve R485.	0505	SI --> PV
18	17	Solve internal MIC has noise when recording.	HW	Reserve C302 and C303.	0509	SI --> PV
19	26	Solve EMI issue for digital MIC (follow Vader DIS).	EMI	Add L10.	0509	SI --> PV
20	30	Follow common design.	HW	Add pull high R61 for SPI WP# and HOLD#.	0510	SI --> PV
21	19	Follow Intel check list.	HW	Change R363 from 180K ohm to 20K ohm and C538 from 0.1uF to 1uF.	0510	SI --> PV
22	24	Follow vender's recommend.	HW	Separate PCIe and USB card present.	0510	SI --> PV
23	04	Delete XDP debug port to solve EMI issue.	EMI	Delete JP42, R730, R733~R735, R738~R741, C851.	0512	SI --> PV
24	15	Delete XDP debug port to solve EMI issue.	EMI	Delete R134 and R135 (Remove XDP clock for XDP port).	0512	SI --> PV
25	20	Remove external HDCP interface.	HW	Delete R440~R441, R1008~R1010.	0512	SI --> PV
26	30	Remove external HDCP ROM.	HW	Delete R438~R439, R415, R422, R427, C304, and U8.	0512	SI --> PV
27	20	Remove useless function.	HW	Reserve R1040.	0512	SI --> PV
28	35	Fine-tune HDMI signal quality.	HW	Change R706 from 4.7K to 3.09K ohm.	0512	SI --> PV
29	15	Solve EMI issue.	EMI	Reserve R126.	0512	SI --> PV
30	34	Solve leakage power for VCC_HV of north bridge when S3/S4/S5..	HW	Base on Intel recommend, change R661 of +3VS discharge circuit from 470 ohm to 10 ohm	0512	SI --> PV
31	31	Solve can not power on issue if +3VL output cap. total over 20uF.	HW	Delete C1009.	0512	SI --> PV
32	28	Audio fail for ESD test.	ESD	Connect U30 thermal PAD to GNDA.	0515	SI --> PV
33	26	Audio fail for ESD test.	ESD	Connect U56 thermal PAD to GNDA.	0515	SI --> PV
34	16	Follow Blade/Vader DIS use the same material.	HW	Change L13, L15, L17.	0515	SI --> PV
35	32	Solve EMI issue for ENE cap. board.	ENE	Stuff R2192, R2193, and C996.	0515	SI --> PV
36	32	Solve EMI issue for ENE cap. board.	ENE	Add C1082, C1087, C1089~C1093.	0515	SI --> PV
37	32	Remove useless parts (LDO for ENE cap. board).	HW	Remove U79, R2139, C2126, C2127, PJP607.	0516	SI --> PV
38	32	Remove useless parts (LDO for ENE cap. board).	HW	Chagne JP38 pin1 power from +3VL_CAP to +3VL.	0516	SI --> PV
39	26	Solve MIC jack detect abnormal when plug in Dock.	HW	Change to right part number for R524 (39.2K_0402).	0519	SI --> PV
40	20	Solve pop noise when press CTRL+ALT+DEL.	HW	Reserve R424.	0520	SI --> PV
41	17	Solve wavy issue in CRT monitor.	HW	Add PJP305 to sparate GND.	0521	SI --> PV
42	17	Remove useless part.	HW	Remove LB.	0521	SI --> PV
43	26	Solve ESD test fail for Audio.	HW	Reserve R69 and C728.	0521	SI --> PV
44	29	For ESD request.	ESD	Delete R2183.	0522	SI --> PV
45	35	There is inverse circuit internal in new version chipset for HPD signal.	HW	Change U50 from STHDLS10QTR to STHDLS10TQTR.	0522	SI --> PV
46	35	Reserve inverse circuit.	HW	Reserve Q102 and R563.	0522	SI --> PV
47	35	Follow vender's recommend.	HW	Add R712 and pull high to +3VS_LS.	0522	SI --> PV
48	10	To prevent wavy issue in CRT.	HW	Add C148.	0522	SI --> PV