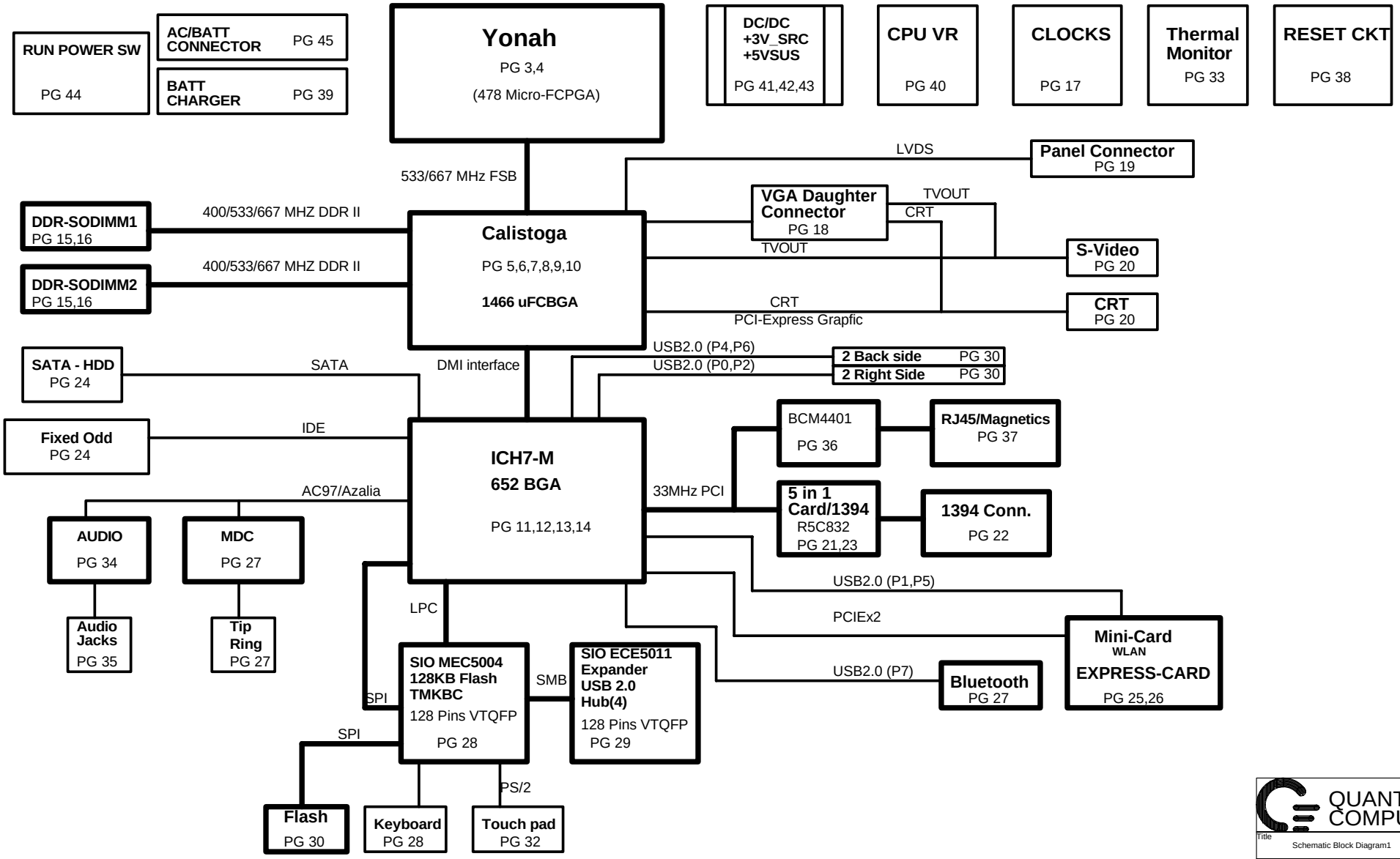
KEYLARGO

VER : 1A



QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 1 of 48	

INDEX

Pg#	Description	DNI LIST
1	Schematic Block Diagram 1	
2	Blank Page	
3	Front Page	
4-5	Dothan	
6-10	Alviso	
11-13	ICH6	
14-15	DDRII SO-DIMM(200P)	
16	Clock Generator	
17	CH7306/7	
18-19	Blank Pages	
20	LCD Conn. & SSP	
21	CRT & TV Conn.	
22	SATA & IDE Conn.	
23	Screw Hole	
24	TI PIC6515	
25	Mini PCI Conn.	
26	MDC Conn.	
27-28	SIO (LPC47N354)	
29	SERIAL PORT & USB	
30	PARALLEL CONN.	
31	Flash ROM	
32	TOUCH PAD & BLUE TOOTH	
33	Switch Board Conn. & LED	
34	FAN & Thermal	
35-36	Audio CODEC (STAC9751) & Phone Jack	
37-38	LOM (BCM5751), Switch	
39	FIR	
40-41	Docking Conn. & Q-Switch	
42	Power Good	
43-44	Battery Selector & Charger	
45	CPU Power	
46	1.8V,0.9V,1.5V,1.05V	
47	3VALW/5V/3V/Power ON	
48	RUN Power Switch	
49	VGA DC/DC	
50	DCIN/Batt Conn.	

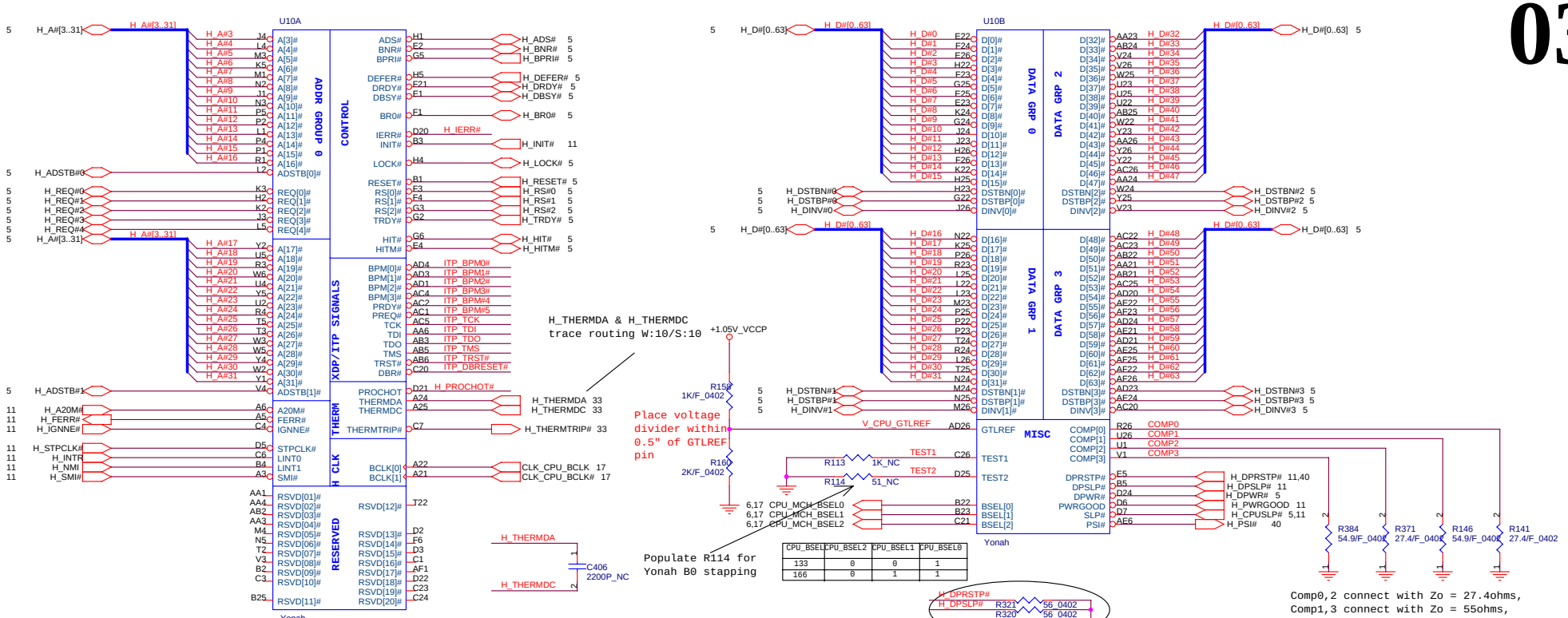
Power & Ground

Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (20V)	
PBATT+		MAIN BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~20V)	
RTC_PWR3_3V		RTC & PCL POWER (3_3V)	
+12V		+12V	DRUNPWROK
VHCORE		CPU CORE POWER (1.25/1.15V)	RUNPWROK
V1_2RUN		AGTL+ POWER (1.2V)	RUNPWROK
+3VRUN		SLP_S3# CTRLD POWER	RUN_ON
+3VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VALW		8051 POWER (5V)	
+5VRUN		SLP_S3# CTRLD POWER	RUN_ON
+5VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VHDD		HDD POWER (5V)	HDDC_EN#
+5VMOD		MODULE POWER (5V)	MODC_EN#
STRB#/5V		EXTERNAL FDD POWER (5V)	FDD/LPT#
+5VFAN1, +5VFAN2		FAN POWER (5V)	FAN_OFF/ON#
VDDA		AUDIO ANALOG POWER (5V)	RUN_ON
1_8VSUS		RESUME WELL IN ICH	
1_8VRUN		SLP_S3# CTRLD POWER	
+3VALW		8051 POWER (3V)	
V1_5RUN		AGP I/O POWER	
GND	ALL PAGES	DIGITAL GROUND	
GNDP		CPU POWER GND	
CGNDP		CHARGER GND	
DGNDP		DC/DC POWER GND	
LANGND		COMBO CONN GND	

02

QUANTA COMPUTER

Title	Index, DNI, Power & Ground	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 2 of 48	



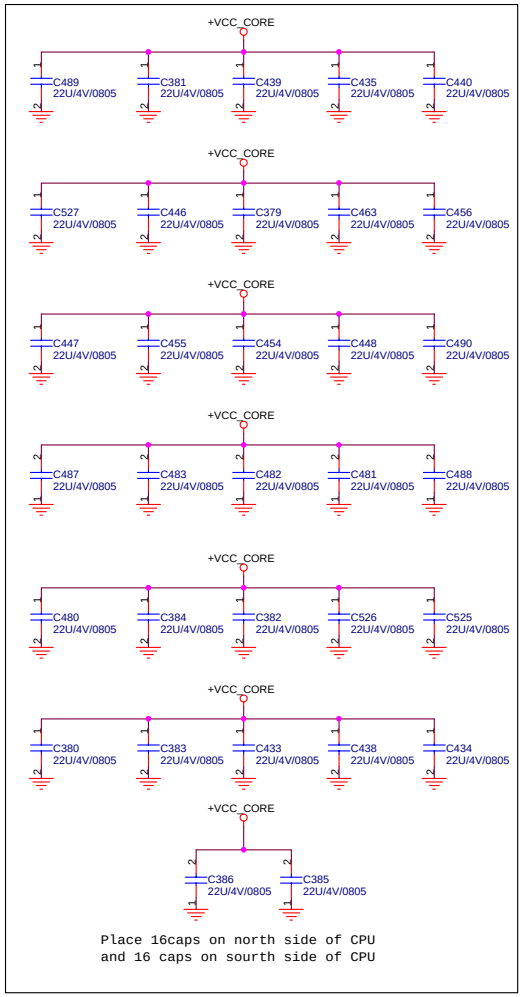
CPU_BSEL2	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

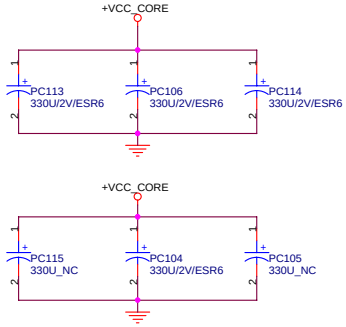
ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
ITP_TDI	150 ohm +/- 5%	+1.05V_VCCP	Within 2.0" of the CPU
ITP_TMS	39 ohm +/- 5%	+1.05V_VCCP	Within 2.0" of the CPU
ITP_TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
ITP_TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	N/A	Within 2.0" of the CPU

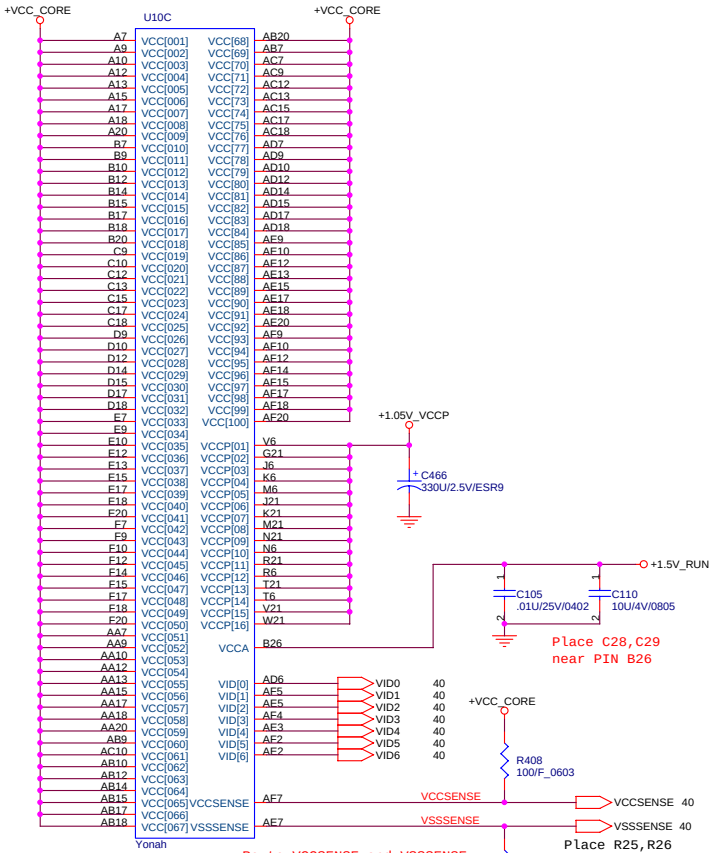
QUANTA COMPUTER

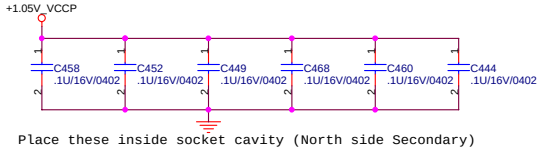
Title	Yonah Processor (HOST)	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 3 of 48	

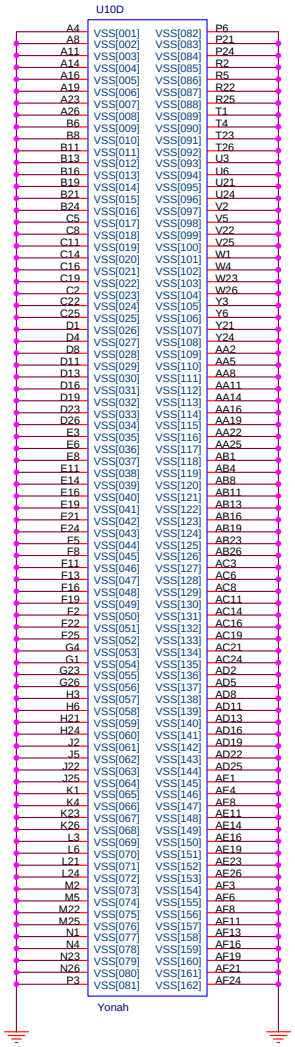




Total caps = 2684 uF
ESR =6m ohm/4 // 3m ohm/32

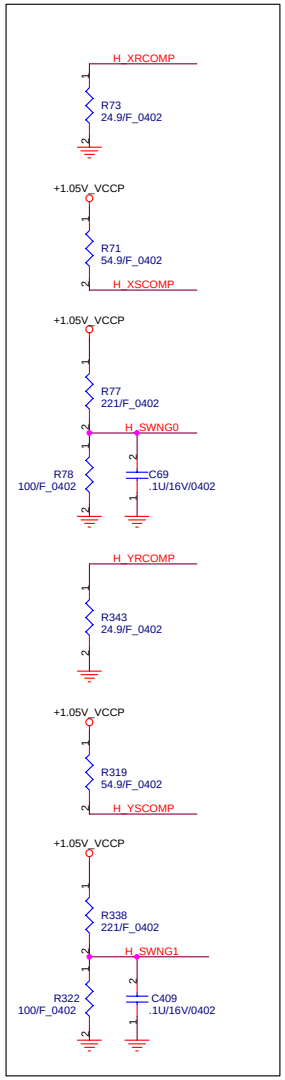






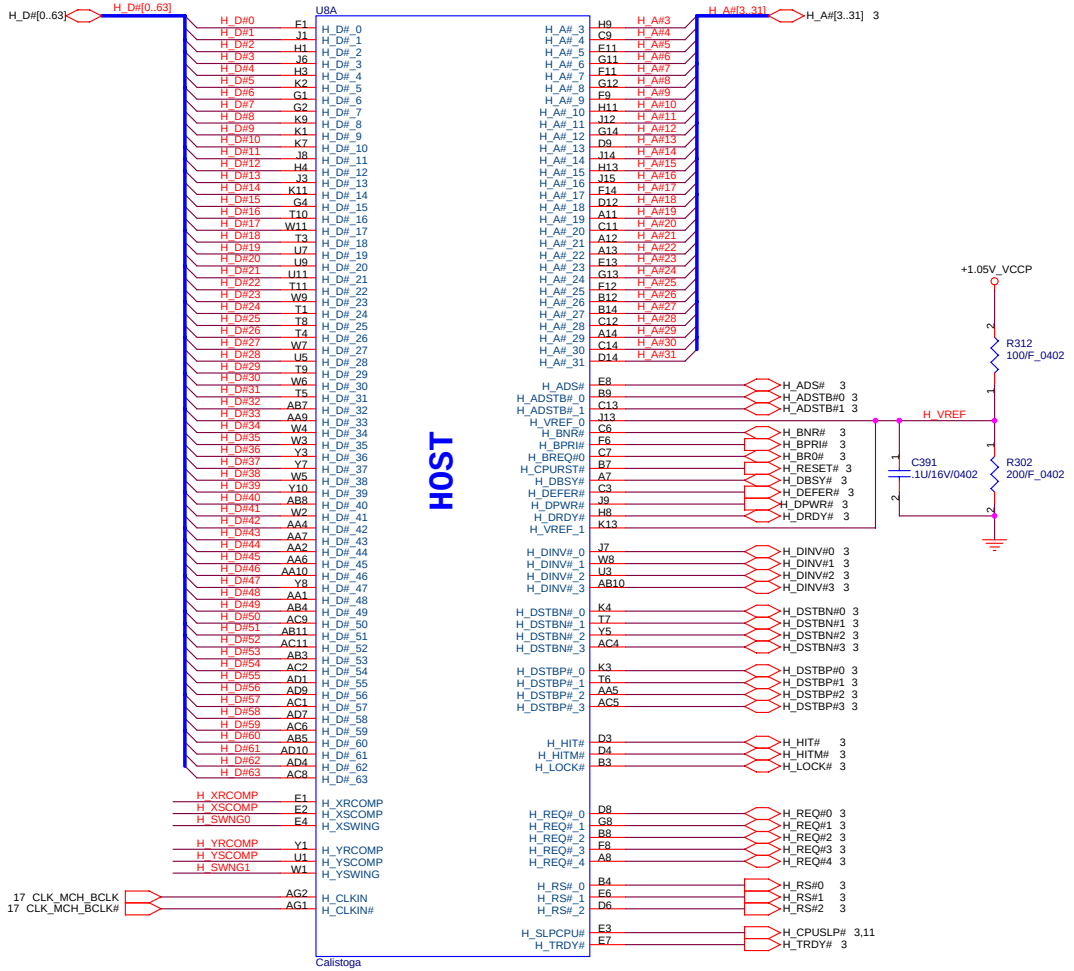
QUANTA COMPUTER

Title	Yonah Processor (POWER)	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 4 of 48	



H_XRCOPM, H_XSCOMP, H_YRCOMP, H_YSCOMP, H_SWNG0, H_SWNG1 used W:10/S:20 mil.

R & C of HXRCOPM, HXSCOMP, HYRCOMP, HYSCOMP, H_SWNG0, H_SWNG1 trace length less 0.5" from U3



QUANTA COMPUTER

Title	Calistoga (Host)	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 5 of 48	

Note:
CFG3:17 has internal pullup; CFG18:19 has internal pulldown

CFG[2:0]
001=FSB533
011=FSB667
Others = Reserved

Low=DMIx2
High=DMIx4

For Discrete:
De-populate
R286,R275

Populate R82,R83 for A1 Calistoga(MCH).

For Discrete:
Populate R298,R63,R299,R57
De-populate R58,R84,R301,R310

For Discrete:
Populate R32,R35,R37,R38,R308,R56
R41,R54,R232,R290,R300,R313.
De-populate: R48,R31,R49,R297,R55
R39,R53,R233,R307,R33

Place C57,C58 close to U3.AK1 & U3.AK41

Update pre GG0504 recomend

For Discrete:
De-populate
R223,R224,RP1,Q4,Q5

Delete R54 per GG0504 recommend

Add R531,R532 per GG0516

Host PLL VCC Select
Low=Reserved
High=Mobility

CPU_Strap
Low=RSVD
High=Mobile CPU

PSB 4X CLK Enable
Low=Calistoga
High=Reserved

PCIE Graphics Lane
Low = Reveise Lane
High = Normal operation

FSB Dynamic ODT
Low=Dynamic ODT Disable
High=Dynamic ODT Enable

VCC Select
Low=1.05V
High=1.5V

DMI Lane Reversal
Low=Normal
High=Lane Reversed

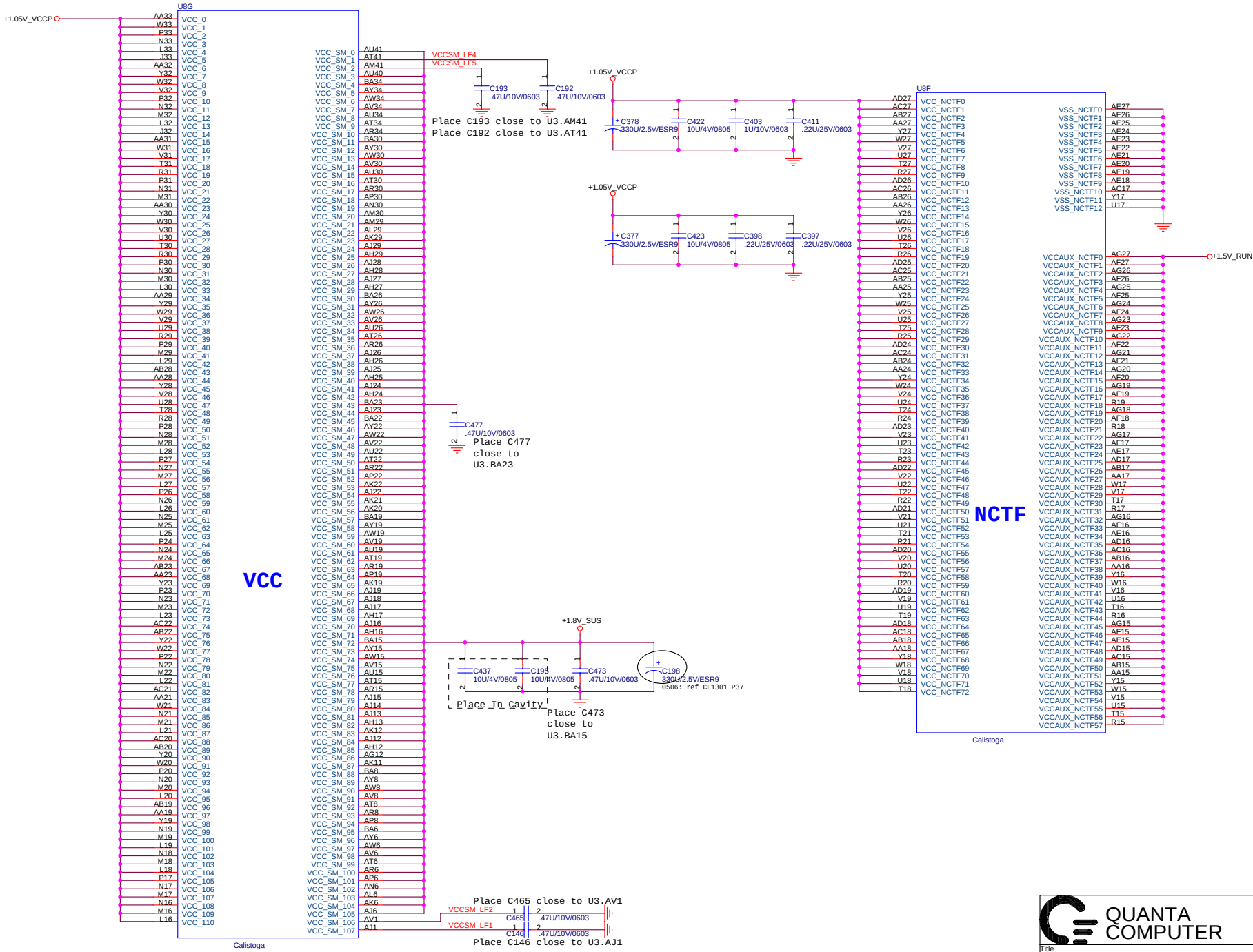
PCIe Backward Interpoerability mode
Low=Only SDVO or PCIEx1 is operational (defaults)
High=SDVO and PCIEx1 are operating simultaneously via PEG port

QUANTA COMPUTER

Title	Calistoga (VGA,DMI)		
Size	Document Number FM1		Rev 1A
Date:	Tuesday, June 28, 2005	Sheet 6 of 48	

QUANTA COMPUTER

Title	Calistoga (DDR2)	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 7 of 48	



Title	Calistoga (VCC, NCTF)	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 8 of 48	

QUANTA COMPUTER

+1.5V_RUN — R449 0.002F_2010 — L31 BLM18PG330SN1 — +1.5VRUN_PCIE
C70 220U/6.3V/ESR25 — C78 10U/4V/0805 — C88 10U/4V/0805
0506: ref CL1301 P35
W=30

+2.5V_RUN — L27 BLM18PG330SN1_NC — +2.5V_CRTDAC
+1.05V_VCCP — R296 0_0805 — C347 .022U_NC — C354 .1U_NC
Place C347,C354 close to U8.E21
U8.F21 less than 250mils.

For Discrete:
Populate R296
Depopulate
L27,C347,C354

U8.G21 should connect to C347
C354 after connect to GND

+2.5V_RUN — R45 0_NC — R50 0_0805 — C38 .1U_NC — C29 4.7U_NC — C36 .1U_NC
For Discrete:
Populate R50
De-populate
R45,C38,C29,C36

Place C29, C36 close to
U4.C30, U4.B30, U4.A30

+1.5V_RUN — L11 BLM18PG181SN1 — +3GPLL_R — R149 0.5/F_0805 — +1.5V_RUN_3GPLL
C191 .1U/16V/0402 — C425 10U/4V/0805 — C419 .1U/16V/0402
+2.5V_RUN — C374 .1U/16V/0402 — VSSA_3GBG

Place C85 to U3.G41
within 200mil

For Discrete:
Depopulate
C340, C337

+1.5V_RUN — L29 10uH_60mA — C364 .1U/16V/0402 — +1.5V_RUN_DPLLA — C340 470U_NC — 40mA Max.
L30 10uH_60mA — C373 .1U/16V/0402 — +1.5V_RUN_DPLLB — C337 470U_NC — 40mA Max.

+1.5V_RUN — L7 BLM11A121S — C129 .1U/16V/0402 — +1.5V_RUN_HPLL — C123 22U/10V/1206 — 45mA Max.
L32 BLM11A121S — C426 .1U/16V/0402 — +1.5V_RUN_MPLL — C431 22U/10V/1206 — 45mA Max.

+2.5V_RUN — R46 0_NC — C31 .1U_NC — C34 .01U_NC — R29 0_0805
For Discrete:
Populate: R29
Depopulate:
R46, C31,C34

+1.5V_RUN — R272 0_NC — R258 0_0805 — C356 10U_NC — C362 .1U_NC
For Discrete:
Populate R258
De-populate
R272,C356,C362

+3.3V_RUN — C328 10U/10V/0805 — C369 1U/16V/0402

+1.5V_RUN — C421 .1U/16V/0402

Delete C108,C113,C118
per ref schematic

+3V_TVDAC
+3.3V_RUN — L26 BLM18PG181SN1_NC — C335 10U_NC
C40 .1U_NC — R44 0_0603 — +3.3V_RUN_TVDACA — C43 22nF_3P_NC
C346 .1U_NC — R253 0_0603 — +3.3V_RUN_TVDACB — C349 22nF_3P_NC
+1.5V_RUN — R34 0_0805 — C350 .1U_NC — R250 0_0603 — +3.3V_RUN_TVDACC — C348 22nF_3P_NC
C32 2.2U_NC — C46 .1U_NC — C35 4.7U_NC — R47 0_0603 — +3VRUN_ATVBG — C42 22nF_3P_NC — VSS_TVBG

For Discrete:
Populate R34
De-populate
L26,C335,C40,C346,C350,C32,C46,C35

+1.5V_RUN — R254 0_NC — R235 0_0805 — C344 .1U_NC — C334 .022U_NC — +1.5V_RUN_TVDAC
L2 BLM18PG181SN1 — +1.5V_RUN_QTVDAC
C41 22U/4V/0805 — C48 .1U/16V/0402 — C45 .022U_NC

Place C334,C344 close to
U8.D21 less than 250mils.

Place C45,C48 close to
U8.H19 less than 250mils.

For Discrete:
Populate R254, C41
De-populate
R254,C344,C334,C45

+1.05V_VCCP — D22 1SS355 — R435 10_0402 — +2.5V_RUN
+1.5V_RUN — D23 1SS355 — R436 10_0402 — +3.3V_RUN

U8H

	H22	VCCSYNC
	C30	VCC_TXLVDS0
	B30	VCC_TXLVDS1
	A30	VCC_TXLVDS2
+1.5VRUN_PCIE	AJ41	VCC3G0
	AB41	VCC3G1
	Y41	VCC3G2
	V41	VCC3G3
	R41	VCC3G4
	N41	VCC3G5
	L41	VCC3G6
	AC33	VCCA_3GPLL
	G41	VCCA_3GBG
	H41	VSSA_3GBG
+2.5V_CRTDAC	F21	VCCA_CRTDAC0
	E21	VCCA_CRTDAC1
	G21	VSSA_CRTDAC
+1.5V_RUN_DPLLA	B26	VCCA_DPLLA
+1.5V_RUN_DPLLB	C39	VCCA_DPLLB
+1.5V_RUN_HPLL	AF1	VCCA_HPLL
	A38	VCCA_LVDS
	B39	VSSA_LVDS
+1.5V_RUN_MPLL	AF2	VCCA_MPLL
+3VRUN_ATVBG	H20	VCCA_TVBG
VSS_TVBG	G20	VSSA_TVBG
+3.3V_RUN_TVDACA	E19	VCCA_TVDACA0
	F19	VCCA_TVDACA1
+3.3V_RUN_TVDACB	C20	VCCA_TVDACB0
	D20	VCCA_TVDACB1
+3.3V_RUN_TVDACC	E20	VCCA_TVDACC0
	F20	VCCA_TVDACC1
+1.5V_RUN	AH1	VCCD_HMPLL0
	AH2	VCCD_HMPLL1
	A28	VCCD_LVDS0
	B28	VCCD_LVDS1
	C28	VCCD_LVDS2
+1.5V_RUN_TVDAC	D21	VCCD_TVDAC
	A23	VCC_HV0
	B23	VCC_HV1
	B25	VCC_HV2
+1.5V_RUN_QTVDAC	H19	VCCD_QTVDAC
	AK31	VCCAUX0
	AF31	VCCAUX1
	AE31	VCCAUX2
	AC31	VCCAUX3
	AL30	VCCAUX4
	AK30	VCCAUX5
	AJ30	VCCAUX6
	AH30	VCCAUX7
	AG30	VCCAUX8
	AE30	VCCAUX9
	AE30	VCCAUX10
	AD30	VCCAUX11
	AC30	VCCAUX12
	AG29	VCCAUX13
	AF29	VCCAUX14
	AE29	VCCAUX15
	AD29	VCCAUX16
	AC29	VCCAUX17
	AG28	VCCAUX18
	AF28	VCCAUX19
	AE28	VCCAUX20
	AH22	VCCAUX21
	AJ21	VCCAUX22
	AH21	VCCAUX23
	AJ20	VCCAUX24
	AH20	VCCAUX25
	AH19	VCCAUX26
	P19	VCCAUX27
	P16	VCCAUX28
	AH15	VCCAUX29
	P15	VCCAUX30
	AH14	VCCAUX31
	AG14	VCCAUX32
	AF14	VCCAUX33
	AE14	VCCAUX34
	Y14	VCCAUX35
	AE13	VCCAUX36
	AE13	VCCAUX37
	AF12	VCCAUX38
	AE12	VCCAUX39
	AD12	VCCAUX40

Calistoga

POWER

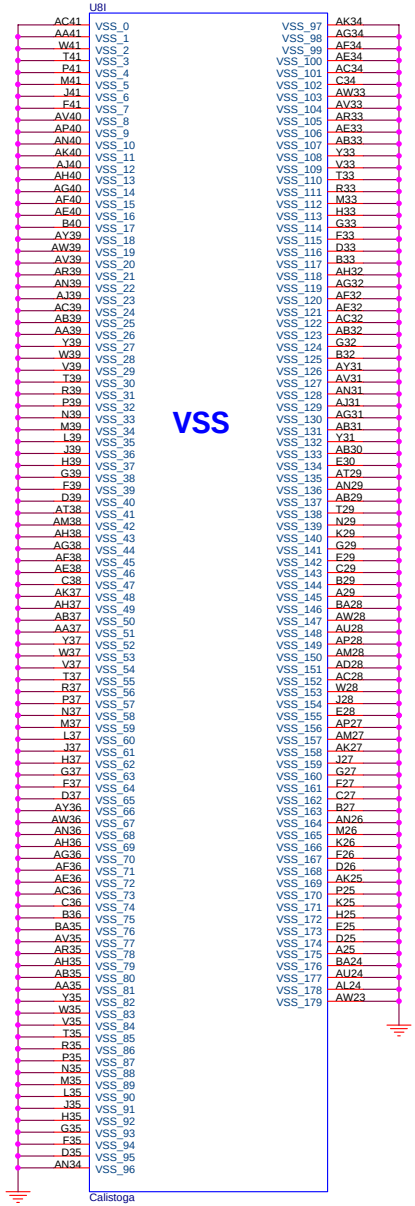
	AC14	VTT_0
	AB14	VTT_1
	W14	VTT_2
	V14	VTT_3
	T14	VTT_4
	R14	VTT_5
	P14	VTT_6
	N14	VTT_7
	M14	VTT_8
	L14	VTT_9
	AD13	VTT_10
	AC13	VTT_11
	AB13	VTT_12
	AA13	VTT_13
	Y13	VTT_14
	W13	VTT_15
	V13	VTT_16
	U13	VTT_17
	T13	VTT_18
	R13	VTT_19
	N13	VTT_20
	M13	VTT_21
	L13	VTT_22
	AB12	VTT_23
	AA12	VTT_24
	Y12	VTT_25
	W12	VTT_26
	V12	VTT_27
	U12	VTT_28
	T12	VTT_29
	R12	VTT_30
	P12	VTT_31
	N12	VTT_32
	M12	VTT_33
	L12	VTT_34
	R11	VTT_35
	P11	VTT_36
	N11	VTT_37
	M11	VTT_38
	R10	VTT_39
	P10	VTT_40
	N10	VTT_41
	M10	VTT_42
	P9	VTT_43
	N9	VTT_44
	M9	VTT_45
	R8	VTT_46
	P8	VTT_47
	N8	VTT_48
	M8	VTT_49
	P7	VTT_50
	N7	VTT_51
	M7	VTT_52
	R6	VTT_53
	P6	VTT_54
	M6	VTT_55
	A6	VTT_56
	R5	VTT_57
	P5	VTT_58
	N5	VTT_59
	M5	VTT_60
	P4	VTT_61
	N4	VTT_62
	M4	VTT_63
	R3	VTT_64
	P3	VTT_65
	N3	VTT_66
	M3	VTT_67
	R2	VTT_68
	P2	VTT_69
	M2	VTT_70
	D2	VTT_71
	AB1	VTT_72
	R1	VTT_73
	P1	VTT_74
	N1	VTT_75
	M1	VTT_76

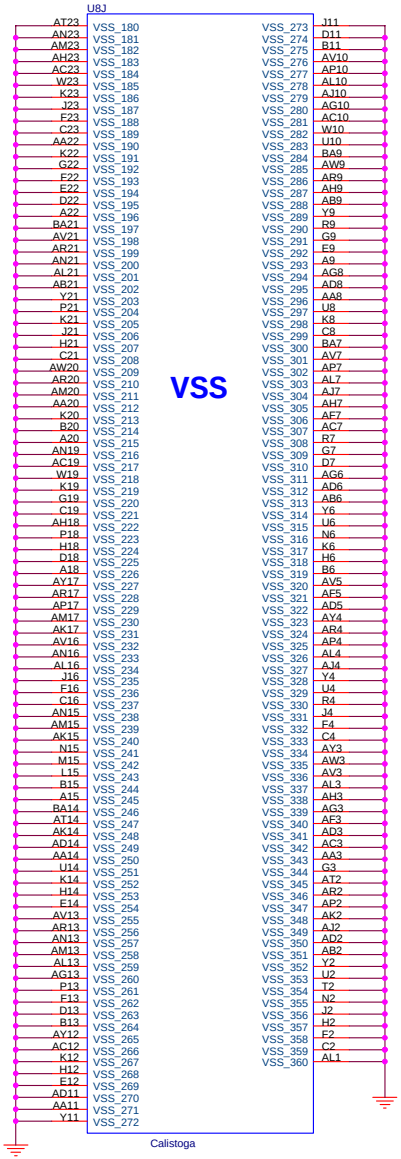
+1.05V_VCCP — C101 330U/2.5V/ESR9
+1.05V_VCCP — C390 2.2U/6.3V/0603 — C418 4.7U/10V/0805 — Place in Cavity.
+1.05V_VCCP — C400 .22U/25V/0603 — Place on the edge.
Place C101 close
to U8.AB13

VTTLF_CAP3 — C44 .47U/10V/0603
VTTLF_CAP2 — C117 .47U/10V/0603
VTTLF_CAP1 — C368 .22U/25V/0603

QUANTA COMPUTER

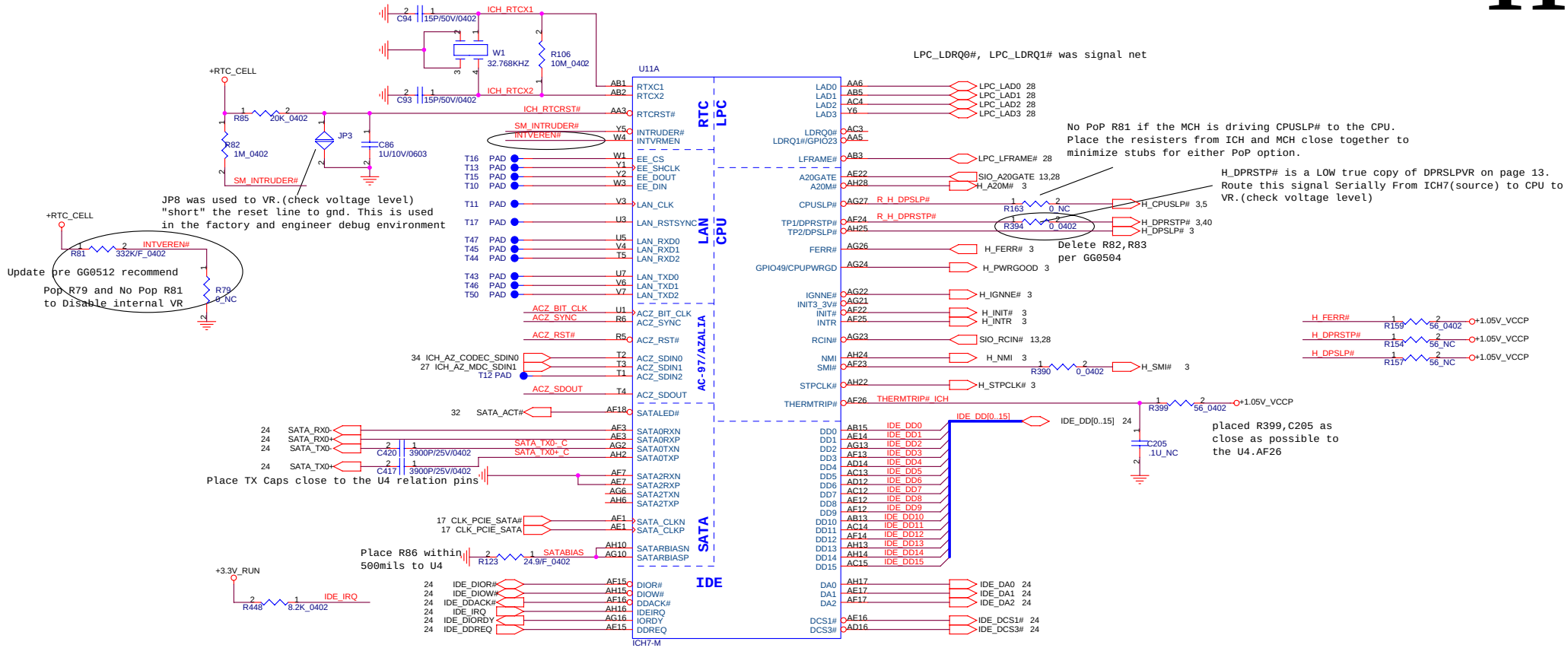
Title	Calistoga (Power)		
Size	Document Number FM1		Rev 1A
Date:	Wednesday, June 29, 2005	Sheet 9 of 48	





QUANTA COMPUTER

Title	Calistoga (VSS,NCTF)	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 10 of 48	

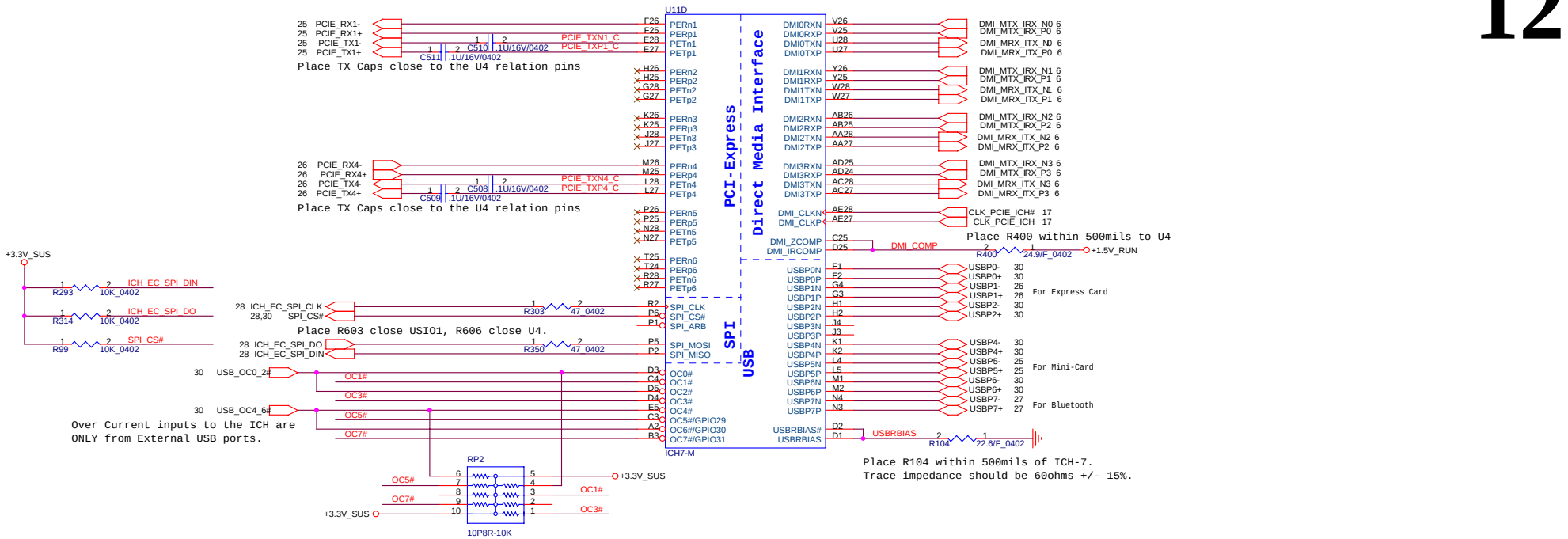


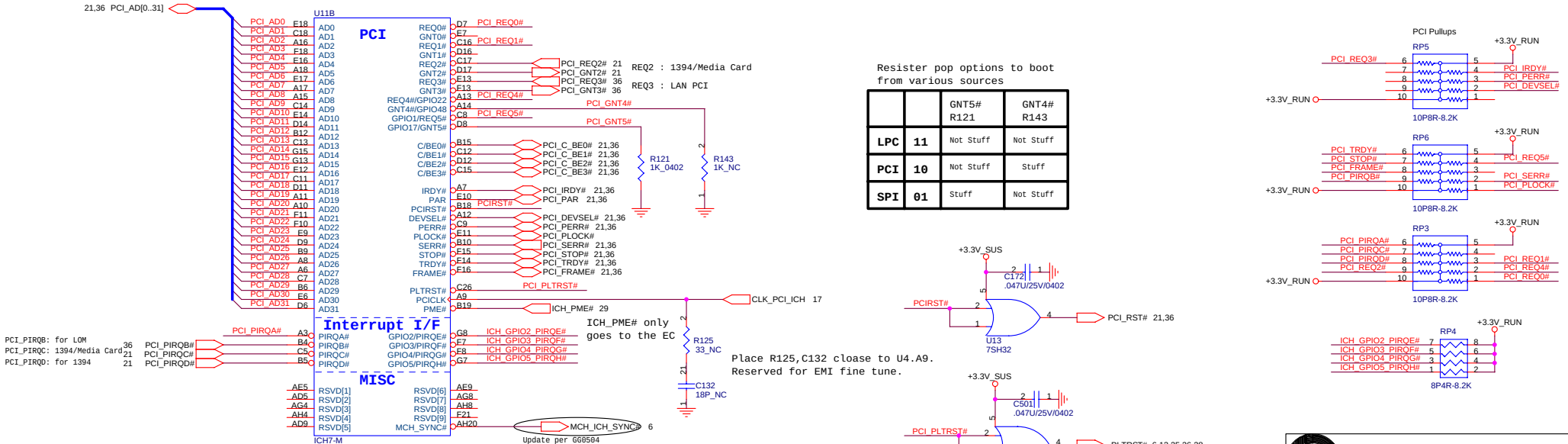
X1,X2 Docking

IAC_SYNC	Port X Line	R126
1	1X2,2X1	STUFF
0	4X1	UNSTUFF

QUANTA COMPUTER

Title	ICH7-M (CPU,IDE,SATA,LPC,AC97)	
Size	Document Number FM1	Rev 1A
Date: Tuesday, July 05, 2005	Sheet 11 of 48	



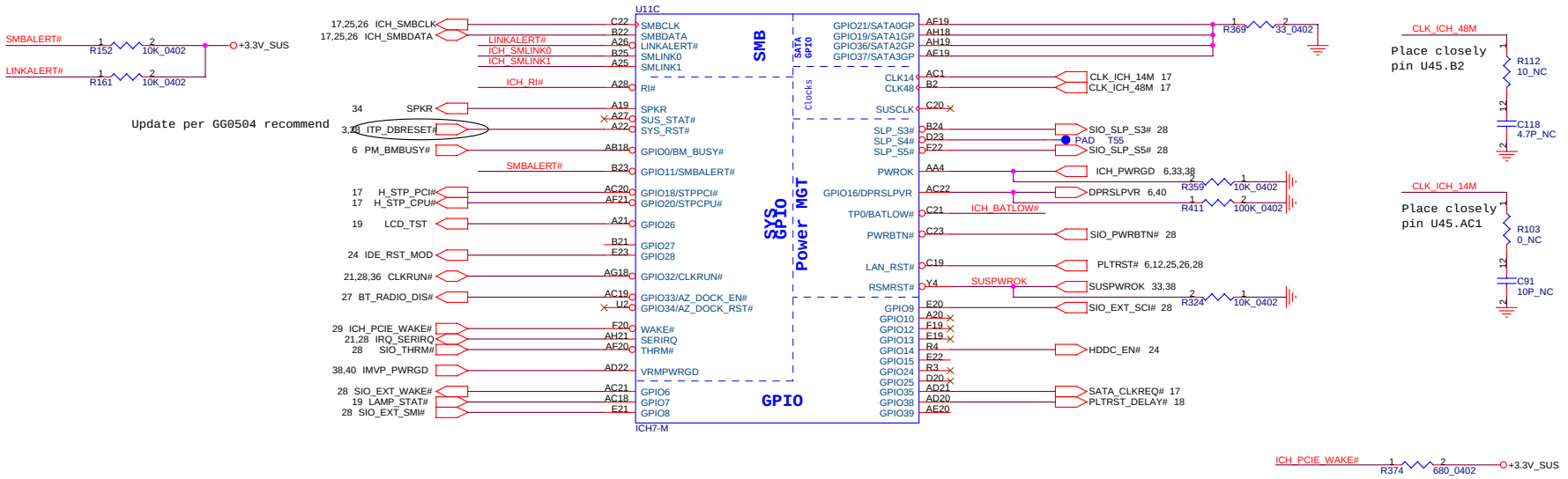


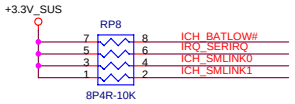
Resister pop options to boot from various sources

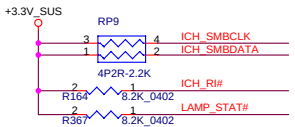
		GNT5# R121	GNT4# R143
LPC	11	Not Stuff	Not Stuff
PCI	10	Not Stuff	Stuff
SPI	01	Stuff	Not Stuff

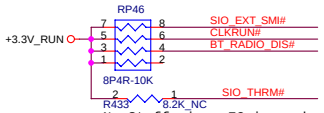
QUANTA COMPUTER

Title	ICH7-M (USB,DMI,PCIE,PCI)		
Size	Document Number FM1		Rev 1A
Date: Tuesday, June 28, 2005	Sheet 12 of 48		

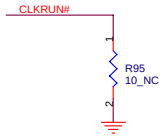




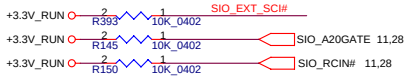




No Stuff since EC is push-pull

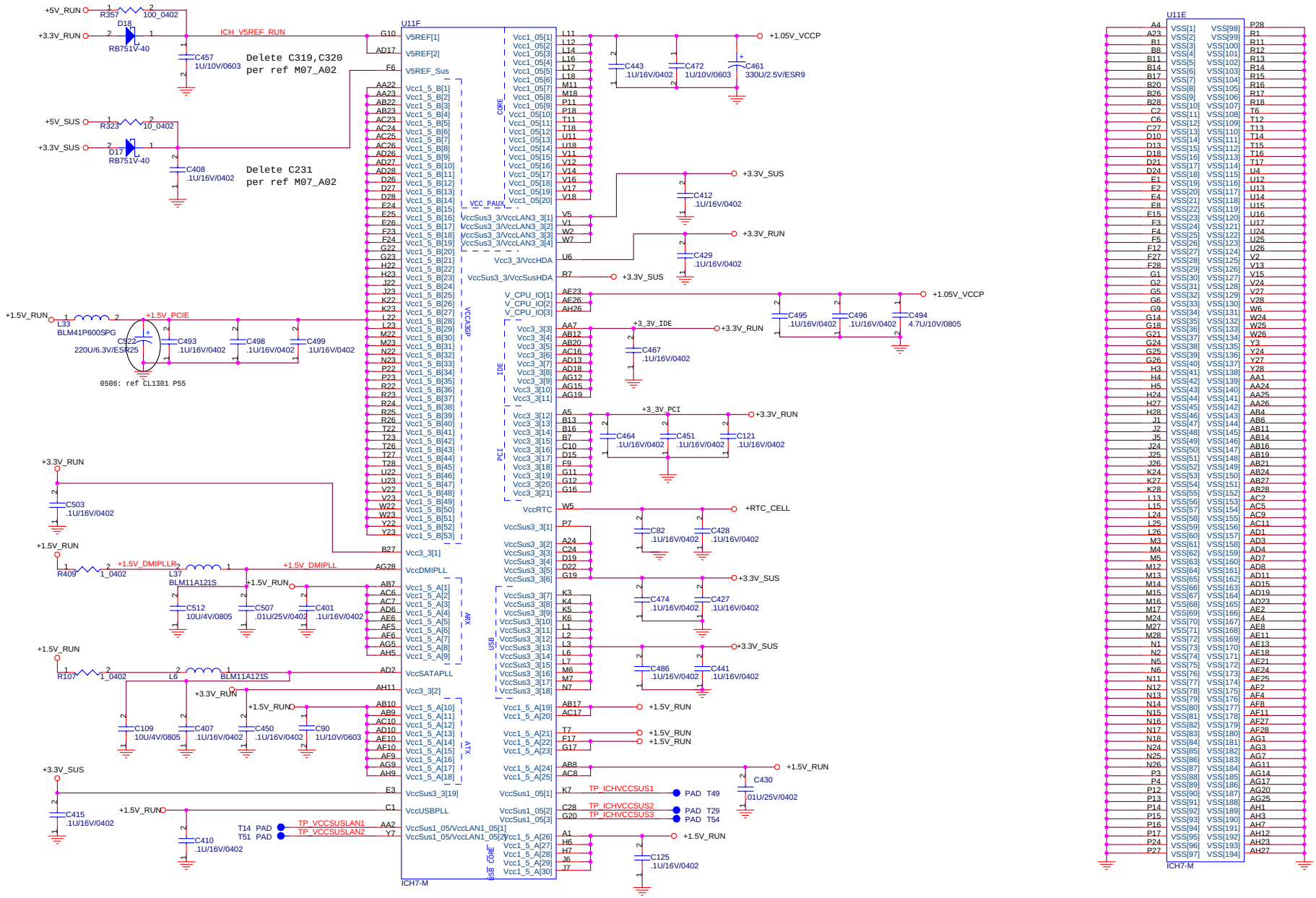


Option to " Disable " clkrun.
Pulling it down will keep the
clks running



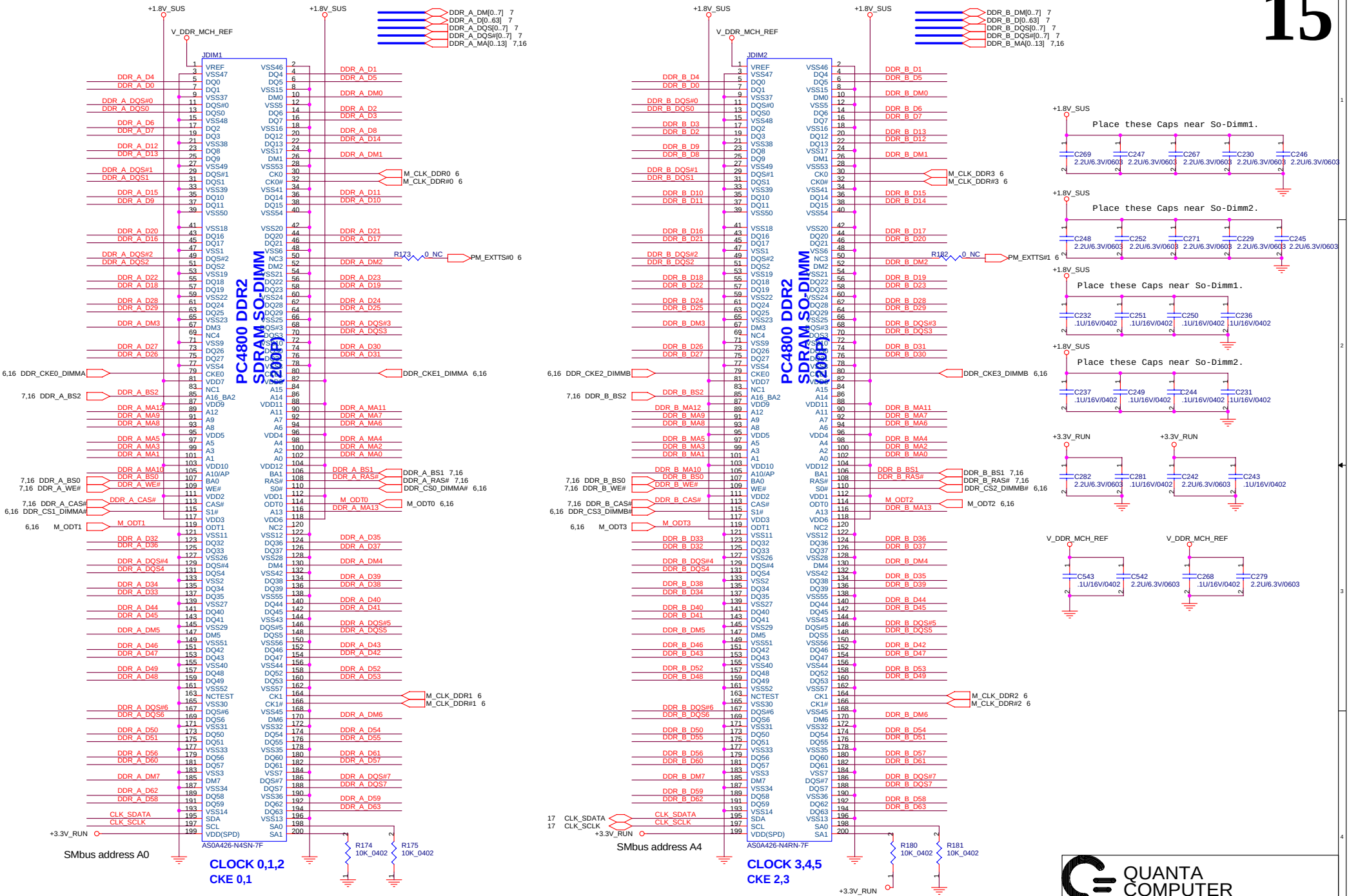
QUANTA COMPUTER

Title	ICH7-M(PM,GPIO,SMB)	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 13 of 48	



QUANTA COMPUTER

Title	ICH7-M (POWER&GND)	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 14 of 48	

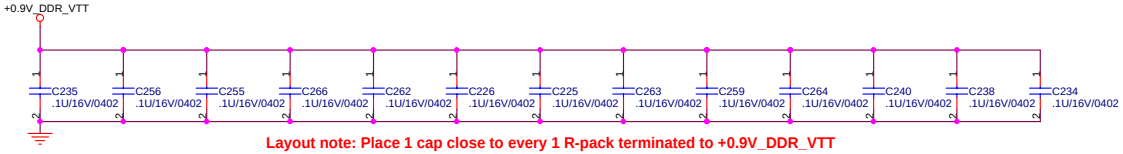


QUANTA COMPUTER

Title	System DRAM Expansion (200P-DDR_SODIMM X 2)	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 15 of 48	

DDR_A_MA[0..13] 7,15

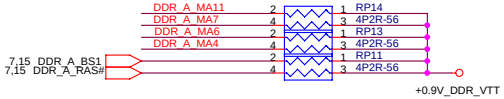
DDR_B_MA[0..13] 7,15

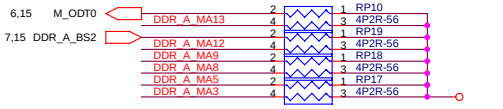


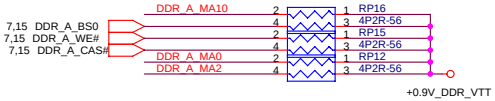
Layout note: Place 1 cap close to every 1 R-pack terminated to +0.9V_DDR_VTT

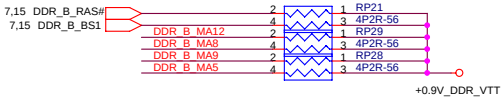
Layout note: Place 1 cap close to every 1 R-pack terminated to +0.9V_DDR_VTT

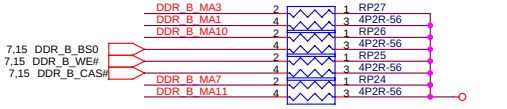
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT

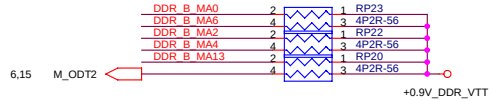


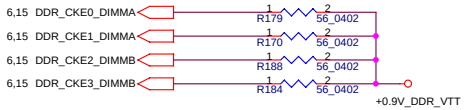


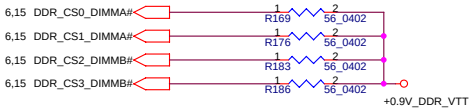


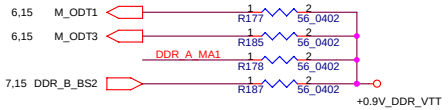












QUANTA COMPUTER

Title	DDR RES.ARRAY		
Size	Document Number FM1		Rev 1A
Date: Tuesday, June 28, 2005	Sheet 16 of 48		

Frequency	BSEL0/FSA	BSEL2/FSC	BSEL1/FSB
100	1	0	1
133	0	0	1
166	0	1	1
200	0	1	0

Place Decoupling as close as possilble to the VDD pins

Place R74,R62,R61 as close as possilble to the VDD pins

Place C74,C75 close to pin7,8.

Place these termination to close CK410M.

Trace length between R277, R278 to UJ42 = <50mils

SMbus address D2

ICS954305D

Pin 43, 44 used for 96Mhz UMA or 27Mhz Disc. Grfx Down on MB

Unused Clock outputs can optionally be connected to Test points

For Discrete:
Populate R274
De-populate R269

PCI_LOM = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0 = UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0

Place pulldown termination close to series R per Design Guide

For Discrete:
De-populate
R285, R288

Place these termination to close CK410M.

These are for backdrive issue

QUANTA COMPUTER

Title: CLOCK GENERATOR

Size: Document Number FM1 — Rev 1A

Date: Tuesday, June 28, 2005 — Sheet 17 of 48

Populate JVDO1 for discrete.

Populate R236 and De-pop R247
for Proto1 build(old VGA card)

SMBUS Address 98

For Discrete:
Populate C60,C68,C65

For Discrete:
Populate C89,C98,C100,C103,C102,C106,C108,C112,
C111,C115,C120,C124,C126,C128,C130,C133,
C138,C140,C142,C144,C145,C148,C151,C152,
C157,C161,C162,C165,C167,C168,C170,C175

For Discrete:
De-populate
R70,R72,R76,R75,R80,R84,R87,R90,R97,R02

Populate R377 and De-populate R386,
R279. for Proto1 build(old VGA card)

For Discrete:
Populate C178,C181

For Discrete:
Populate
C188,C186,C207,C187,C182,U19

For Discrete: Populate TH6,TH15,TH19

TOP Side

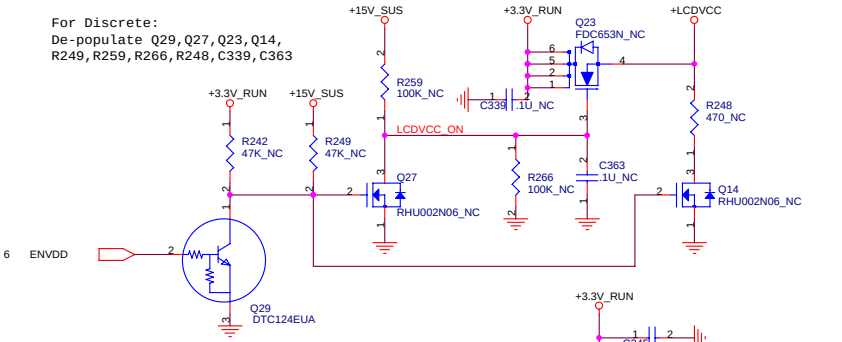
VGACARD STANDOFF

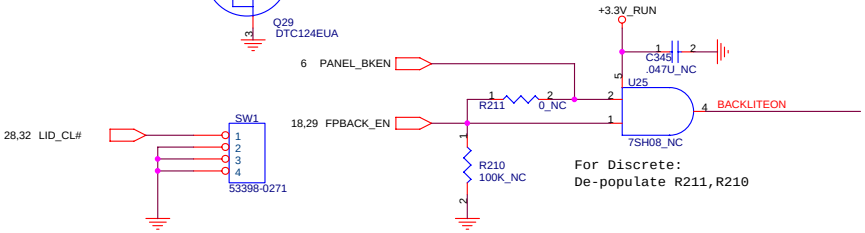
VGA GUIDE POST

HONDA LPF-SC200SMYGA+

Title	DDR RES.ARRAY
Size	Document Number FM1 — Rev 1A
Date:	Tuesday, June 28, 2005 — Sheet 18 of 48

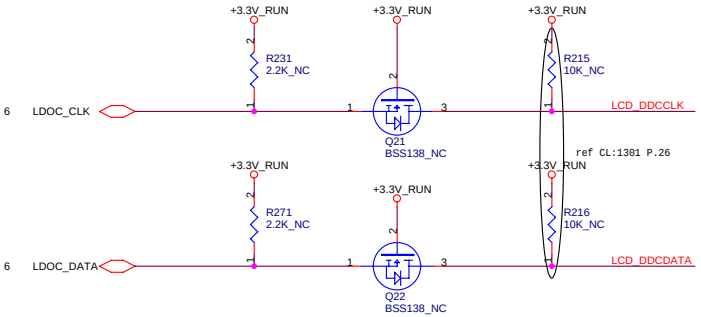
For Discrete:
De-populate Q29,Q27,Q23,Q14,
R249,R259,R266,R248,C339,C363



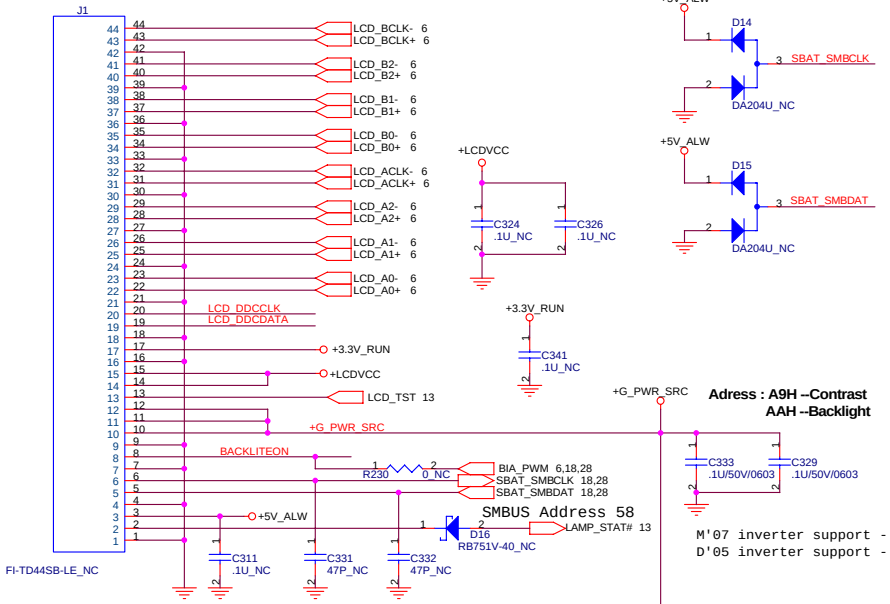


For Discrete:
De-populate R211,R210

Support M07-Inverter: Populate R230,R211 and Depopulate U8,C345.
Support D05-Inverter: Depopulate R230,R211 and Populate U8,C345.



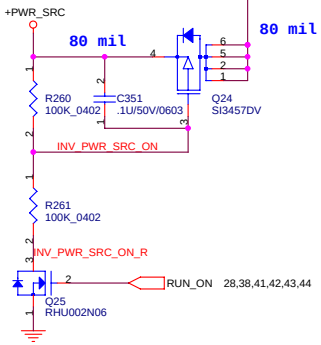
For Discrete:
Depopulate
R231,R271,R215,R216,Q21,Q22



Adress : A9H --Contrast
AAH --Backlight

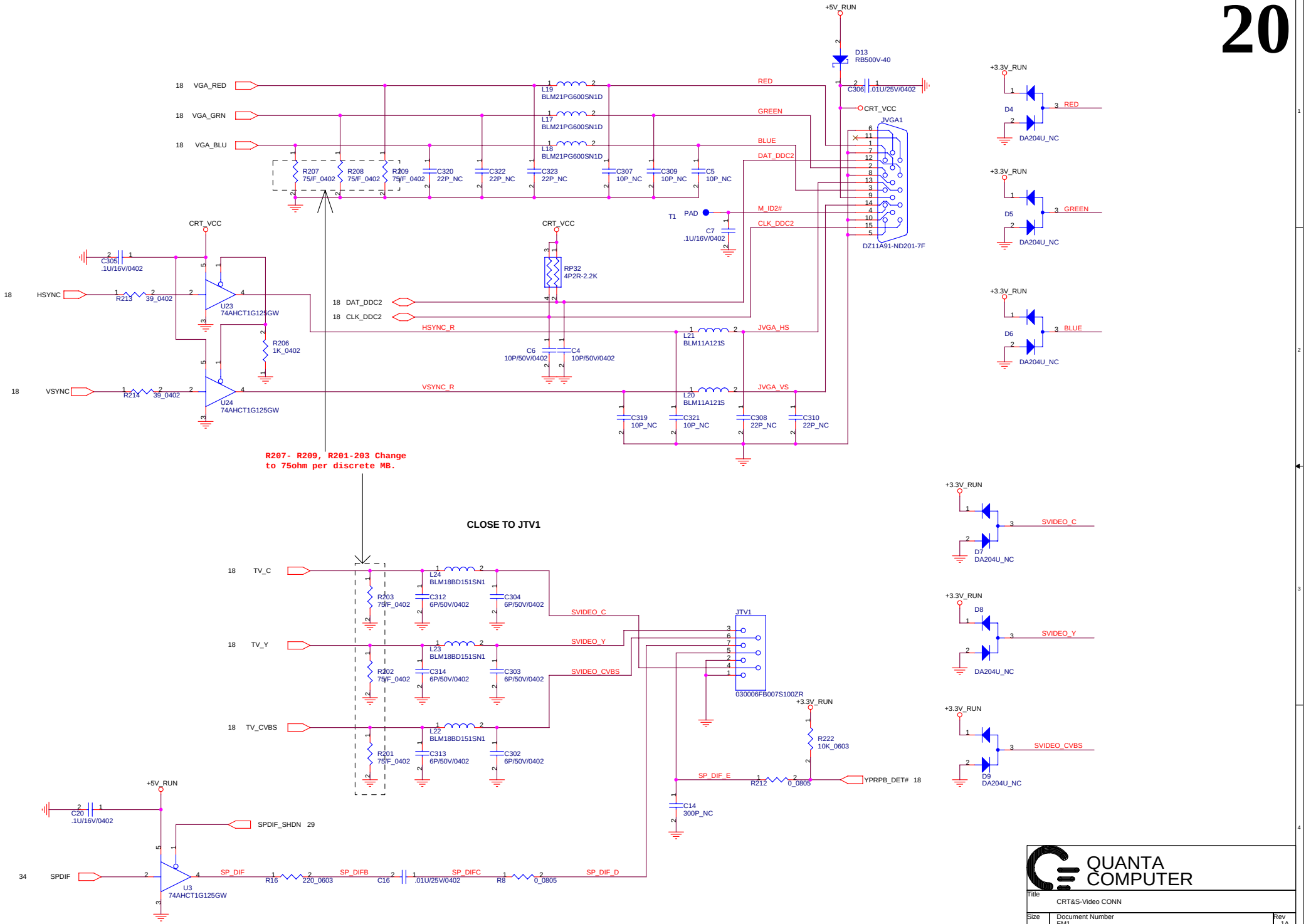
M'07 inverter support - De-populate D16.
D'05 inverter support - Populate D16

For Discrete:
De-populate J1,R230,C311,C331,C332,
D16,C341,C324,C326



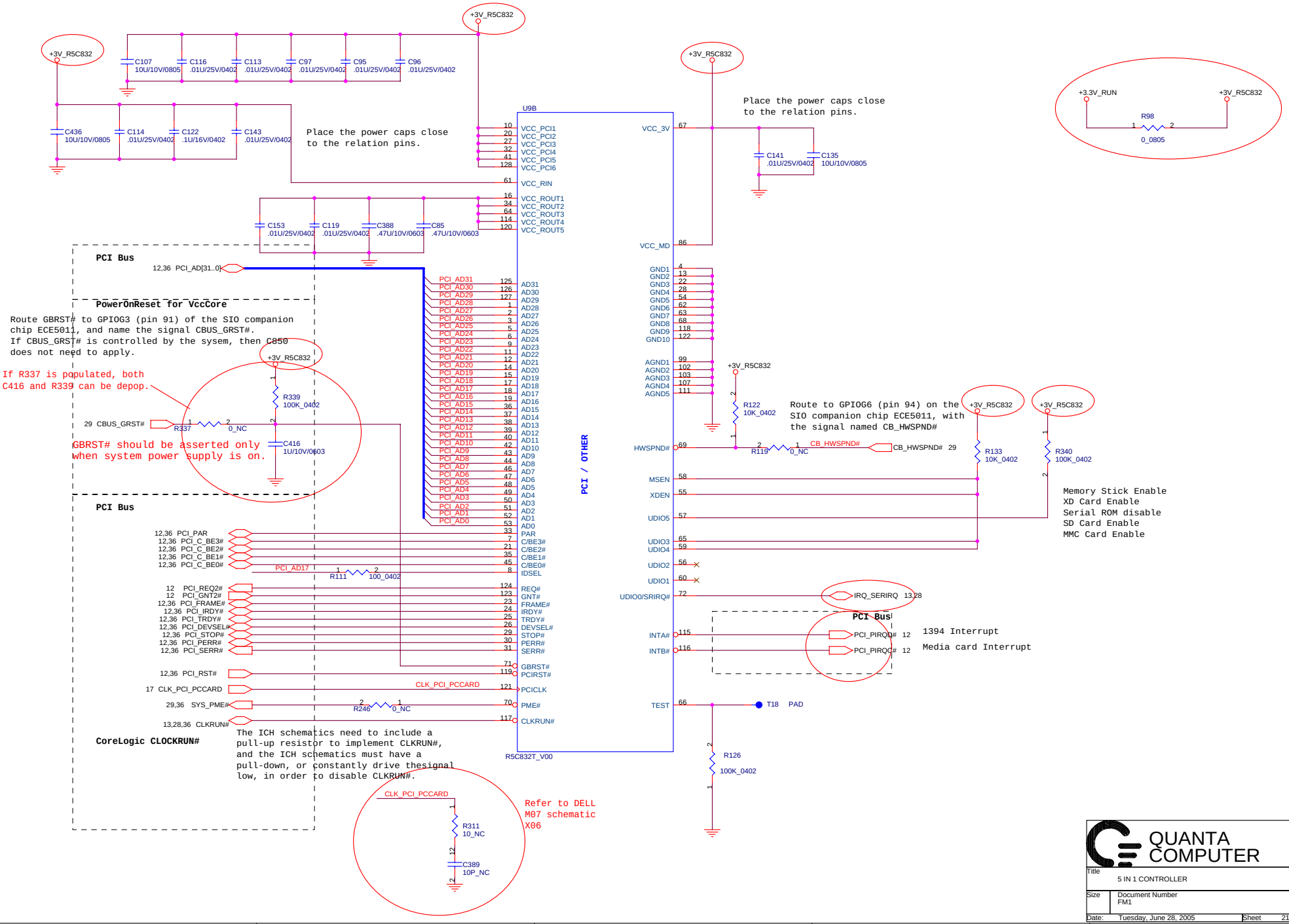
QUANTA COMPUTER

Title	LCD CONN&CK-SSCD		
Size	Document Number FM1		Rev 1A
Date: Tuesday, June 28, 2005	Sheet 19 of 48		



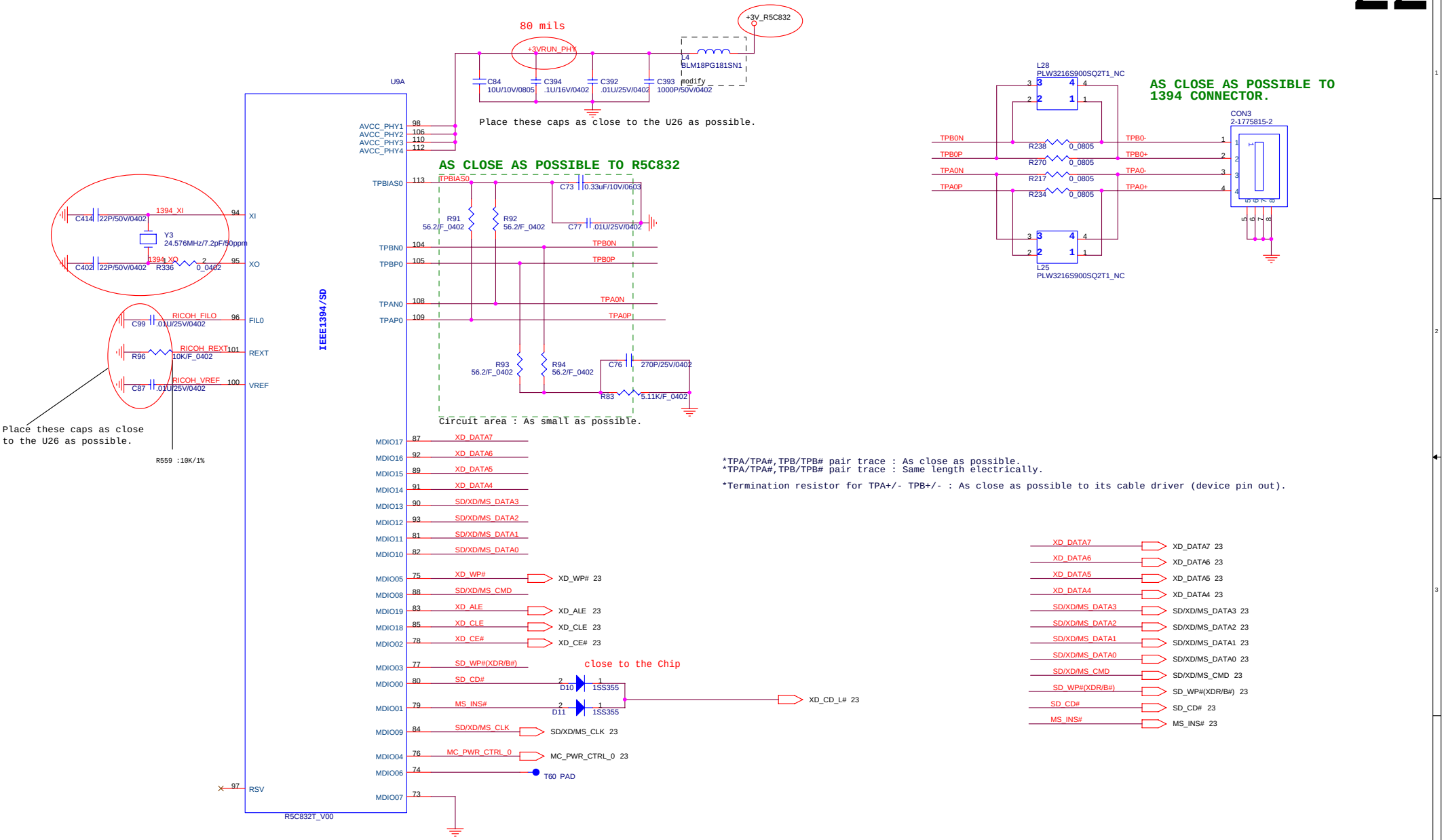
Title	CRT&S-Video CONN
Size	Document Number FM1
Rev	1A
Date:	Tuesday, June 28, 2005
Sheet	20 of 48

QUANTA COMPUTER



QUANTA COMPUTER

Title	5 IN 1 CONTROLLER	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 21 of 48	



QUANTA COMPUTER

Title	IEEE 1394	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 22 of 48	

DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

5 IN1 CARD READER

Accroding to Molex's new pin define, swap Pin1 and Pin2.

Accroding to Molex's new pin define, change this pin from Vcc to Data1.

Need GND Shields to the clock trace.

Refer to M07, connect C160,C163 to +3VRUN_XD.

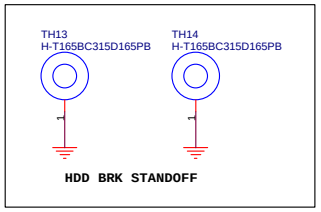
Accroding to RICOH's suggestion, place this resister at trident point of R_SD/XD/MS_CLK trace.

For SD/MS power

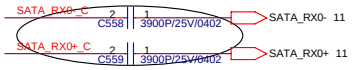
For XD power

QUANTA COMPUTER

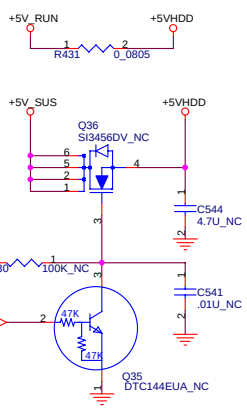
Title	CARD READER CONN
Size	Document Number CM1
Rev	1A
Date:	Tuesday, June 28, 2005
Sheet	23 of 48

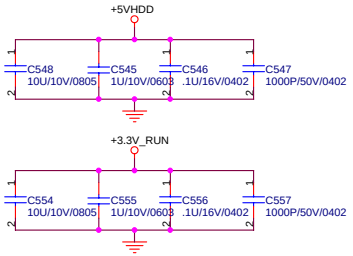


Place close to
connector side

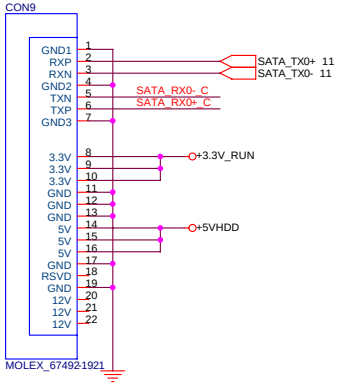


Locate caps C558, C559 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 20mils.



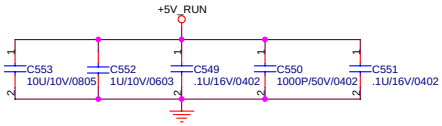


Place closed to
HDD connector

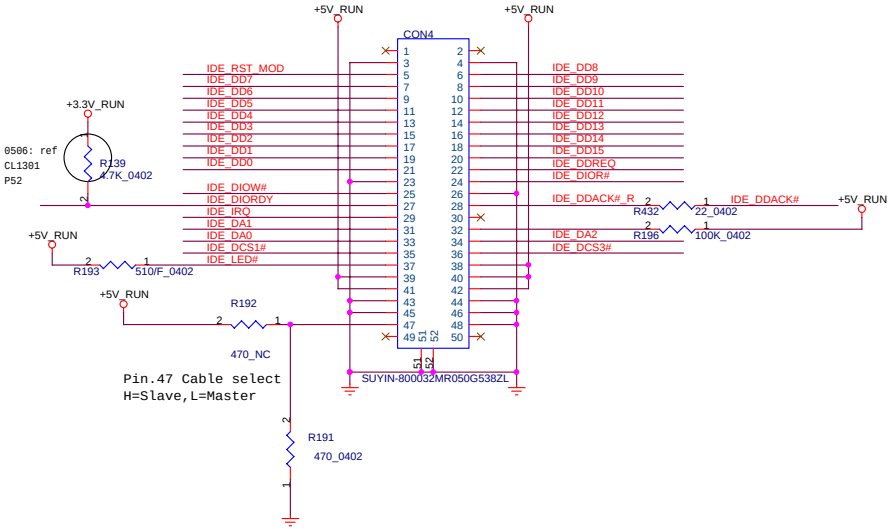


SATA drive vendors will use only 5V
supply from the system and will derive
3.3V on the drive. If drive power
goals are not achieved, drive vendors
will use both 5V and 3.3V supplies
from the system. Initial power saving
using 3.3V from system is less than 5%.

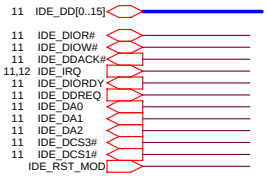
Power Estimate:
SATA drive power consumption estimate at
MobileMark is 1.1W. An additional 150mW
can be saved using Intel's IMST driver.



Place closed to
MOD connector

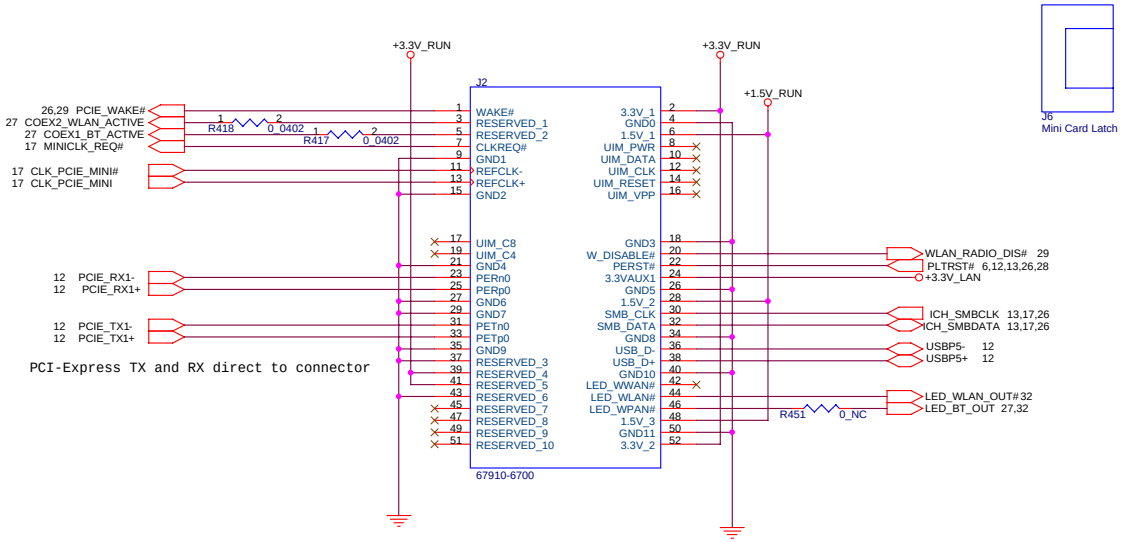


Pin.47 Cable select
H=Slave,L=Master

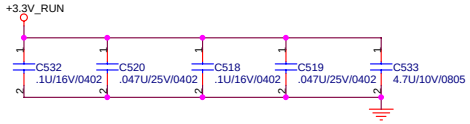


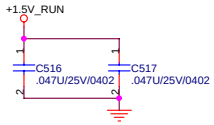
QUANTA COMPUTER

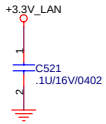
Title	STAT HDD & PATA ODD	
Size	Document Number FM1	Rev 1A
Date: Tuesday, July 05, 2005	Sheet 24 of 48	



PCI-Express TX and RX direct to connector

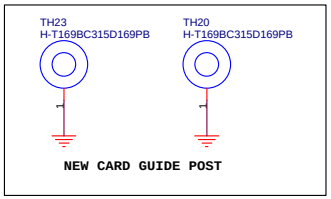


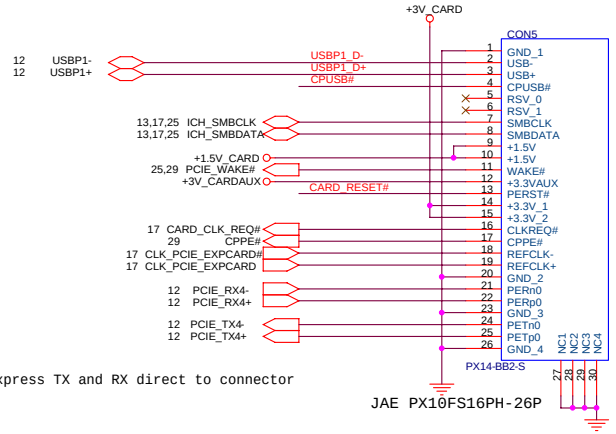




QUANTA COMPUTER

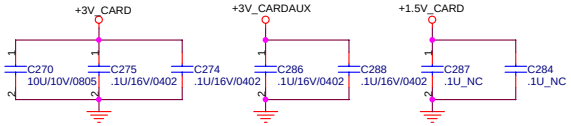
Title	Minicard	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 25 of 48	

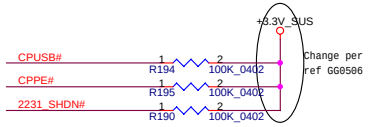




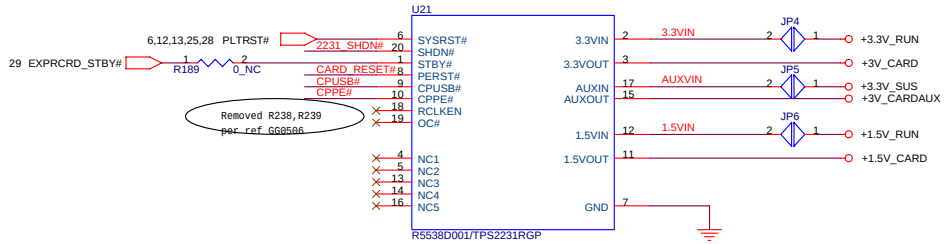
PCI-Express TX and RX direct to connector

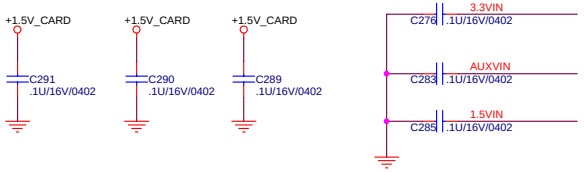
JAE PX10FS16PH-26P





+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA



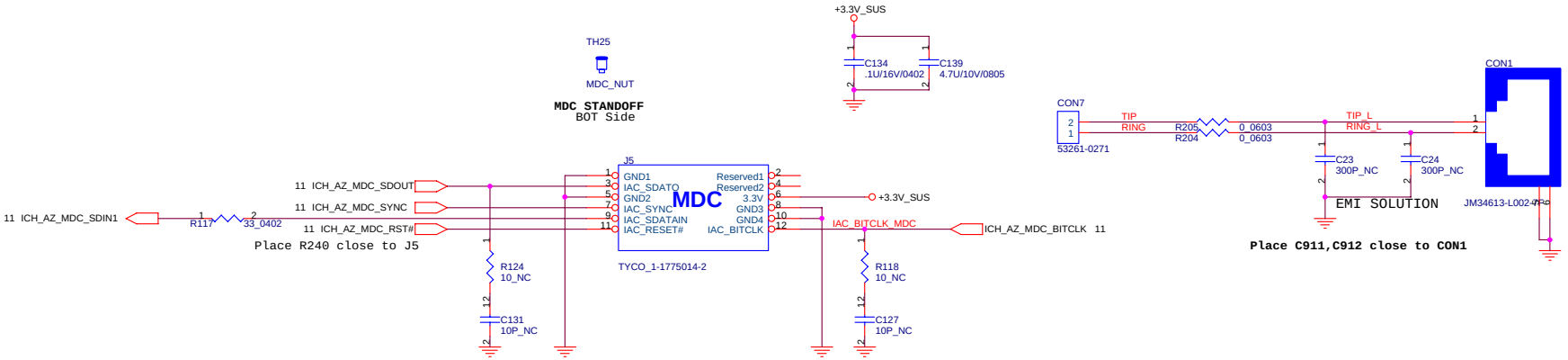


QUANTA COMPUTER

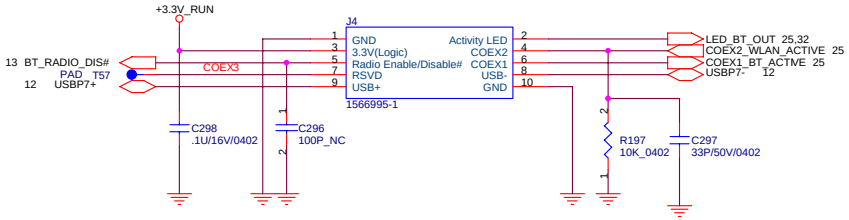
Title	Express Card	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 26 of 48	

MDC Layout Notes

1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG
(stranded or twisted pair wire)

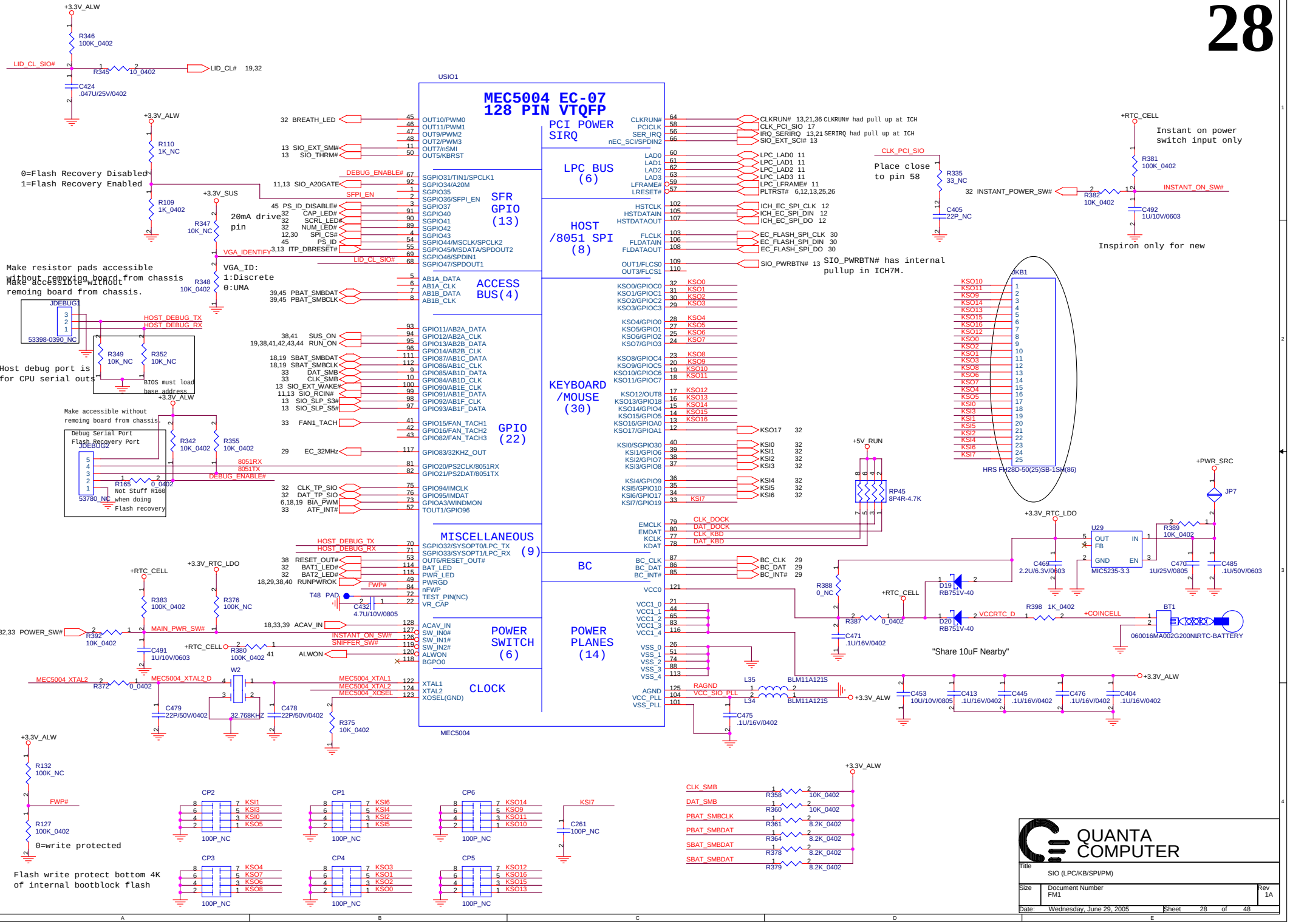


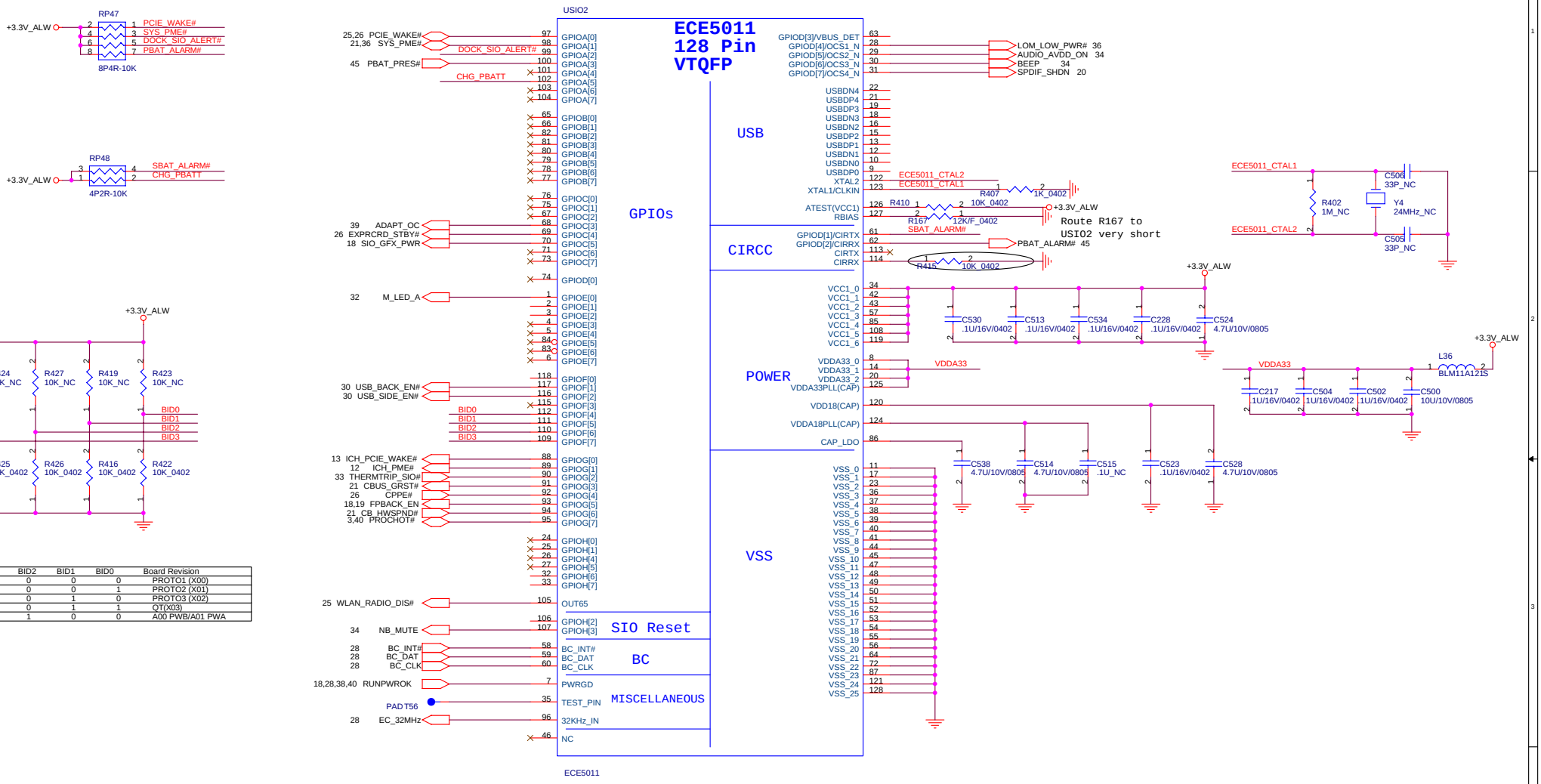
Bluetooth



QUANTA COMPUTER

Title	MDC CONN & BlueTooth.	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 27 of 48	


MEC5004 EC-07
128 PIN VTQFP
USIO1
PCI POWER SIRQ
LPC BUS (6)
SFR GPIO (13)
HOST /8051 SPI (8)
ACCESS BUS(4)
KEYBOARD /MOUSE (30)
GPIO (22)
MISCELLANEOUS (9)
BC
POWER SWITCH (6)
POWER PLANES (14)
CLOCK
MEC5004
0=Flash Recovery Disabled
1=Flash Recovery Enabled
20mA drive pin
VGA_ID:
1:Discrete
0:UMA
Make resistor pads accessible without removing board from chassis
Make accessible without remoing board from chassis.
Host debug port is for CPU serial outs
BIOS must load base address
Make accessible without remoing board from chassis.
Debug Serial Port
Flash Recovery Port
Not Stuff R160 when doing Flash recovery
Place close to pin 58
Instant on power switch input only
Inspiron only for new
SIO_PWRBTN# has internal pullup in ICH7M.
"Share 10uF Nearby"
0=write protected
Flash write protect bottom 4K of internal bootblock flash
HRS FH28D-50(25)SB-1SH(86)
060016MA002G200NIRTC-BATTERY
QUANTA COMPUTER
SIO (LPC/KB/SPI/PM)
Wednesday, June 29, 2005



BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	PROTO1 (X00)
0	0	0	1	PROTO2 (X01)
0	0	1	0	PROTO3 (X02)
0	0	1	1	QT(X03)
0	1	0	0	A00 PWB/A01 PWA

QUANTA COMPUTER

Title	SIO (GPIO/BC/USB/CIRR)	
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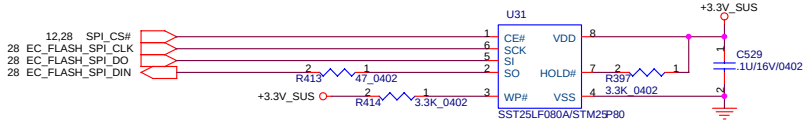
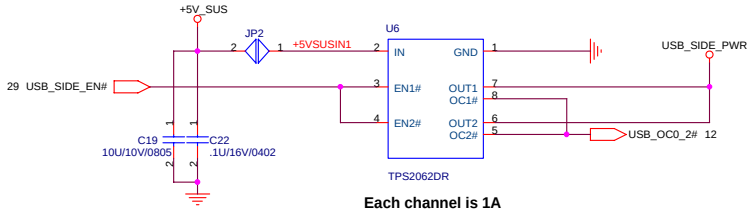
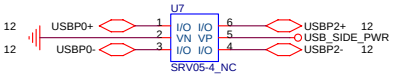
8Mbit (1M Byte), SPI



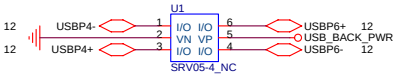
Delete UPW1, C434-436, RP53 per GG0524 item 135.

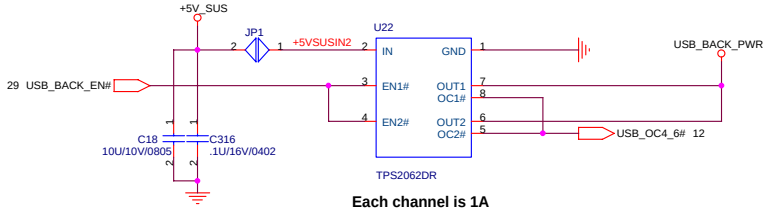


Each channel is 1A

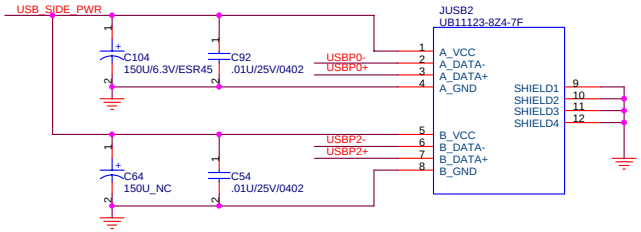


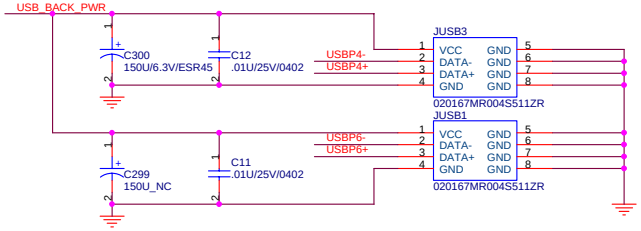
Place ESD diodes as close as USB connector.





Each channel is 1A





QUANTA COMPUTER

Title	USB & Flash	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 30 of 48	

TH10 H-C197D63P2
TH9 H-C197D63P2
TH11 H-C197D63P2
TH17 H-C197D63P2
TH2 H-C197D63P2
TH7 H-C197D63P2
TH5 H-C197D63P2
TH3 H-C197D63P2
TH12 H-C197D63P2

TH4 H-C197D63P2
TH16 H-C110D110N
TH8 H-C197D63P2
TH22 H-C110D110N
TH1 H-C197D63P2
TH18 H-C197D63P2
TH21 H-C197D63P2
TH24 H-C197D63P2

PV4 PAD138X98
PV10 PAD138X98
PV9 PAD138X98
PV8 PAD138X98
PV2 PAD138X98
PV7 PAD138X98
PV5 PAD138X98
PV3 PAD138X98
PV1 PAD138X98
PV6 PAD138X98

DC_IN+
C578 .1U_NC

+PWR_SRC C587 .1U_NC +5V_SUS
+PWR_SRC C588 .1U_NC +5V_SUS
+PWR_SRC C589 .1U_NC +5V_SUS
+PWR_SRC C590 .1U_NC +5V_SUS

+3.3V_RUN C593 .1U_NC +1.5V_RUN
+3.3V_RUN C599 .1U_NC +1.5V_RUN

+PWR_SRC C620 .1U_NC +3.3V_RUN

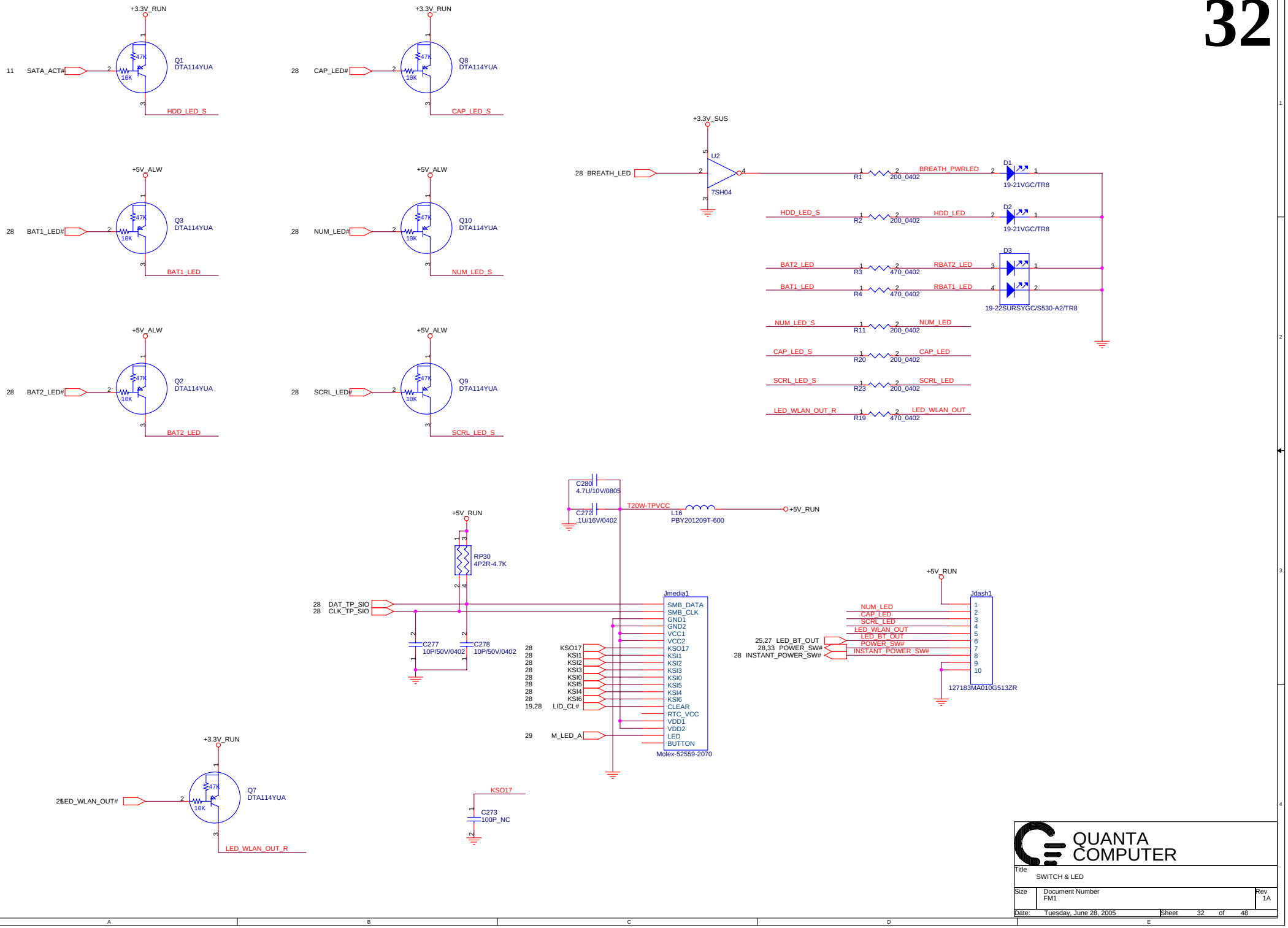
+3.3V_RUN C612 .1U_NC +5V_SUS
+3.3V_RUN C614 .1U_NC +5V_SUS

+PWR_SRC C632 .1U_NC
+PWR_SRC C633 .1U_NC

+3.3V_SUS C639 .1U_NC +5V_SUS

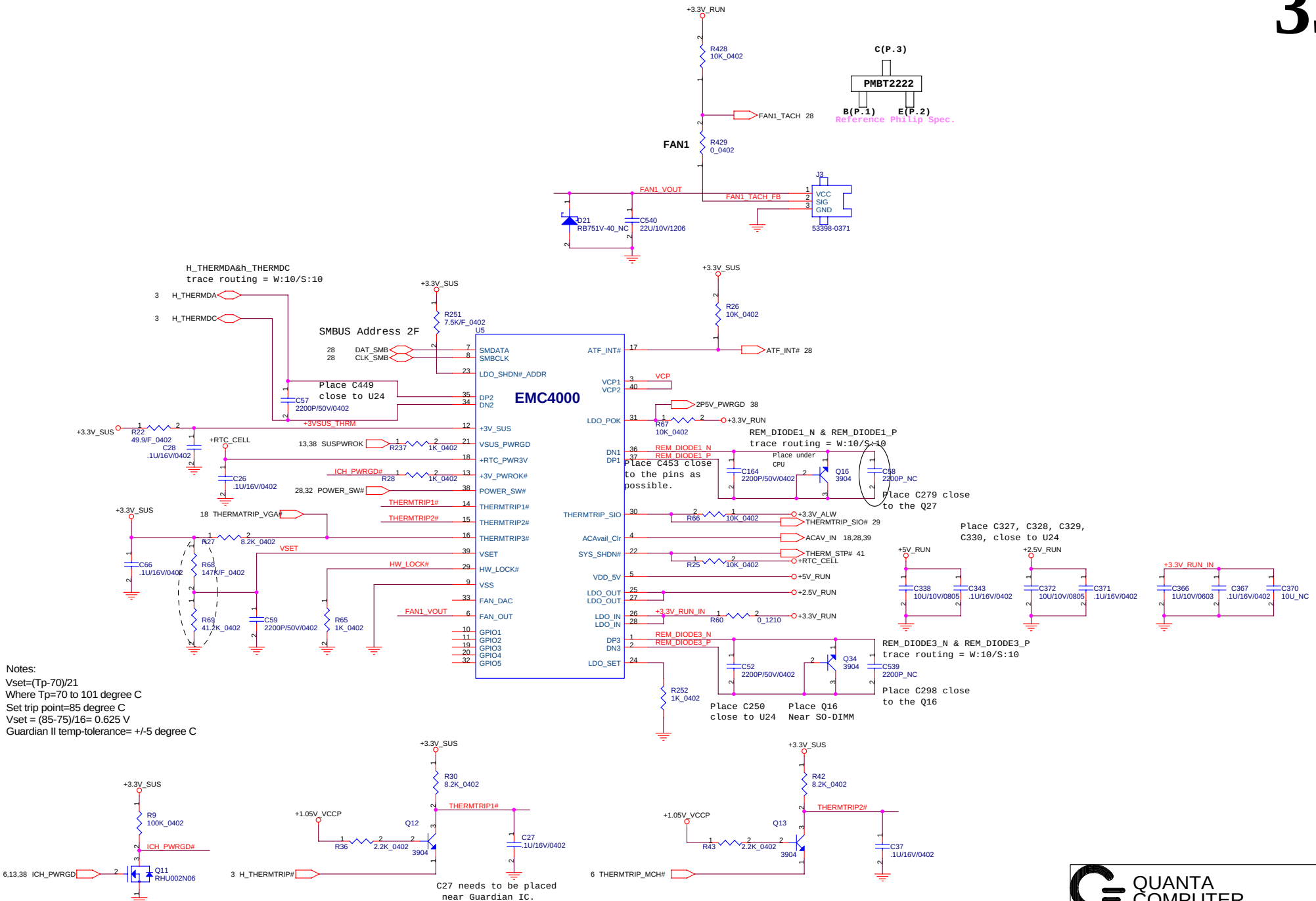
QUANTA COMPUTER

Title	EMI & Screw hole	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 31 of 48	



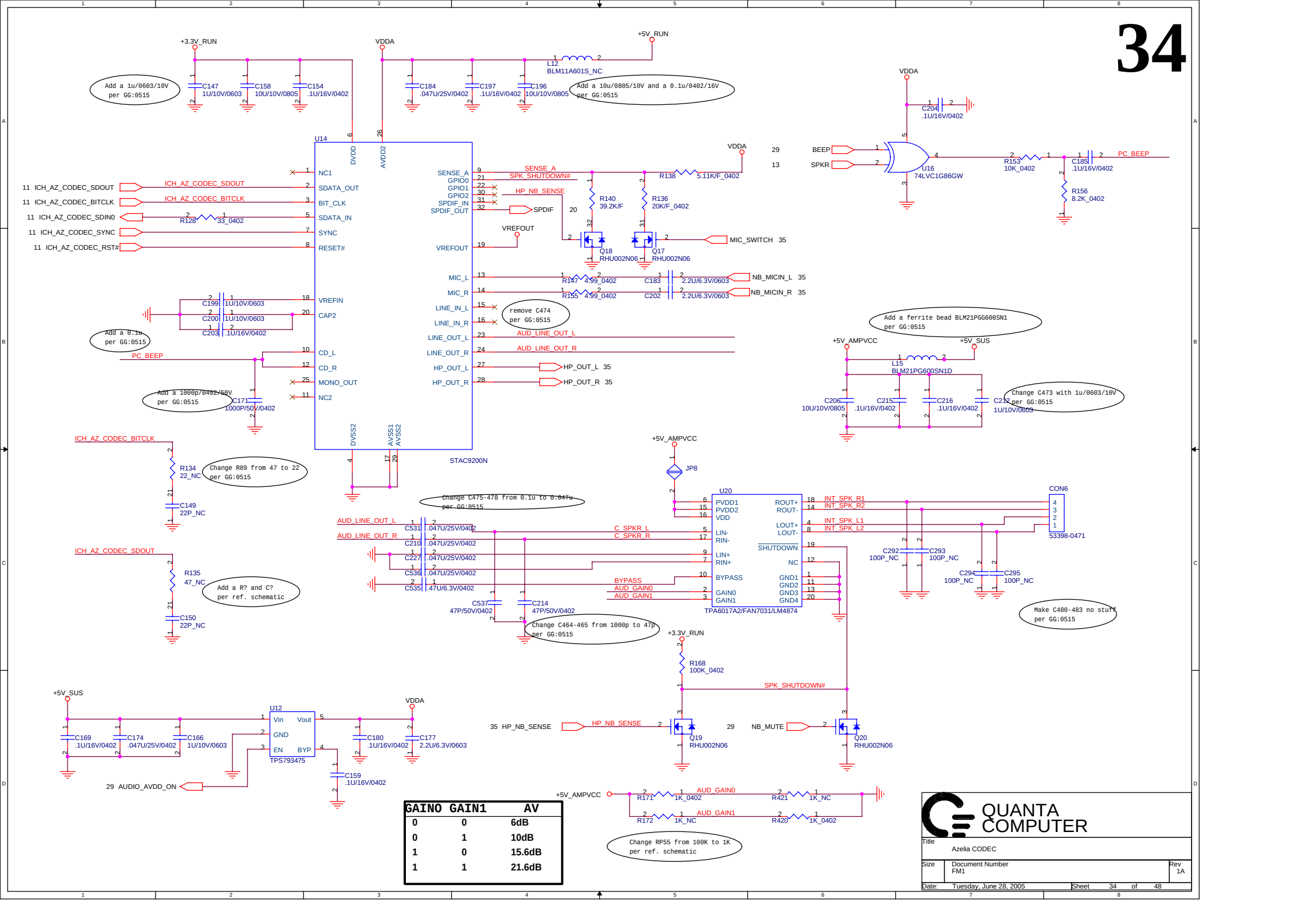
QUANTA COMPUTER

Title	SWITCH & LED	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 32 of 48	



QUANTA COMPUTER

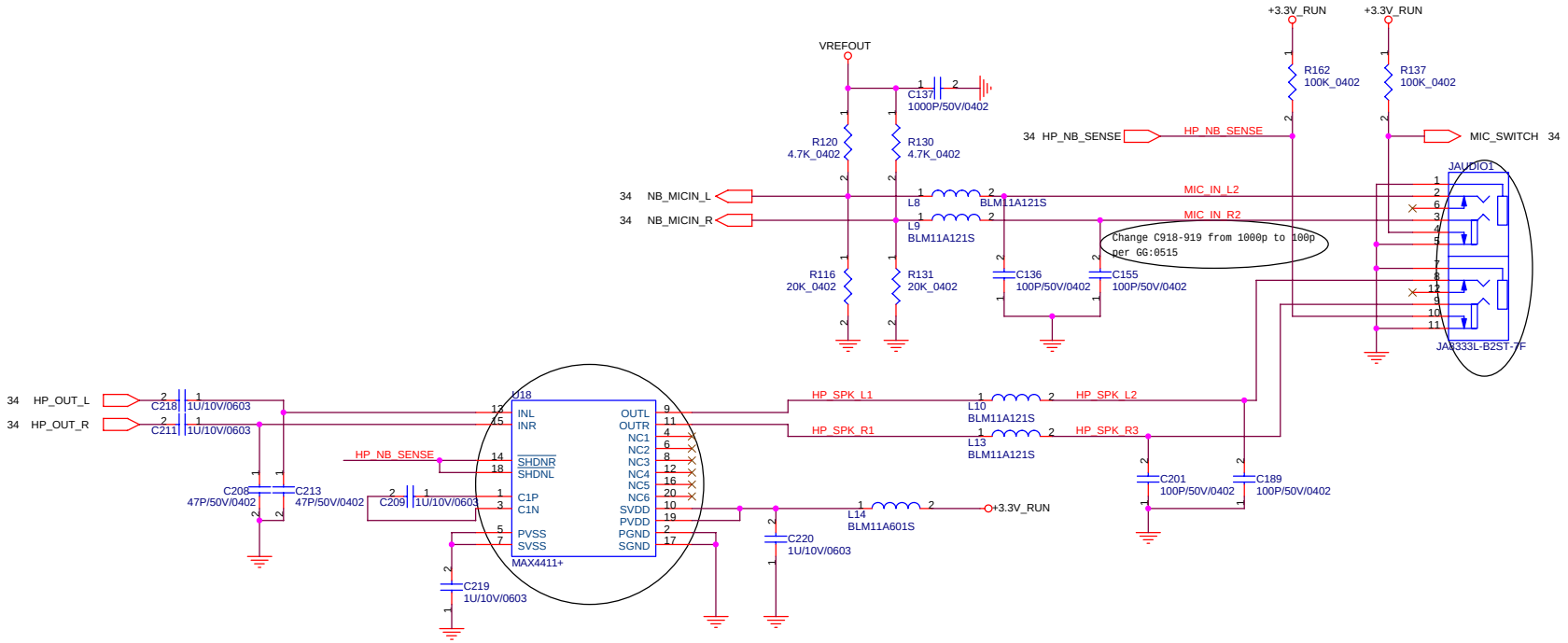
Title	FAN & THERMAL	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 33 of 48	



GAINO	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

QUANTA COMPUTER

Title	Azelia CODEC	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 34 of 48	



QUANTA COMPUTER

Title	AUDIO CONN	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 35 of 48	

Refer to M07_LOM4401_X06 schematic.
'+3VLAN should be sourced from +3VSUS instead of +3VSRC since WOL is not supported on Key Largo.

+3.3V_LAN
C50 4.7U/10V/0805
C17 4.7U/10V/0805
C336 .1U/16V/0402
C359 .1U/16V/0402
C1 .1U/16V/0402
C358 .1U/16V/0402
C33 .1U/16V/0402
C365 .1U/16V/0402
C30 .1U/16V/0402
C318 .1U/16V/0402
C49 .1U/16V/0402
C3 .1U/16V/0402
C361 .1U/16V/0402
C317 1000P/50V/0402
+1.8V_LOM
C25 .1U/16V/0402
C10 .1U/16V/0402
C47 .1U/16V/0402
C360 .1U/16V/0402
C301 4.7U/10V/0805
Refer to M07_LOM4401_X06 schematic.
Refer to M07_LOM4401_X06 schematic.
Close to power pins
0.1U*12 pcs
Place C874 close to pin65
+3.3V_SUS
+3.3V_LAN
R59 0_0805

These three pin LINK_LED10#, LINK_LED100#, ACT_LED are open-drain type.

Place L46, C717, C718 close to pin64.

Place R673, C610, C611 close to pin69

U4 BCM4401

12,21 PCI_AD[31..0]
PCI_AD31 122
PCI_AD30 123
PCI_AD29 124
PCI_AD28 126
PCI_AD27 127
PCI_AD26 128
PCI_AD25 1
PCI_AD24 3
PCI_AD23 6
PCI_AD22 8
PCI_AD21 9
PCI_AD20 10
PCI_AD19 11
PCI_AD18 14
PCI_AD17 15
PCI_AD16 16
PCI_AD15 33
PCI_AD14 34
PCI_AD13 36
PCI_AD12 37
PCI_AD11 38
PCI_AD10 39
PCI_AD9 41
PCI_AD8 42
PCI_AD7 45
PCI_AD6 48
PCI_AD5 49
PCI_AD4 50
PCI_AD3 51
PCI_AD2 53
PCI_AD1 54
PCI_AD0 55

12,21 PCI_C_BE3# 4
12,21 PCI_C_BE2# 18
12,21 PCI_C_BE1# 32
12,21 PCI_C_BE0# 43
12,21 PCI_FRAME# 20
12,21 PCI_IRDY# 21
12,21 PCI_TRDY# 23
12,21 PCI_DEVSEL# 26
12,21 PCI_STOP# 27
12,21 PCI_PERR# 28
12,21 PCI_SERR# 29
12,21 PCI_PAR 31
12 PCI_PIRQB# 116
PCI_INT_L

12,21 PCI_RST# 117
PCI_RST_L
PCI_CLK
12 PCI_GNT3# 119
12 PCI_REQ3# 121
21,29 SYS_PME# 113
PCI_PME_L
PCI_IDSEL 5
PCI_CLKRUN_L 22

17 CLK_PCI_LOM
R40 33_NC
Place R444, C619 close to U148.118
C39 22P_NC
13,21,28 CLKRUN#
R268 100_0402
Refer to M07_LOM4401_X06 schematic. R489 and R490 removed from schematic because of Bios can configure the state of CLKRUN# signal.

XTAL_IN 67
XTAL_OUT 66
R7 800_0402
Y1 25MHz/20pF/50ppm
C8 27P/50V/0402
C9 27P/50V/0402

LINK_LED10# 75
LINK_LED100# 76
ACT_LED# 77
COL_LED# 78
T31
LINK_LED10# 37
LINK_LED100# 37
ACTLED# 37

EPHY_BIAS_AVDD 69
+3.3V_LAN_BIAS_AVDD
EPHY_AVDD 57
EPHY_PLLVDD 64
+1.8V_LOM_PLLVDD
L1 BLM11A601S
C13 1000P/50V/0402
C315 2.2U/6.3V/0603
C330 .1U/16V/0402
Delete L47 per 4401 ref schematic
Place R440 close to U148
EPHY_VREF 71
RDAC 72
EPHY_TESTMODE 88
R218 1.27K/F_0402

EPHY_TDP 62
EPHY_TDN 61
EPHY_RDP 59
EPHY_RDN 60
LOM_TX+ 37
LOM_TX- 37
LOM_RX+ 37
LOM_RX- 37

NC 104
NC 105
NC 103
NC 108
NC 102
NC 109
NC 110
NC 107
R21 49.9/F_0402
R24 49.9/F_0402
R15 49.9/F_0402
R12 49.9/F_0402
C21 .1U/16V/0402
C15 .1U/16V/0402

Resistors must be rated at least 1/16W. Place termination close to connector the chip 4401.

GPIO2/VAUXAVAIL 87
GPIO1 86
GPIO0 85
R5 1K_0402
T33
T34
Delete R638&R631 per 4401 ref schematic

BOOTROM_SCL 90
BOOTROM_SDA 93
T30
T32

SPROM_CS 98
SPROM_CLK 95
SPROM_DOUT 101
SPROM_DIN 99
U26
M93C46-WDW6T
C342 .1U/16V/0402

EXT_POR_L 89
LOM_LOW_PWR# 29
Note: EXT_POR_L has a interal pull up.

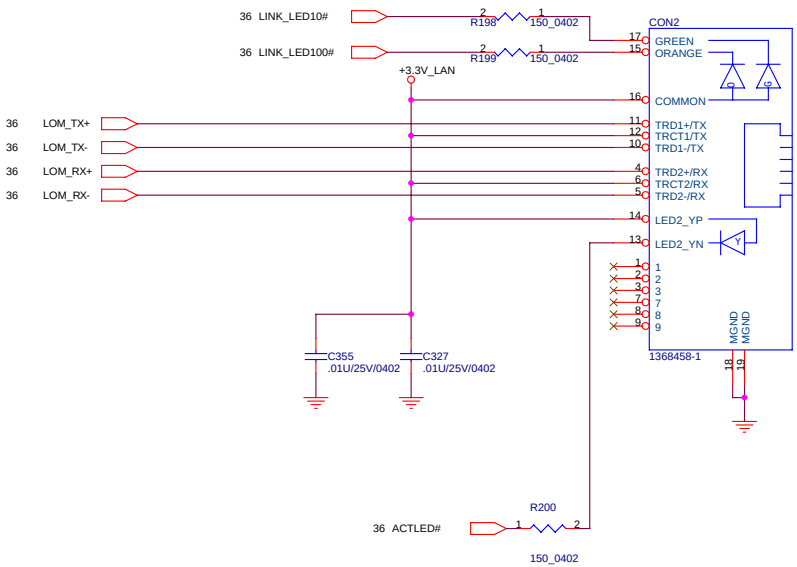
JTAG_TDP 83
JTAG_TCK 80
JTAG_TDI 82
JTAG_TRST_L 73
JTAG_TMS 81

Note: BCM4401 requires 16-bit R/W data width

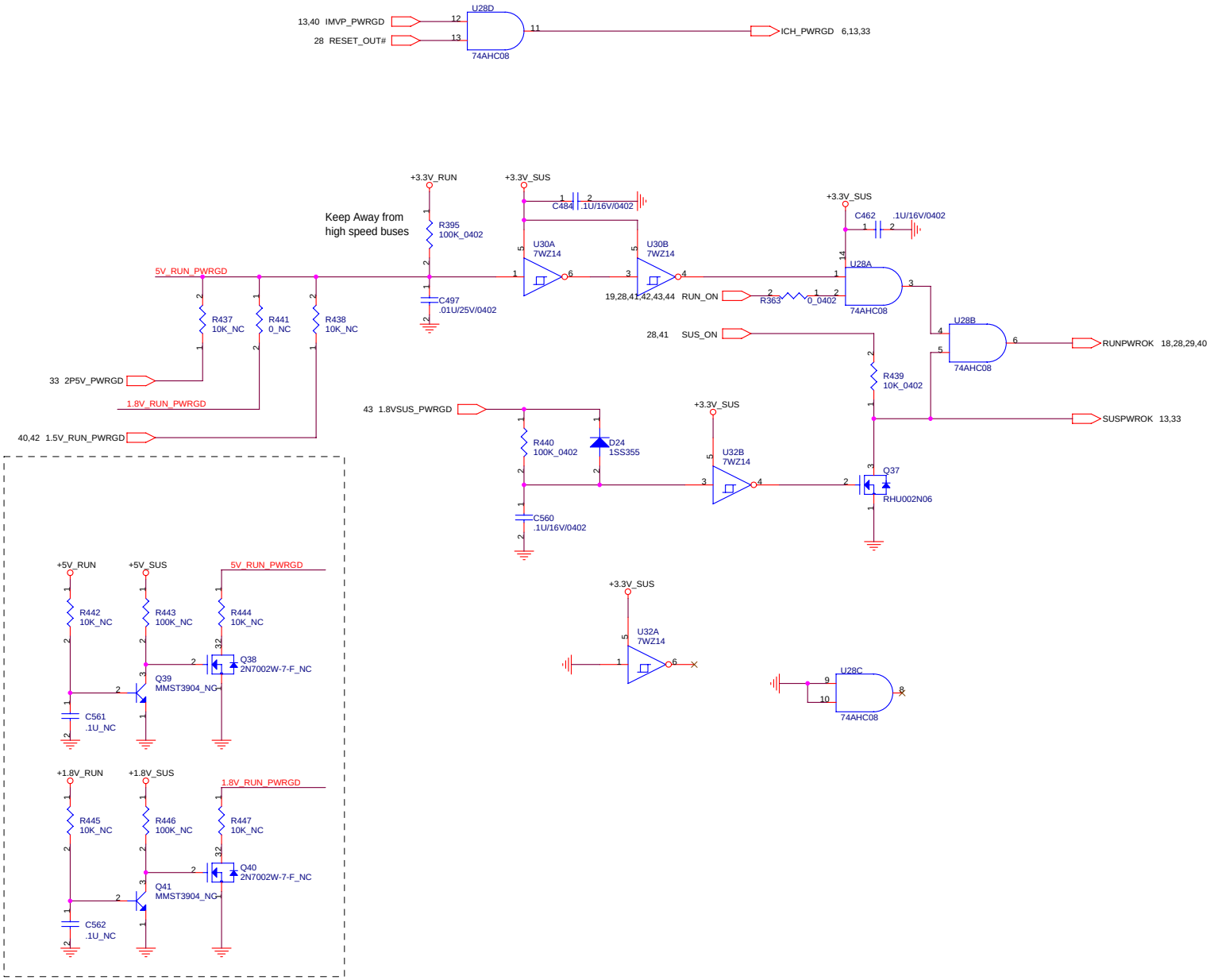
Note: The BCM4401 has weak internal pulldown resistors on the following signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.

QUANTA COMPUTER

Title	LAN (BCM4401)	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 36 of 48	

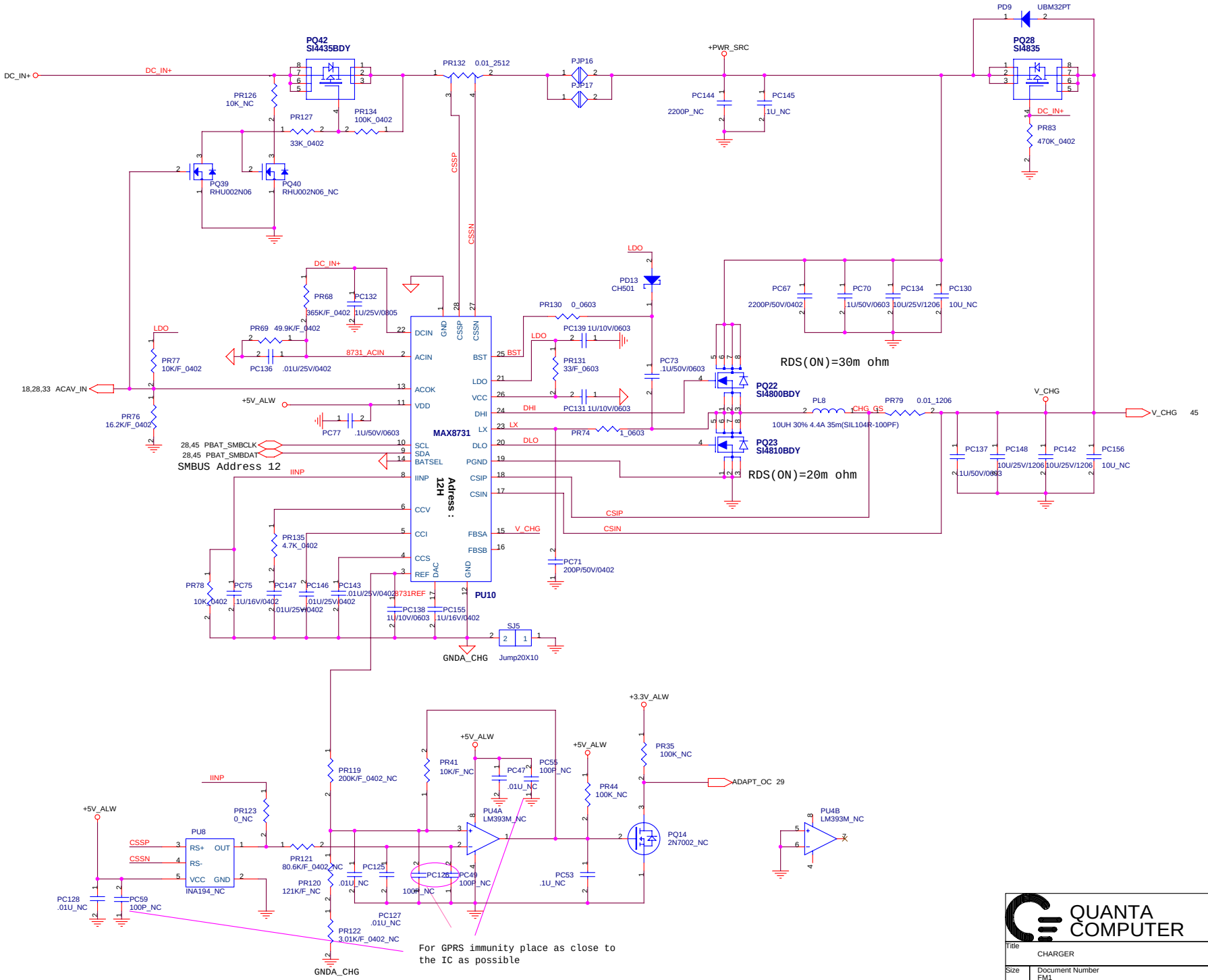


QUANTA COMPUTER		
Title: LAN Jack		
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 37 of 48	



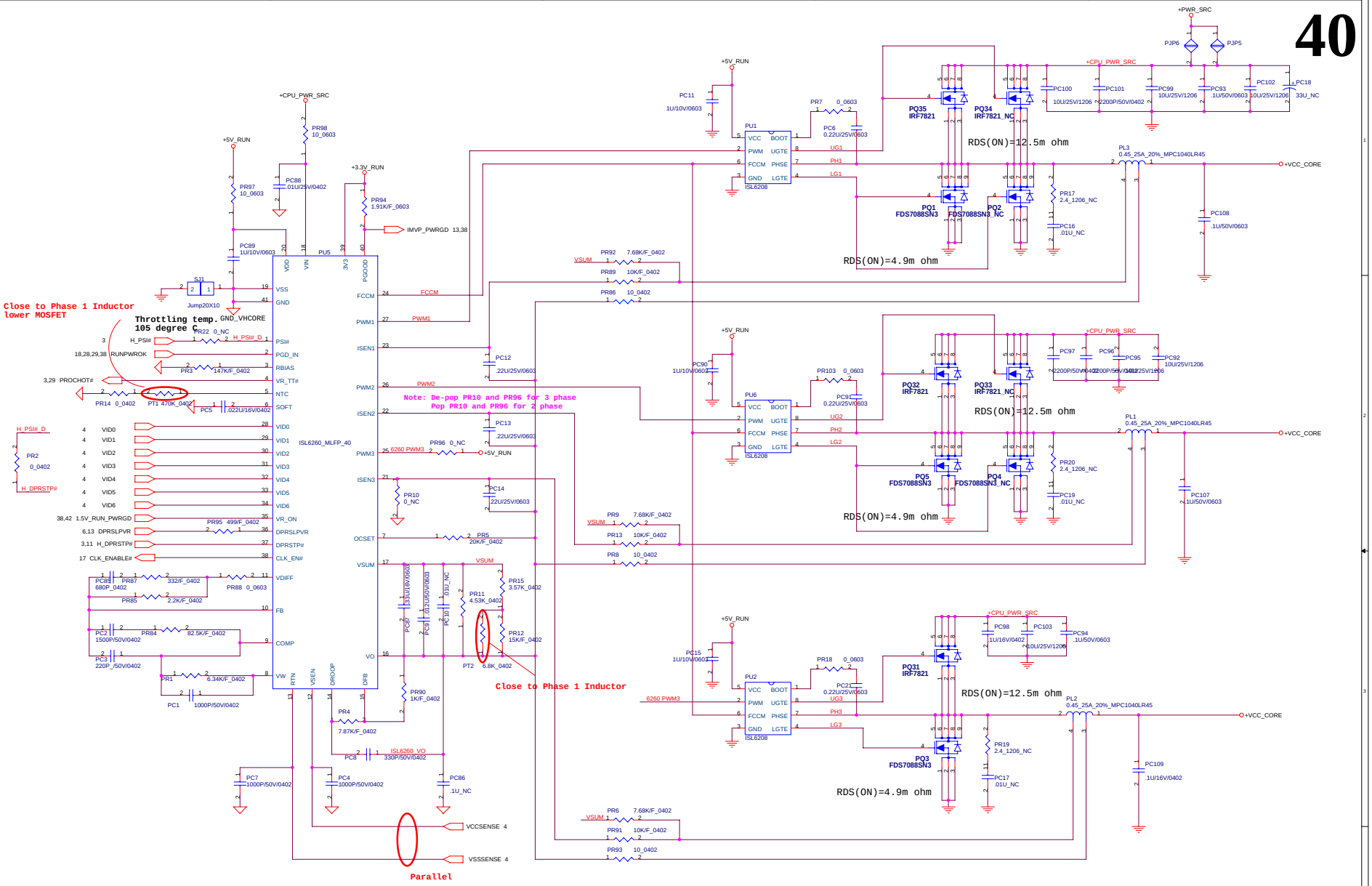
QUANTA COMPUTER

Title	System Reset Circuit	
Size	Document Number FM1	Rev 1A
Date: Tuesday, June 28, 2005	Sheet 38 of 48	



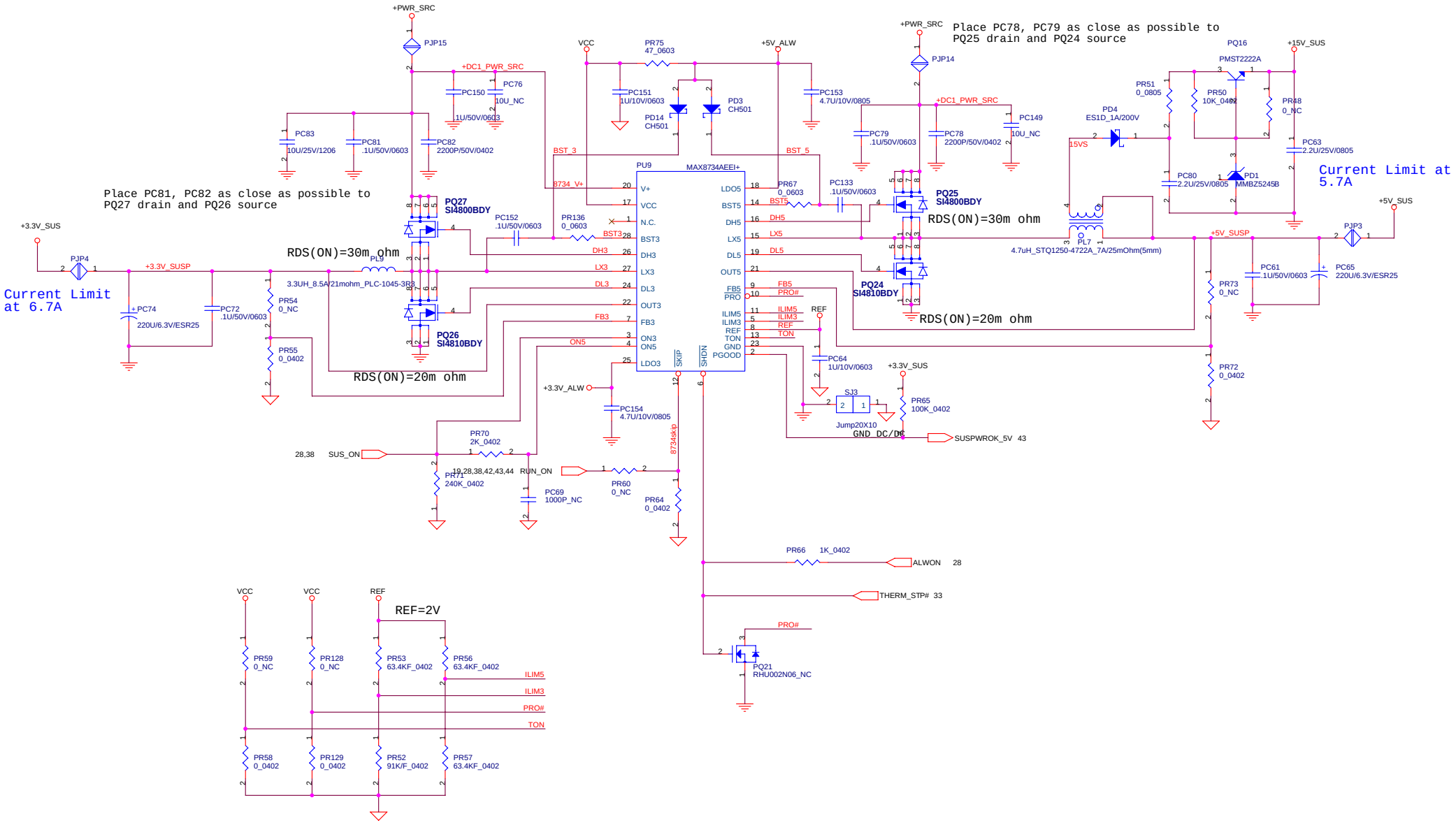
QUANTA COMPUTER

Title	CHARGER	
Size	Document Number FM1	Rev 1A
Date: 2005/4/21	Sheet 39 of 48	



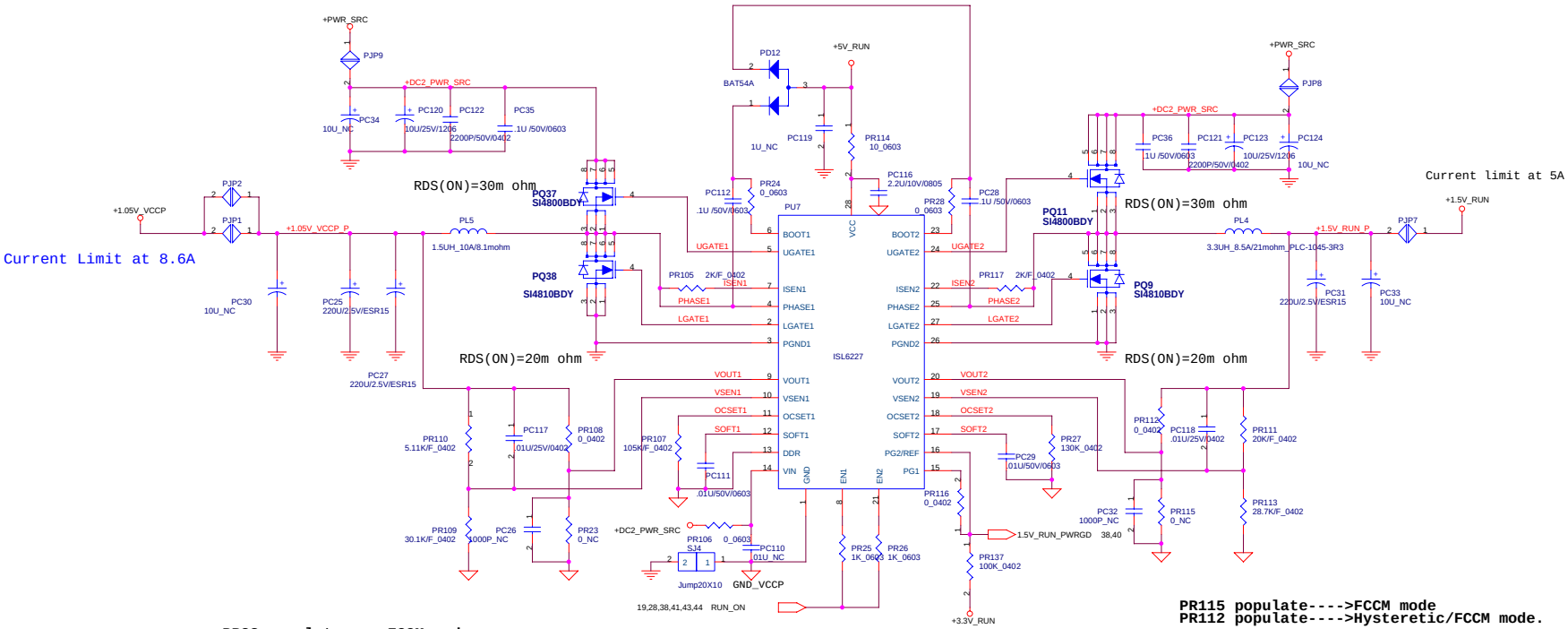
Title	CPU POWER
Size	Document Number FM1
Rev	1A
Date:	2005/4/21
Sheet	40 of 48

QUANTA COMPUTER



QUANTA COMPUTER

Title	3VALW,5VALW,5V,3V	
Size	Document Number FM1	Rev 1A
Date: 2005/4/21	Sheet 41 of 48	

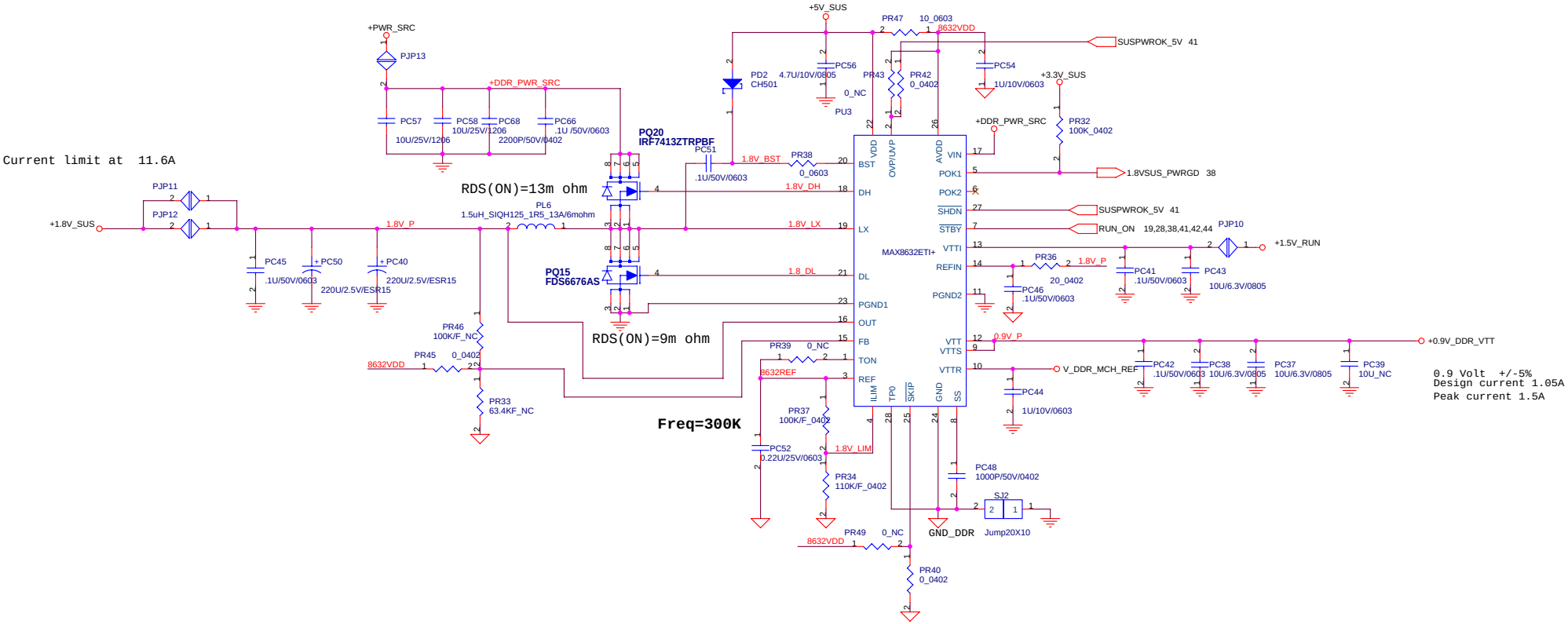


PR23 populate---->FCCM mode
PR108 populate---->Hysteretic/FCCM mode.

PR115 populate---->FCCM mode
PR112 populate---->Hysteretic/FCCM mode.

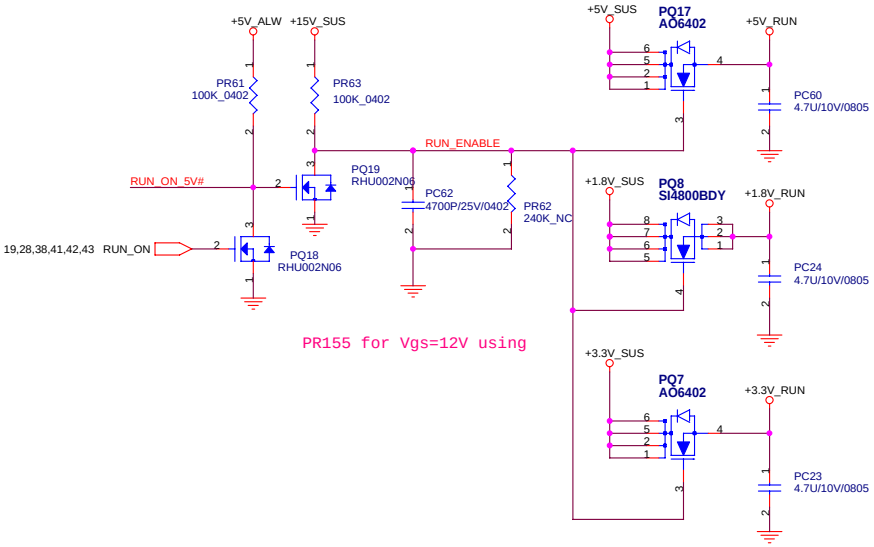
QUANTA COMPUTER

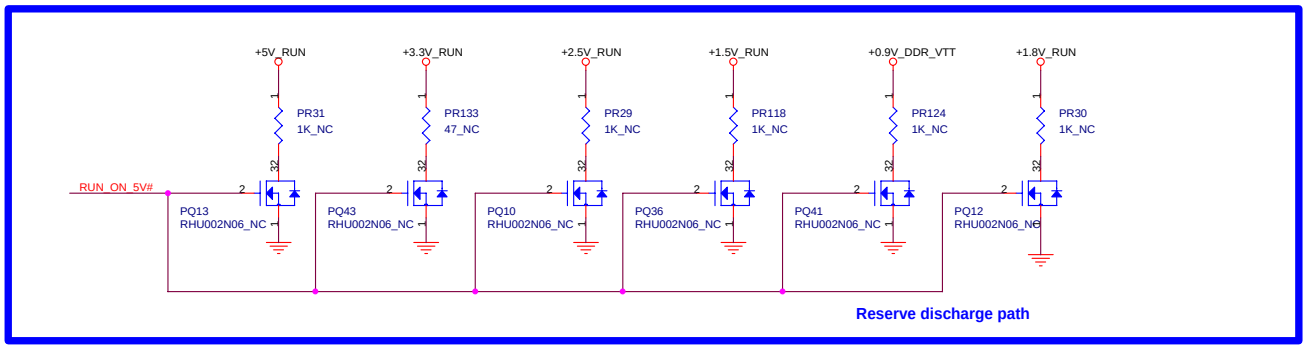
Title	VCCP	
Size	Document Number FM1	Rev 1A
Date: 2005/4/21	Sheet 42 of 48	



QUANTA COMPUTER

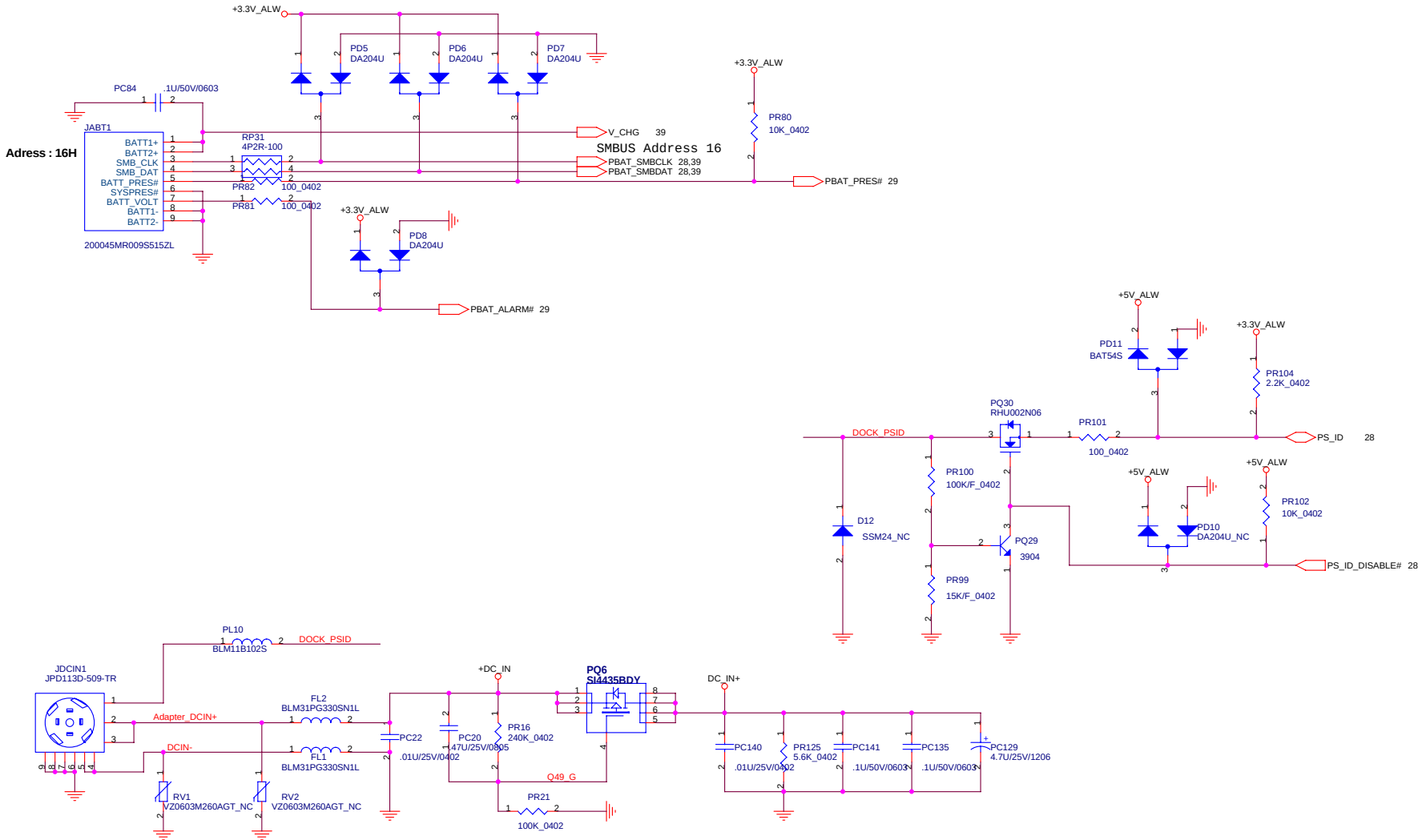
Title	DDR II	
Size	Document Number FM1	Rev 1A
Date: 2005/4/21	Sheet 43 of 48	





QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number FM1	Rev 1A
Date: 2005/4/21	Sheet 44 of 48	



QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number FM1	Rev 1A
Date: 2005/4/21	Sheet 45 of 48	