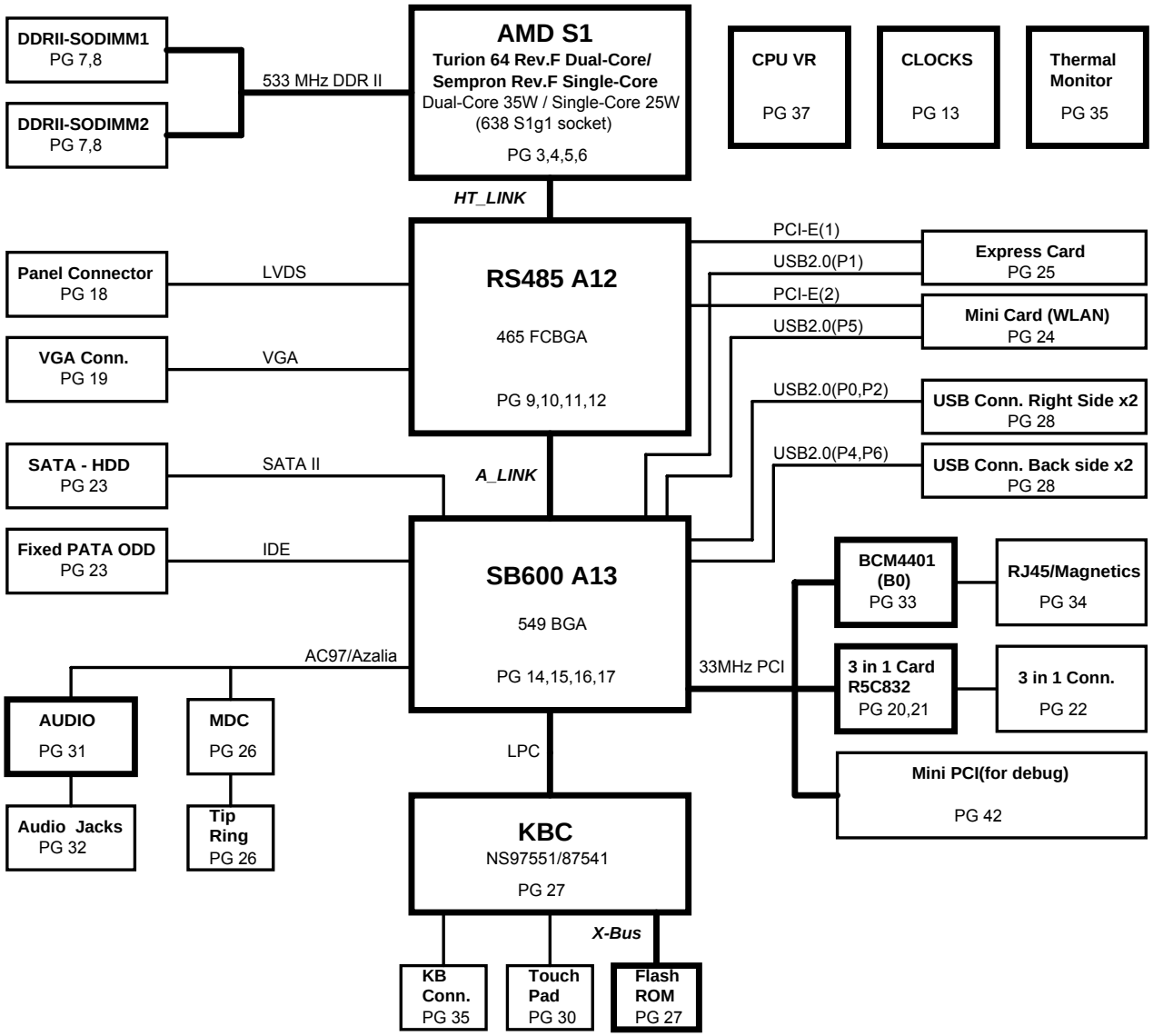
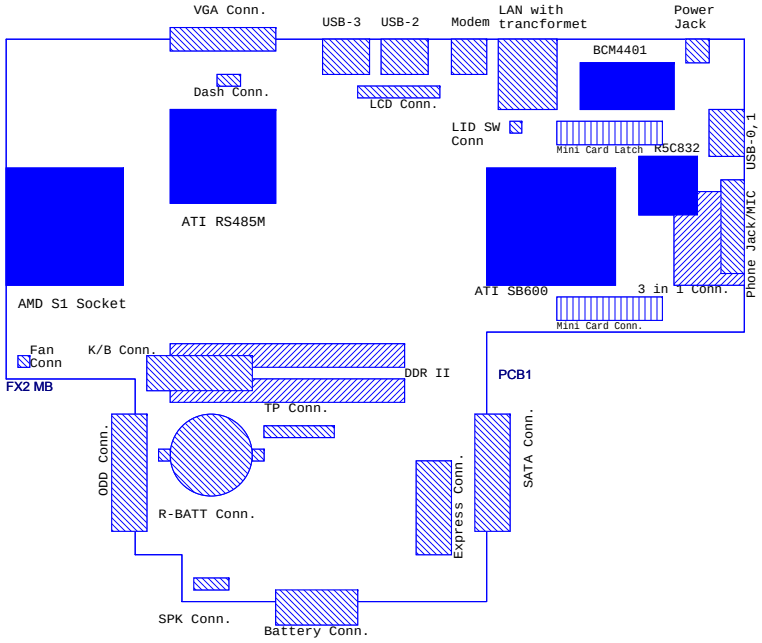
Kirin (FX2 with NS) VER : 1A



CPU VR	CLOCKS	Thermal Monitor	SYSTEM	VCCP DDR II	BATT CHARGER	AC/BATT Conn.	RUN POWER SW
PG 37	PG 13	PG 35	PG 38	PG 39	PG 36	PG 41	PG 40



QUANTA COMPUTER

Title	BLOCK DIAGRAM	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 1 of 47	

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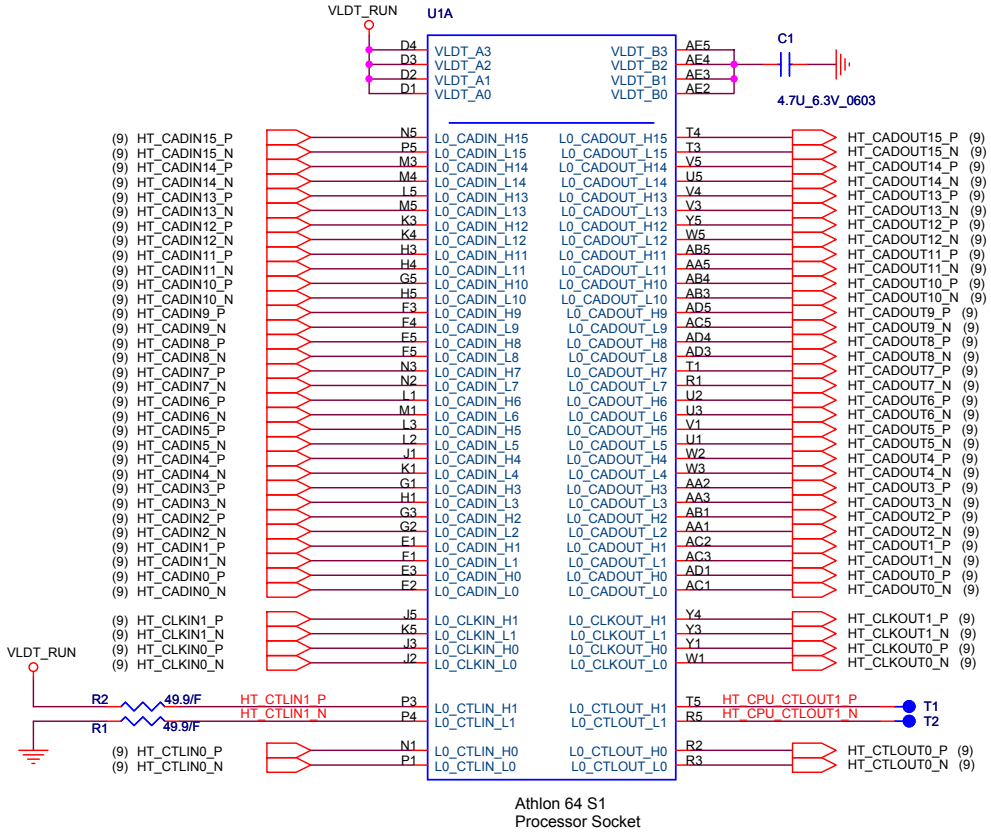
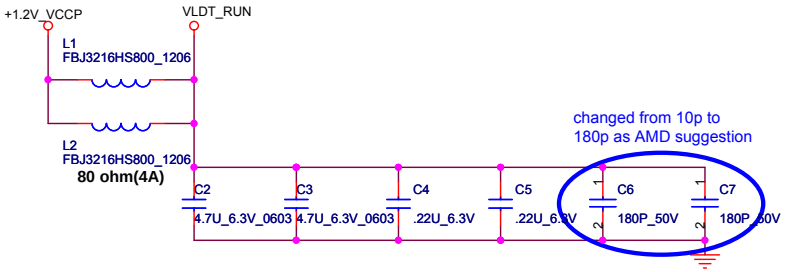
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE





LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

QUANTA COMPUTER

Title	ATHLON64 HT I/F		
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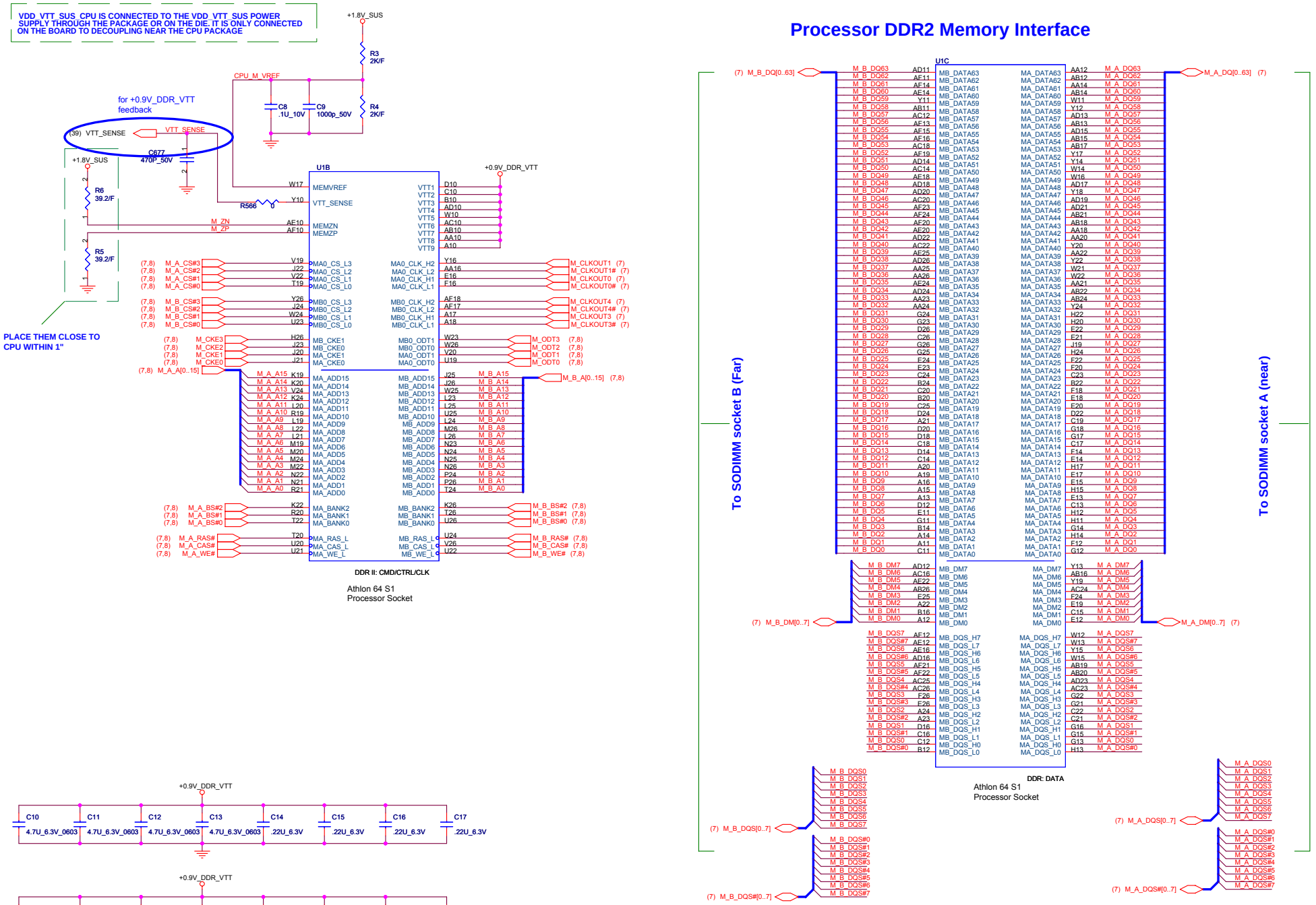
Processor DDR2 Memory Interface



QUANTA COMPUTER

Title	ATHLON64 DDRII MEMORY		
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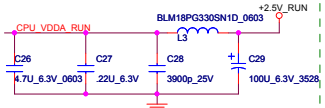
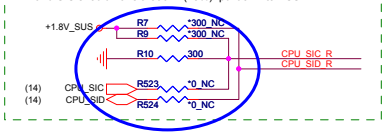
ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

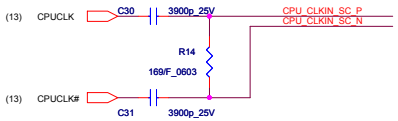
CPU_VDDA_RUN



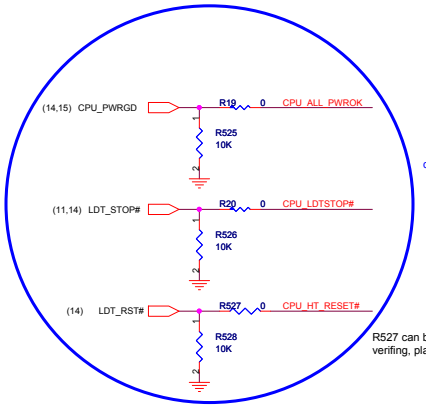
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.



for CPU rev.F , if for rev.G , populate R7,R9,R523,R524 and depopulate R10

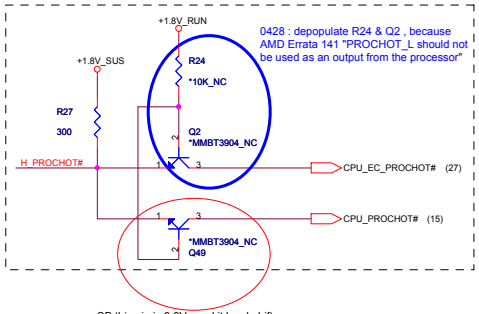


R14 close U1 within 600 mil , C30 & C31 close U1 within 1250 mil



change for SB600 from SB460

R527 can be used for EMI verifing, place close to CPU

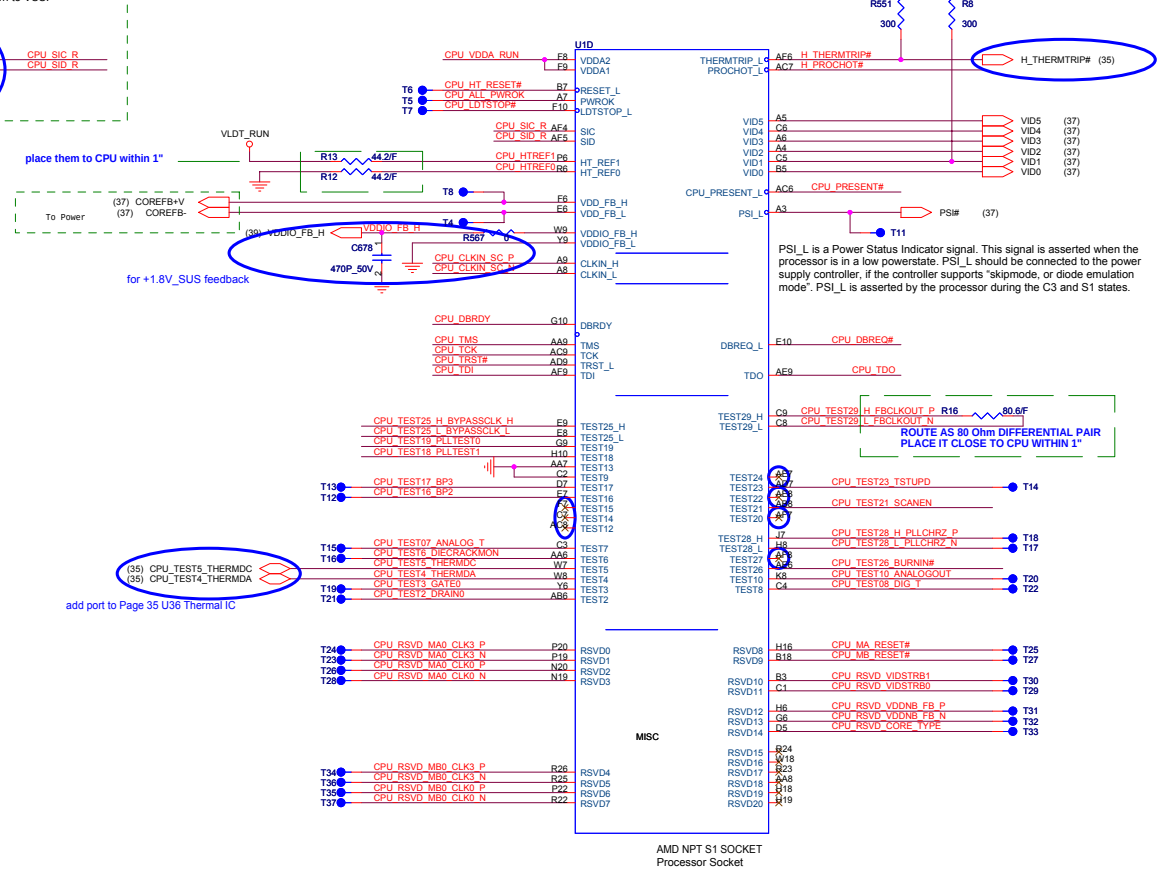


0428 : depopulate R24 & Q2 , because AMD Errata 141 "PROCHOT_L should not be used as an output from the processor"

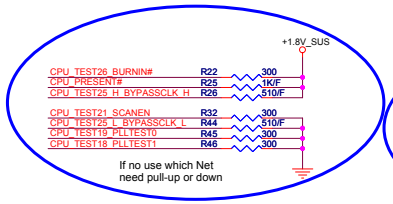
SB this pin is 3.3V,need it level-shift.

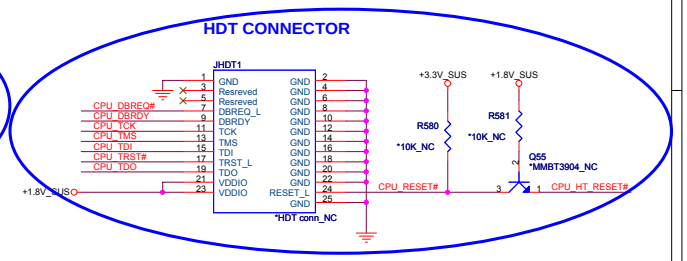
delete ED5 H_THERMTRIP# circuit

delete ED5 thermal sensor



add HDT connector for debug convenience





QUANTA COMPUTER

Title	ATHLON64 CTRL & DEBUG	
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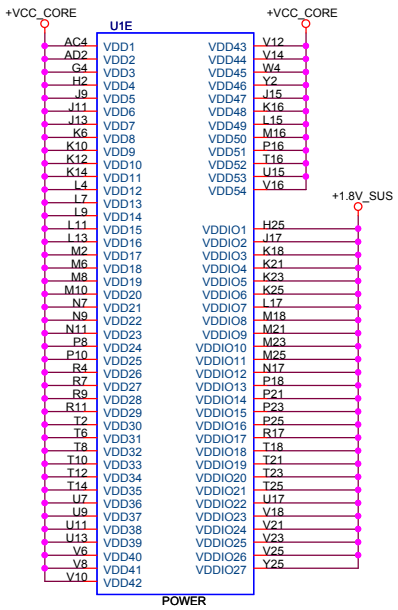
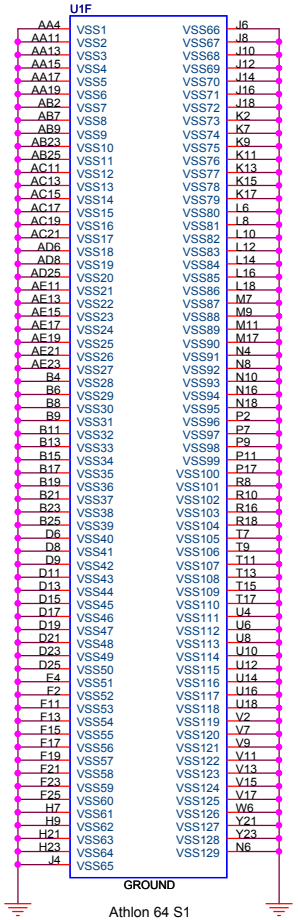
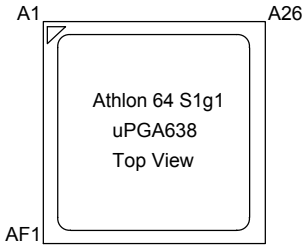
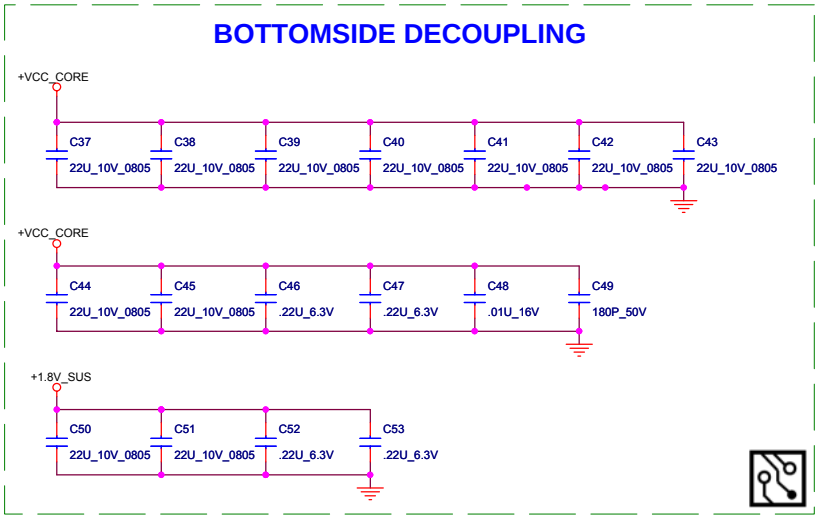


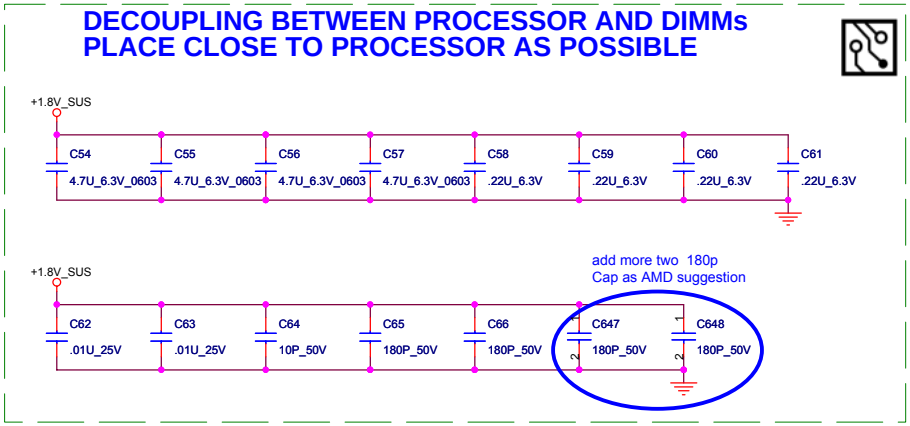
Athlon 64 S1
Processor Socket



Athlon 64 S1
Processor Socket







PROCESSOR POWER AND GROUND

QUANTA COMPUTER

Title	ATHLON64 PWR & GND		
Size	Document Number FX2		Rev 1A
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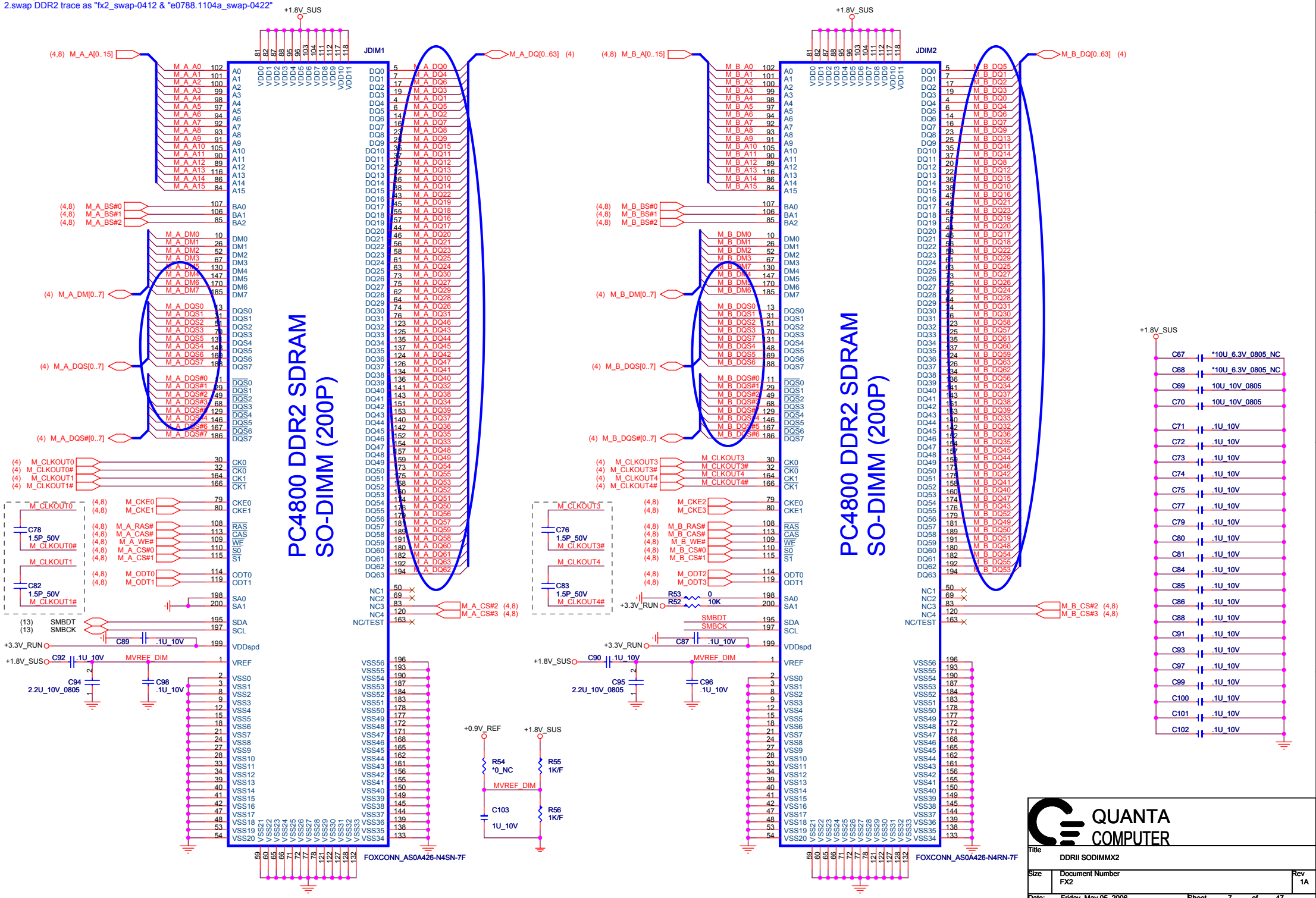
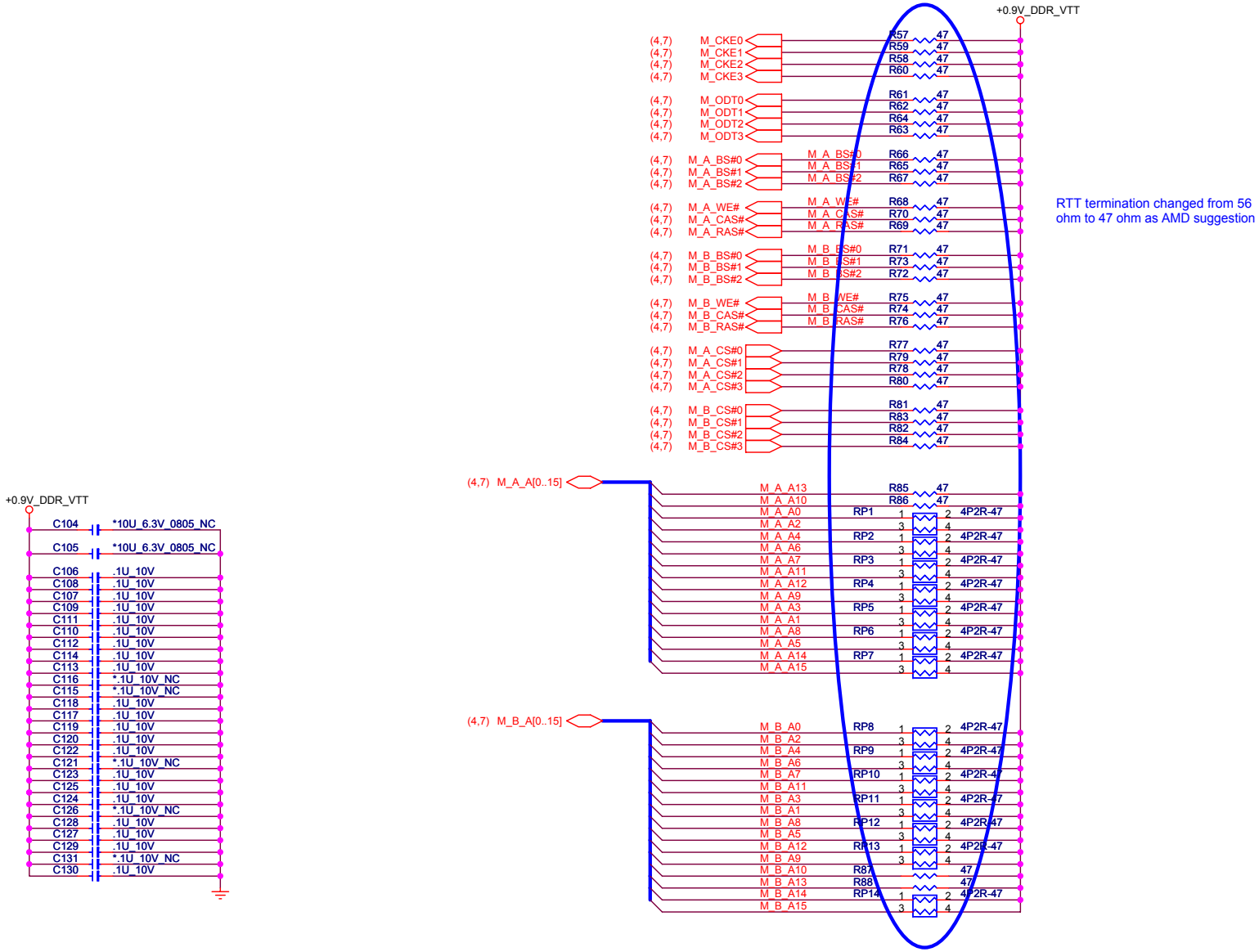
1.Change DDR2 socket(P/N, Description, footprint, part reference, value)
2.swap DDR2 trace as "fx2_swap-0412 & "e0788.1104a_swap-0422"



QUANTA COMPUTER

Title	DDRII SODIMMX2		
Size	Document Number FX2		Rev 1A
Date: Friday, May 05, 2006	Sheet 7 of 47		



RTT termination changed from 56 ohm to 47 ohm as AMD suggestion

QUANTA COMPUTER

Title	DDRII TERMINATION
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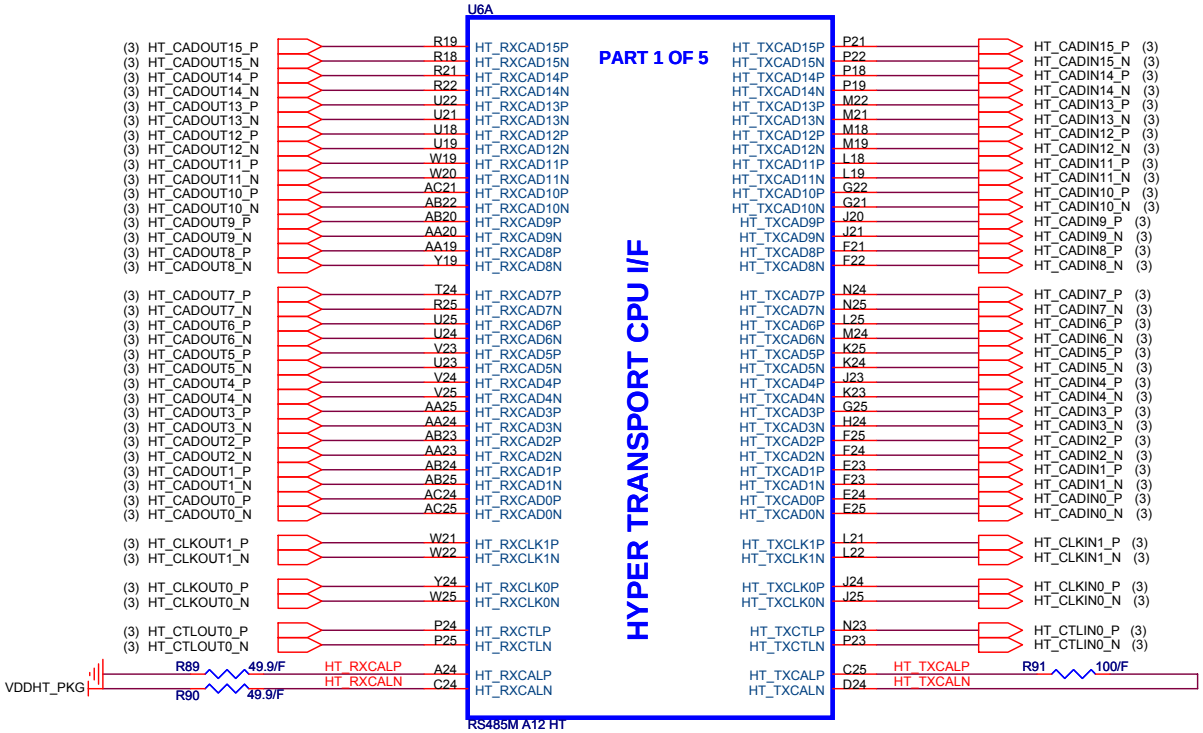
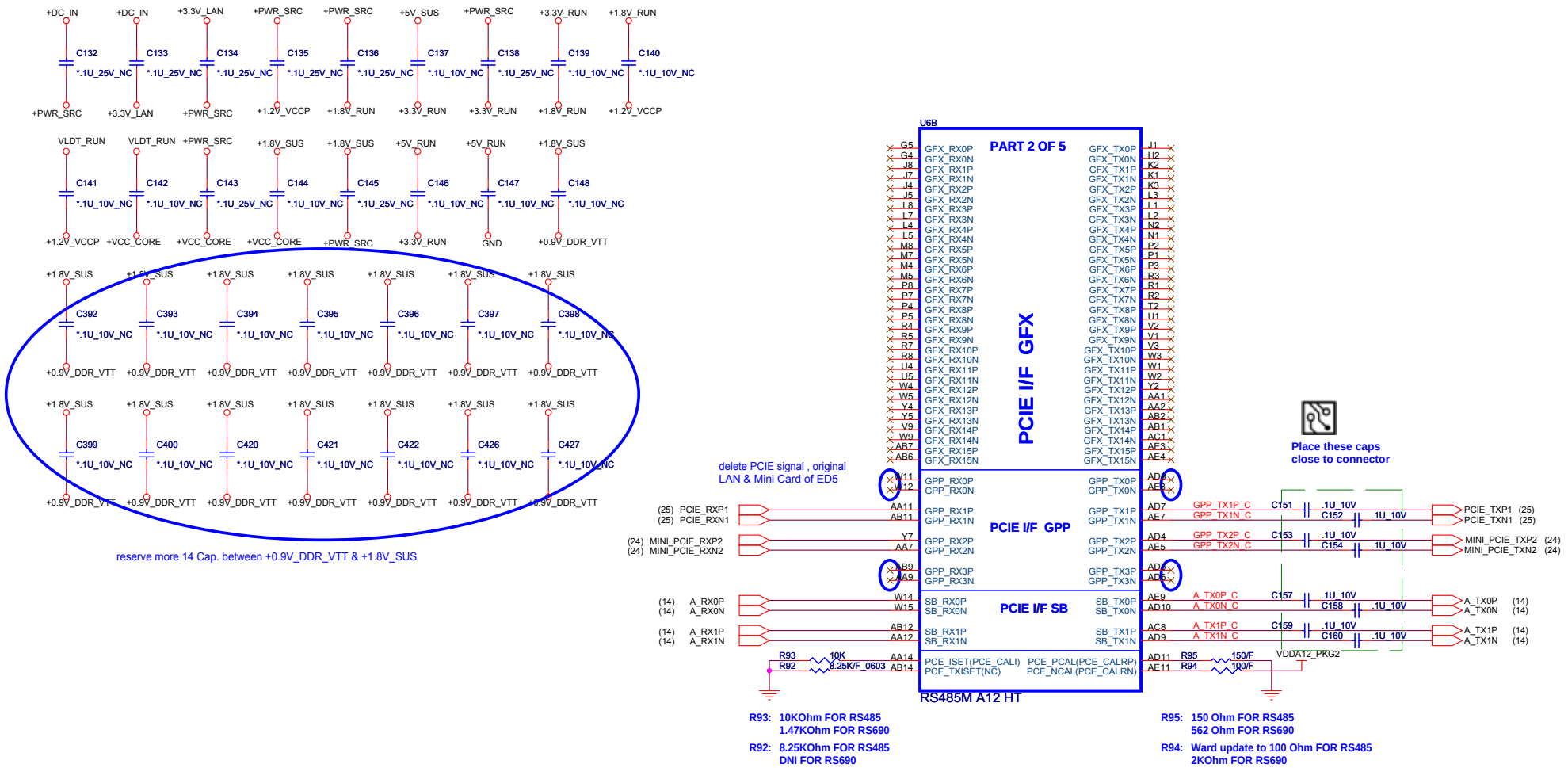


QUANTA COMPUTER

Title	RS485-HT LINK0 I/F		
Size	Document Number FX2		Rev 1A
Date: Friday, May 05, 2006	Sheet 9 of 47		



R93: 10KOhm FOR RS485
1.47KOhm FOR RS690

R92: 8.25KOhm FOR RS485
DNI FOR RS690

R95: 150 Ohm FOR RS485
562 Ohm FOR RS690

R94: Ward update to 100 Ohm FOR RS485
2KOhm FOR RS690

QUANTA COMPUTER

Title	RS485-PCIE LINK I/F	
Size	Document Number FX2	Rev 1A
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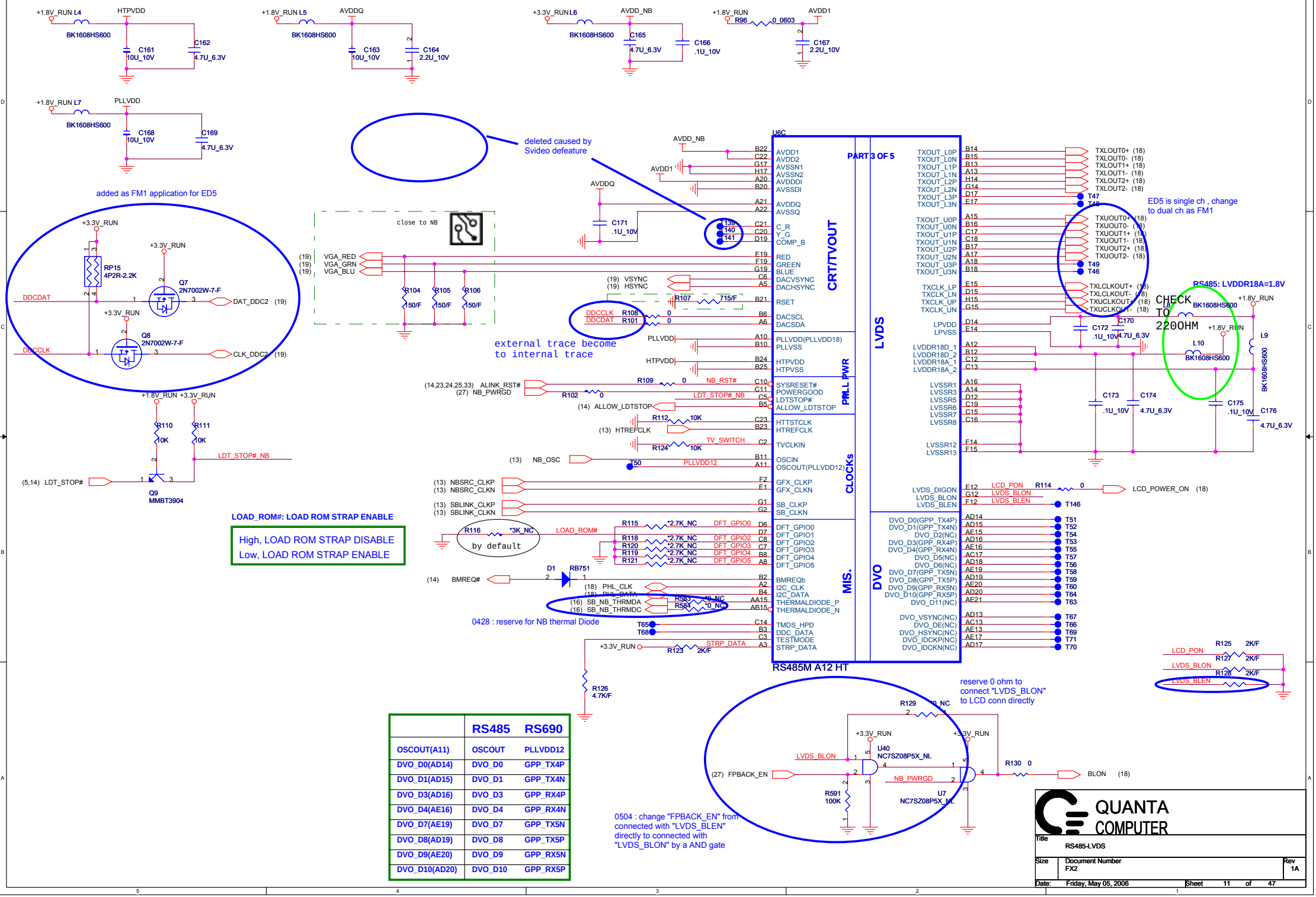
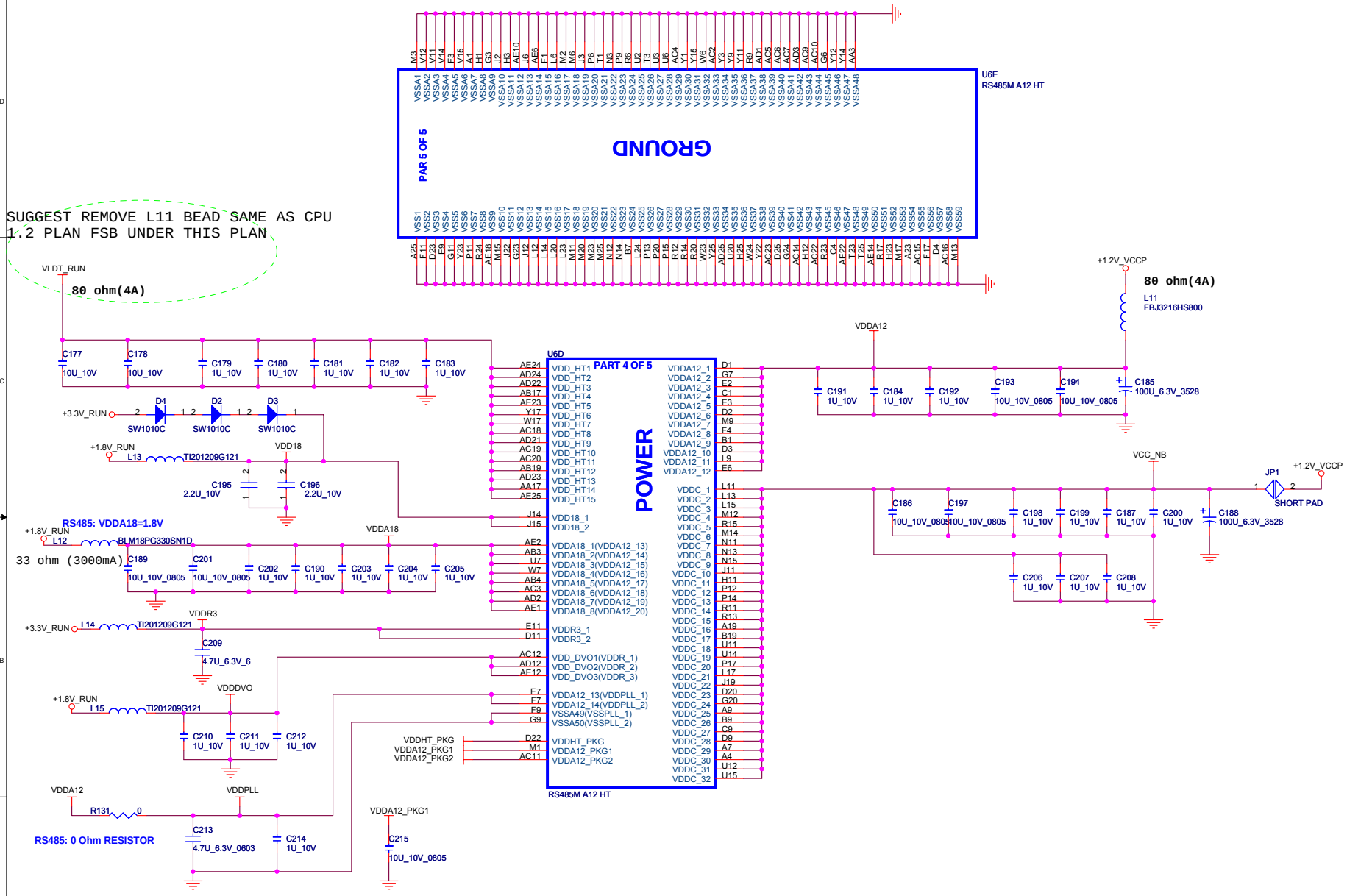


	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVDD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P



NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

QUANTA COMPUTER

Title	RS485-POWER	
Size	Document Number FX2	Rev 1A
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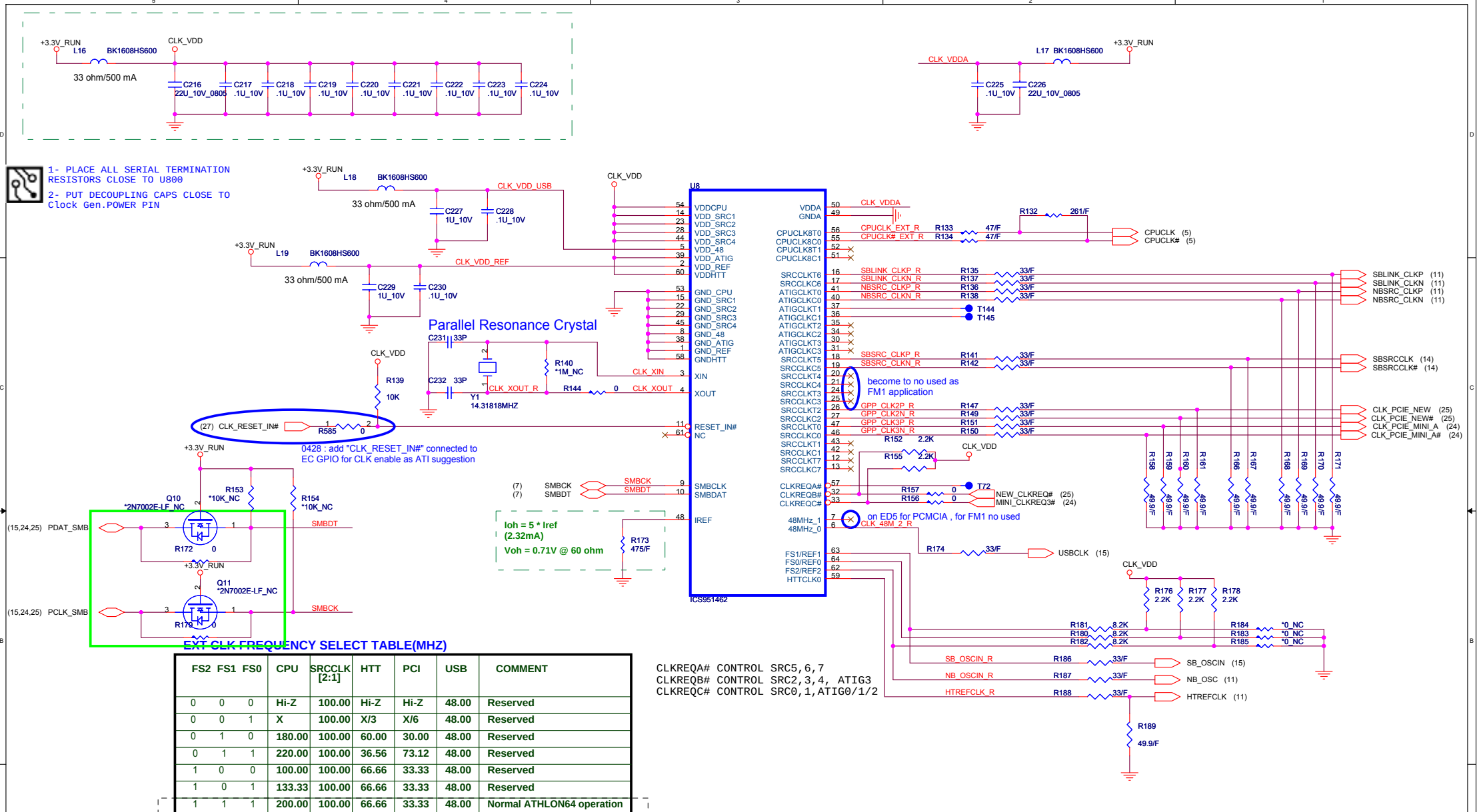
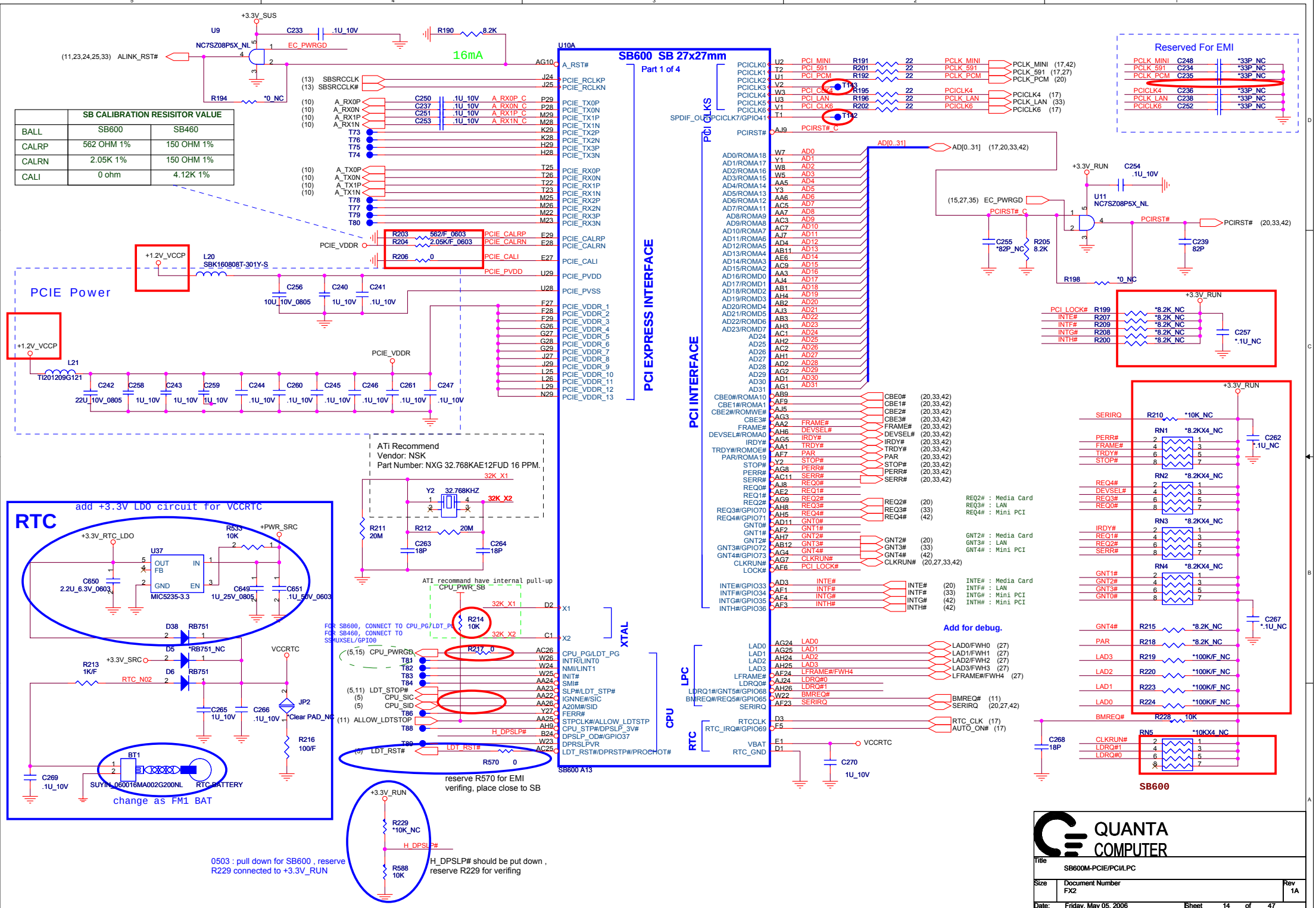
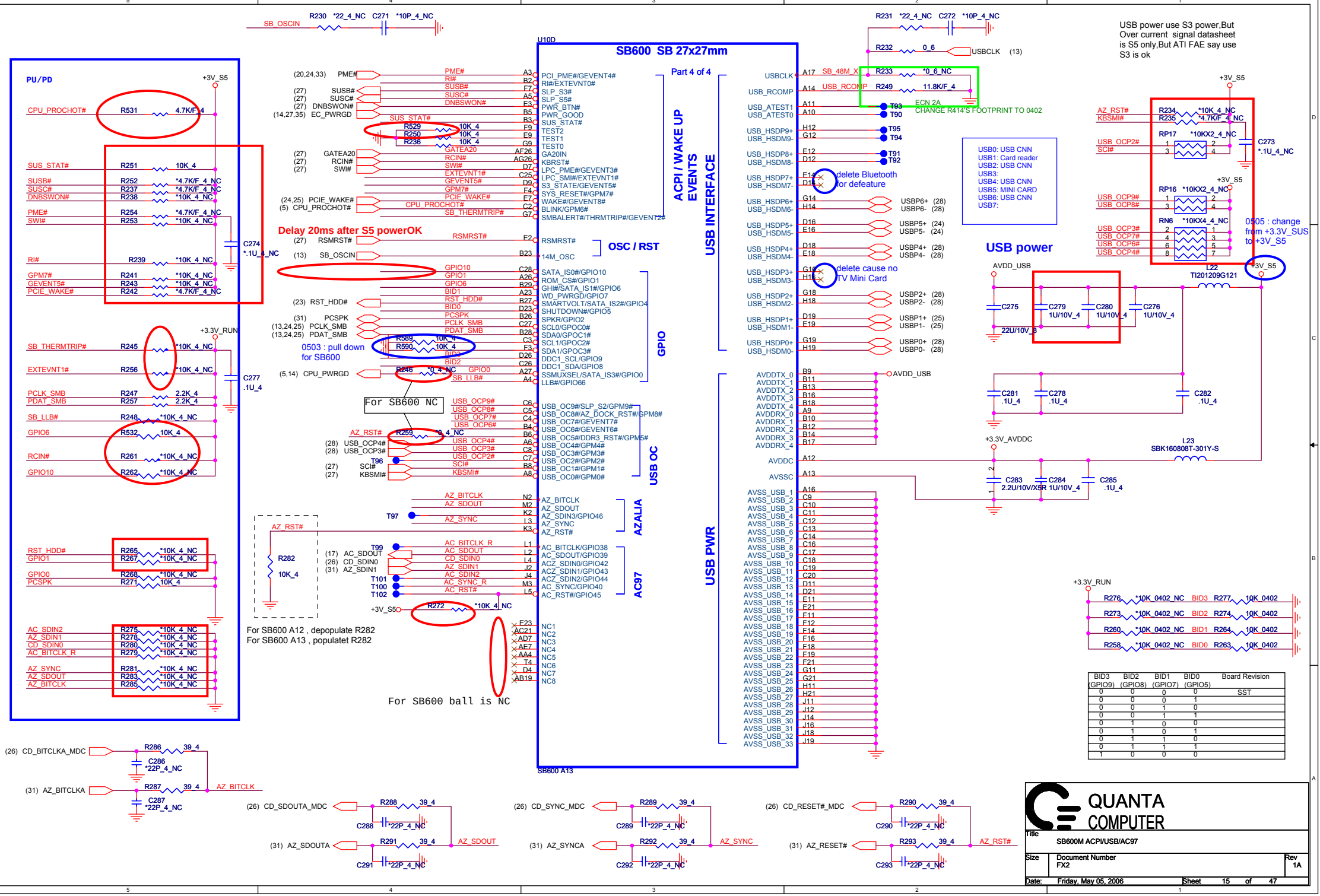


FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation



SB CALIBRATION RESISITOR VALUE		
BALL	SB600	SB460
CALRP	562 OHM 1%	150 OHM 1%
CALRN	2.05K 1%	150 OHM 1%
CALI	0 ohm	4.12K 1%


SB600 SB 27x27mm
U10D
Part 4 of 4
ACPI / WAKE UP EVENTS
USB INTERFACE
GPIO
USB OC
AZALIA
AC97
USB PWR
OSC / RST
PU/PD
USB power
USB power use S3 power,But Over current signal datasheet is S5 only,But ATI FAE say use S3 is ok
USB0: USB CNN
USB1: Card reader
USB2: USB CNN
USB3:
USB4: USB CNN
USB5: MINI CARD
USB6: USB CNN
USB7:
delete Bluetooth for defeature
delete cause no TV Mini Card
ECN 2A
CHANGE R414'S FOOTPRINT TO 0402
Delay 20ms after S5 powerOK
0503 : pull down for SB600
0505 : change from +3.3V_SUS to +3V_S5
For SB600 NC
For SB600 A12 , depopulate R282
For SB600 A13 , populatet R282
For SB600 ball is NC
SB600 A13
BID3 BID2 BID1 BID0 Board Revision
(GPIO9) (GPIO8) (GPIO7) (GPIO5)
0 0 0 0 SST
0 0 0 1
0 0 1 0
0 0 1 1
0 1 0 0
0 1 0 1
0 1 1 0
0 1 1 1
1 0 0 0
QUANTA COMPUTER
Title
SB600M ACPI/USB/AC97
Size
Document Number
FX2
Rev
1A
Date: Friday, May 05, 2006
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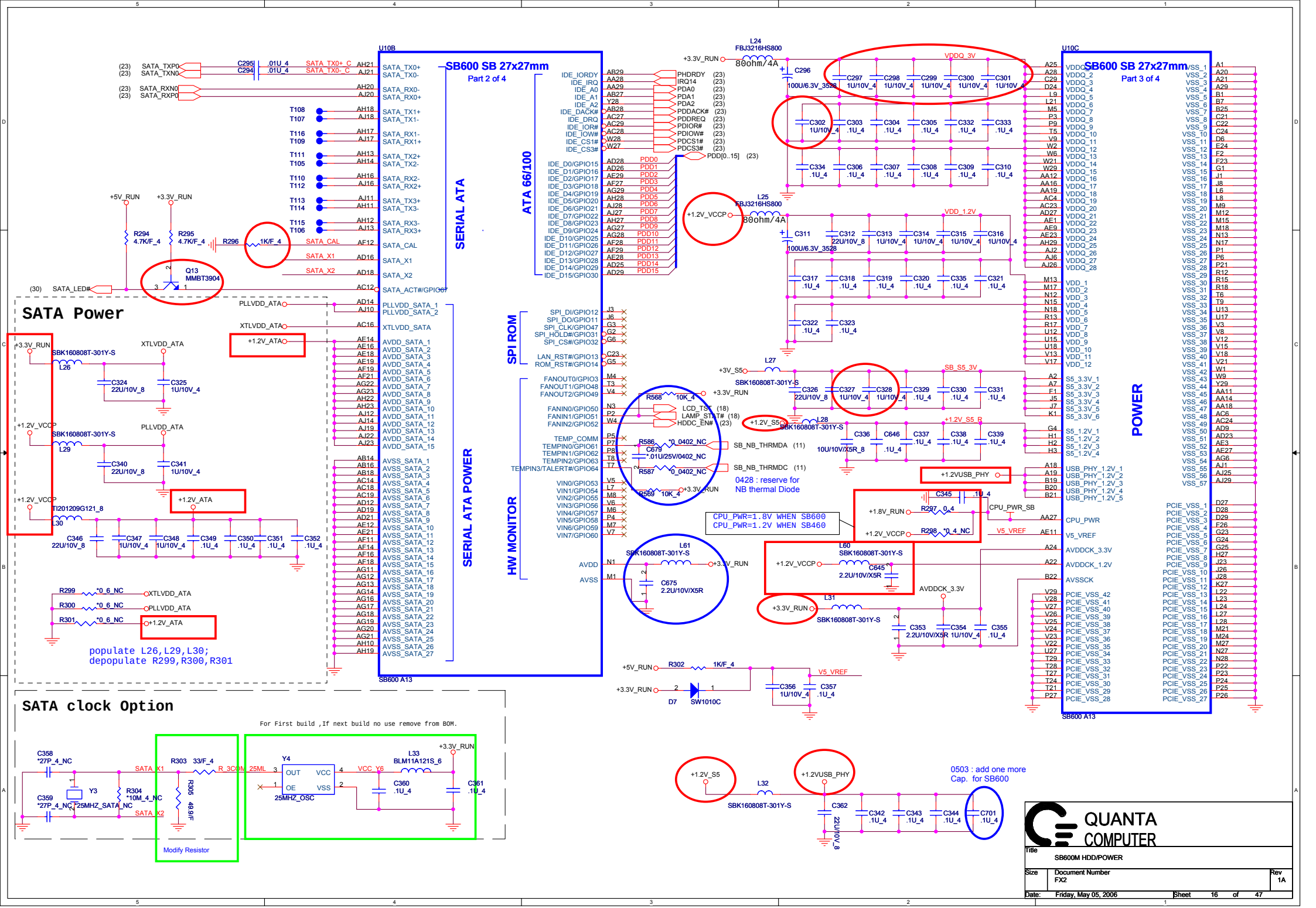

QUANTA COMPUTER

Title	SB600M HDD/POWER
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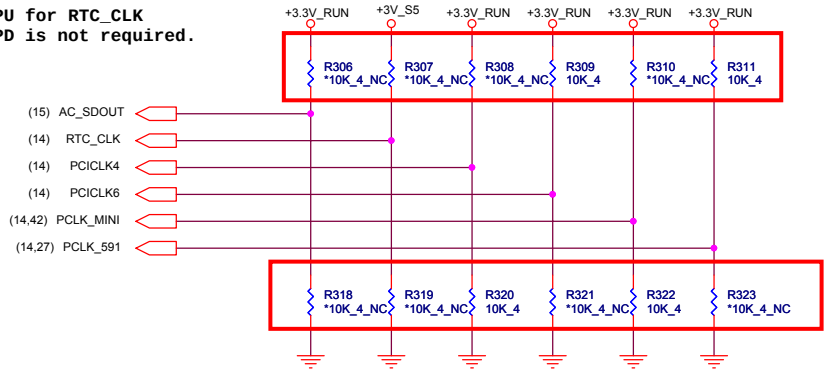
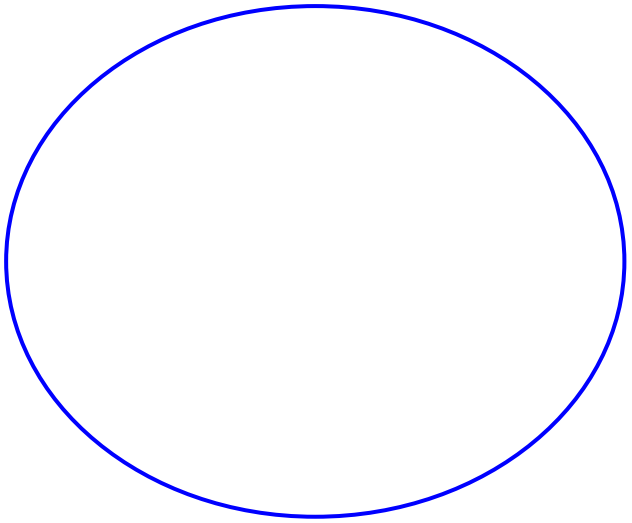
SB600 has 15K internal PD for AC_SDOUT
15K internal PU for RTC_CLK
,External PU/PD is not required.

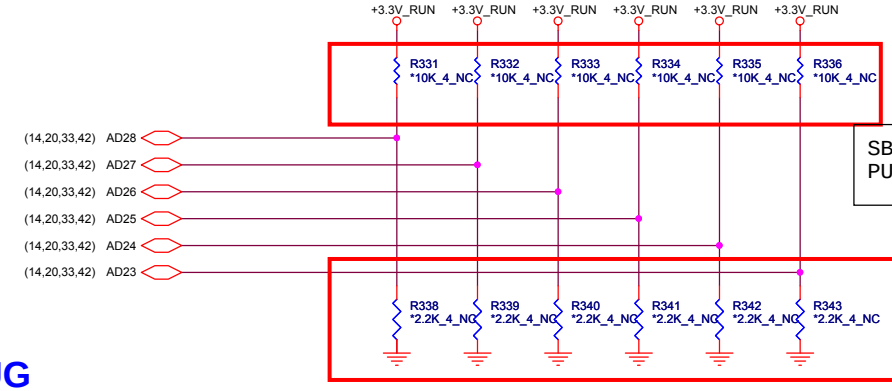


delete SB460 setting



REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI PCLK_591 / PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48 DEFAULT	CPU IF=K8 DEFAULT	H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	



SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Use Long Reset DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	boot fail time disabled DEFAULT
PULL LOW	USE SHORT RESET	Use Short Reset	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	boot fail time enabled
	SB460 Only	SB600 Only					SB600 Only

QUANTA COMPUTER

Title	SB600M STRAPS	
Size	Document Number FX2	Rev 1A
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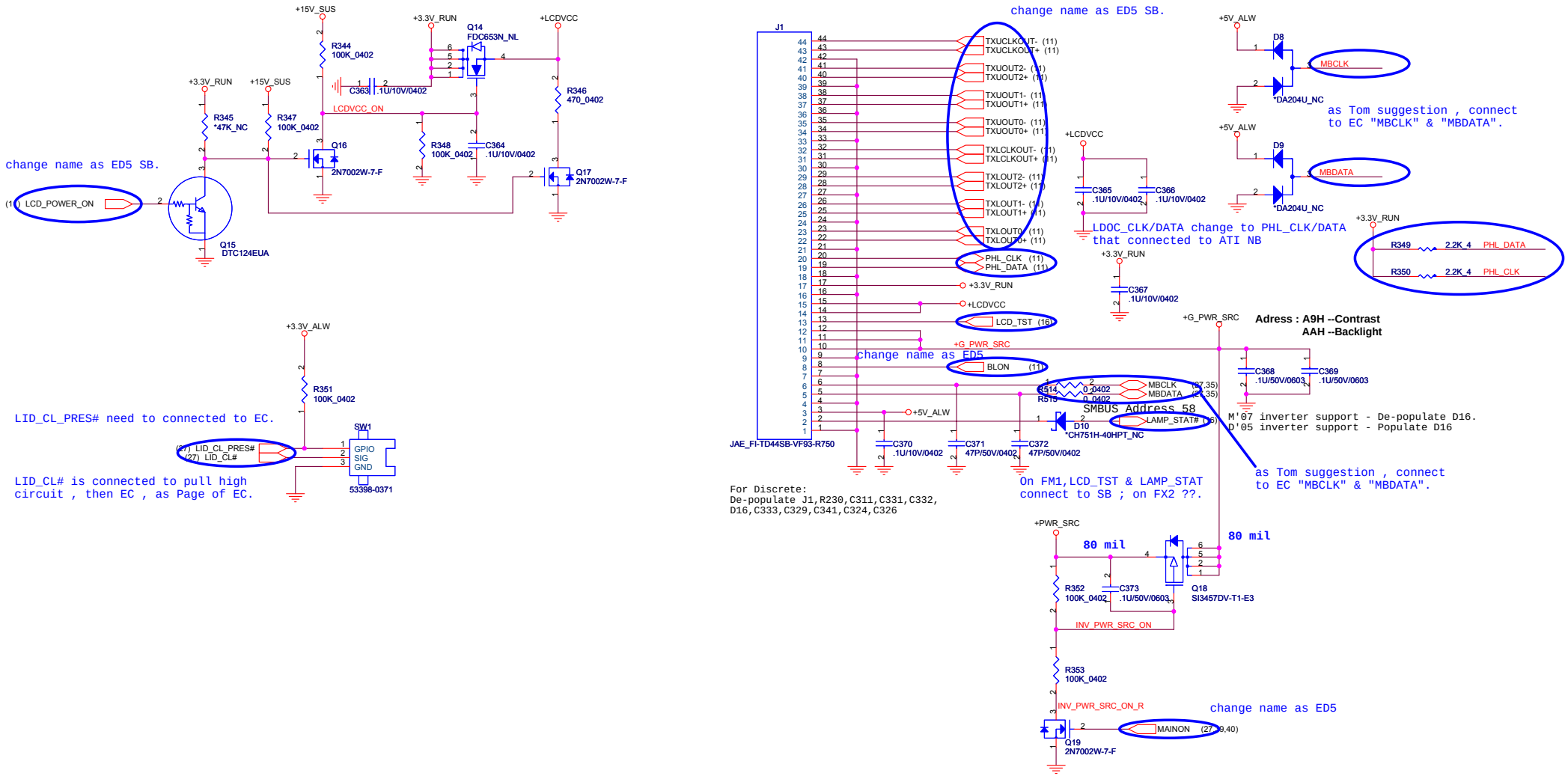

QUANTA COMPUTER

Title	LCD CONN	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 18 of 47	

VGA is kept as FM1's solution.
Page 6 has some change for DDCCLK & DDCDAT.

Place All of those
Inductors Caps close
to JVGA1 <200 mils

(11) VGA_RED
(11) VGA_GRN
(11) VGA_BLU
L34 BLM21PG220SN1D
L35 BLM21PG220SN1D
L36 BLM21PG220SN1D
R354 150/F_0402
R355 150/F_0402
R356 150/F_0402
C375 *22P_NC
C376 *22P_NC
C377 *22P_NC
C378 *10P_NC
C379 *10P_NC
C380 *10P_NC
RED
GREEN
BLUE
+5V_RUN
D11 CH501H-40PT
C374 .01U/25V/0402
CRT_VCC
JVGA1
DZ11A91-ND200-7F
M_ID2#
T117 PAD
C381 .1U/10V/0402
+3.3V_RUN
D12 *DA204U_NC
D14 *DA204U_NC
D15 *DA204U_NC
Place D4,D5,D6 close
to JVGA1 <200 mils
+5V_RUN
D13 CH501H-40PT
C382 .1U/10V/0402
(11) HSYNC
R357 39_0402
U12 74AHCT1G125GW
HSYNC_B
R359 1K_0402
(11) VSYNC
R360 39_0402
U13 74AHCT1G125GW
VSYNC_B
CRT_VCC
RP18 4P2R-2.2K
(11) DAT_DDC2
(11) CLK_DDC2
R358 0_0402
Place near U12 <200mil
HSYNC_R
C383 10P/50V/0402
C384 10P/50V/0402
L37 BLM11A121S
JVGA_HS
R361 0_0402
Place near U13 <200mil
VSYNC_R
L38 BLM11A121S
JVGA_VS
C385 *10P_NC
C386 *10P_NC
C387 *22P_NC
C388 *22P_NC

delete Svideo for defeature

QUANTA COMPUTER

Title	CRT	
Size	Document Number FX2	Rev 1A
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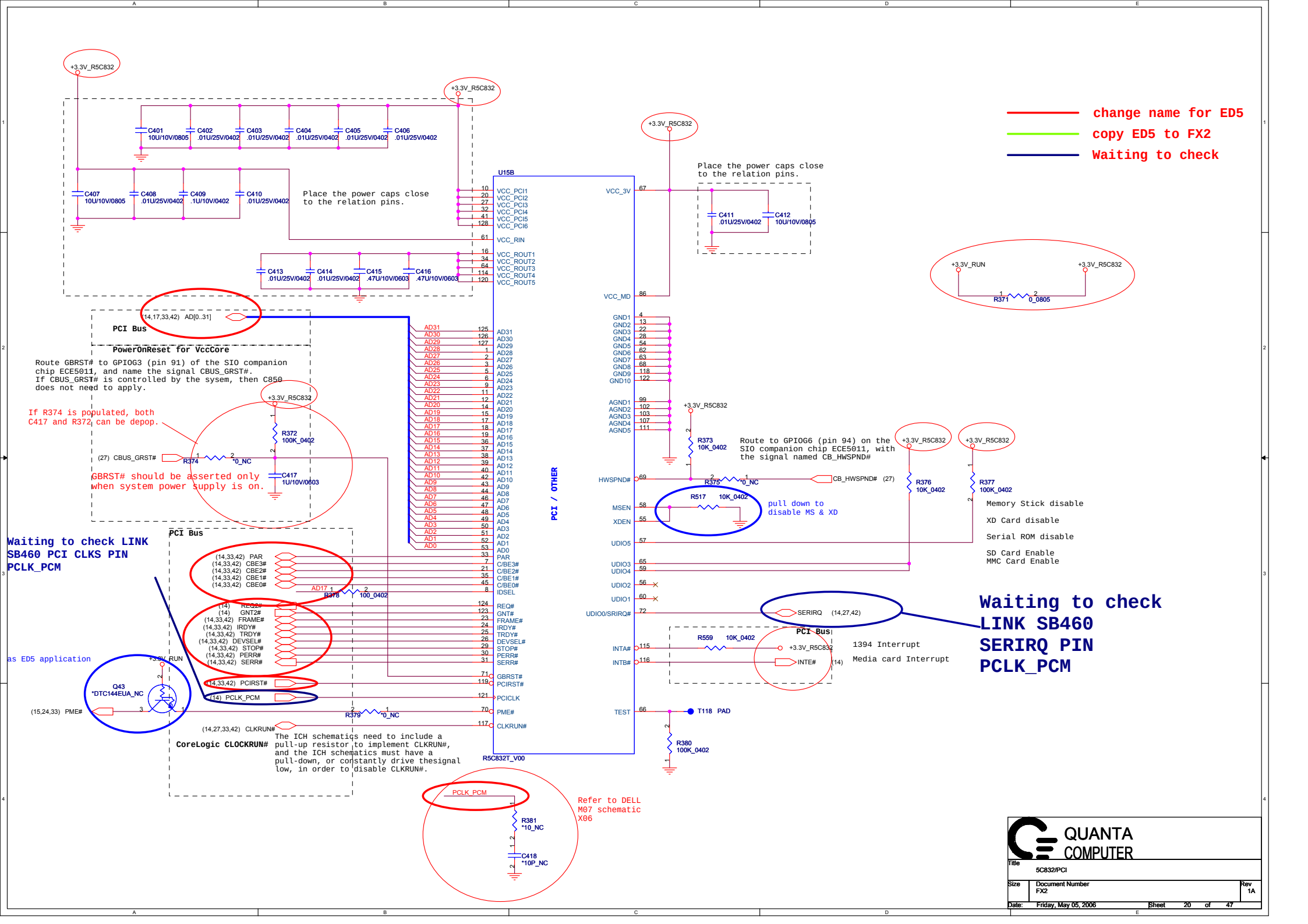
change name for ED5
copy ED5 to FX2
Waiting to check
U15B
PCI / OTHER
R5C832T_V00
Place the power caps close to the relation pins.
PCI Bus
PowerOnReset for VccCore
Route GBRST# to GPIOG3 (pin 91) of the SIO companion chip ECE5011, and name the signal CBUS_GRST#.
If CBUS_GRST# is controlled by the sysem, then C850 does not need to apply.
If R374 is populated, both C417 and R372 can be depop.
GBRST# should be asserted only when system power supply is on.
Route GBRST# to GPIOG3 (pin 91) of the SIO companion chip ECE5011, and name the signal CBUS_GRST#.
Route to GPIOG6 (pin 94) on the SIO companion chip ECE5011, with the signal named CB_HWSPND#
pull down to disable MS & XD
Memory Stick disable
XD Card disable
Serial ROM disable
SD Card Enable
MMC Card Enable
Waiting to check LINK SB460 PCI CLKS PIN PCLK_PCM
as ED5 application
Waiting to check LINK SB460 SERIRQ PIN PCLK_PCM
1394 Interrupt
Media card Interrupt
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive thesignal low, in order to disable CLKRUN#.
CoreLogic CLOCKRUN#
Refer to DELL M07 schematic X06
QUANTA COMPUTER
Title 5C832/PCI
Size Document Number FX2
Rev 1A
Date: Friday, May 05, 2006
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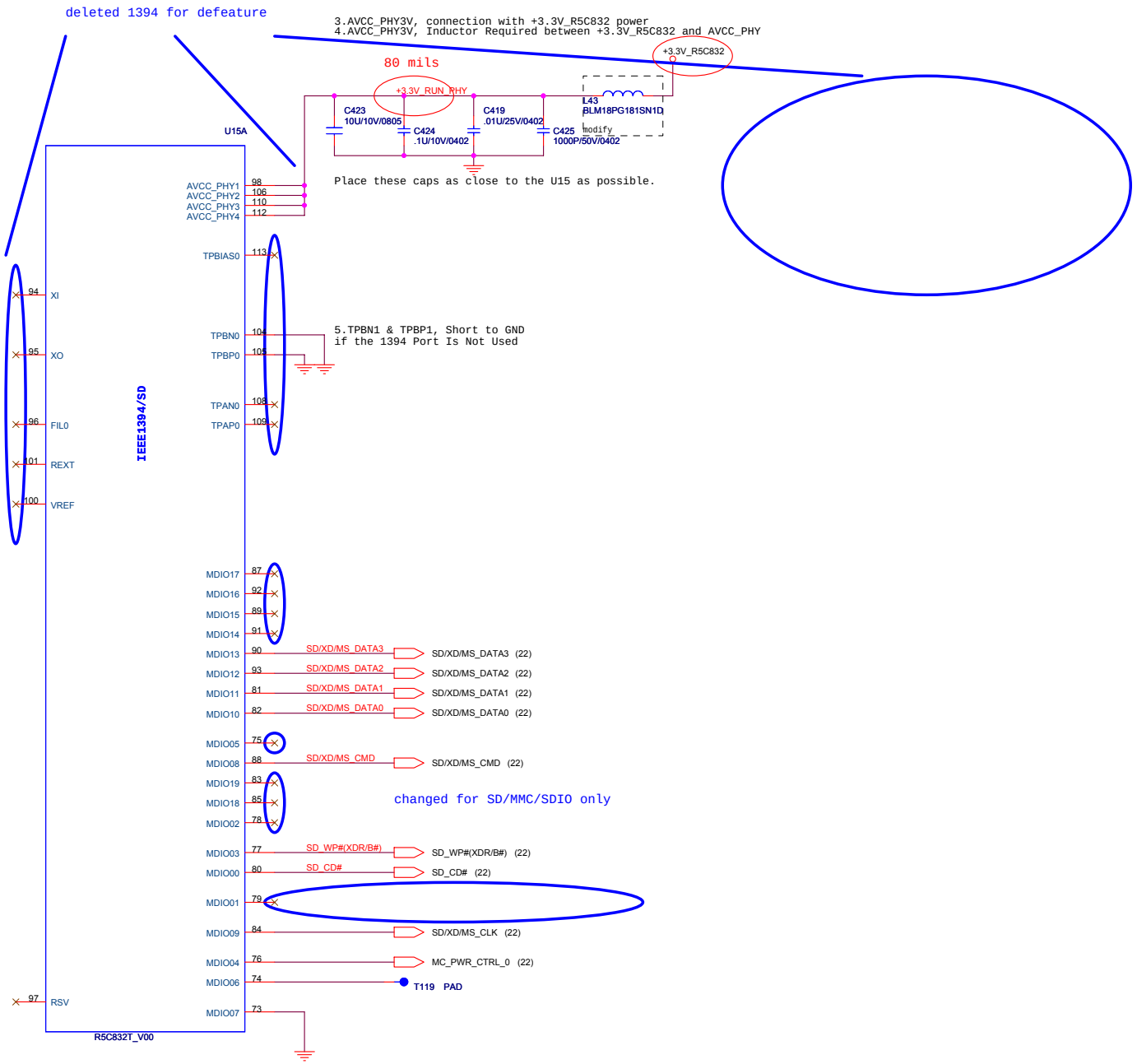

QUANTA COMPUTER

Title	CARD READER	
Size	Document Number FX2	Rev 1A
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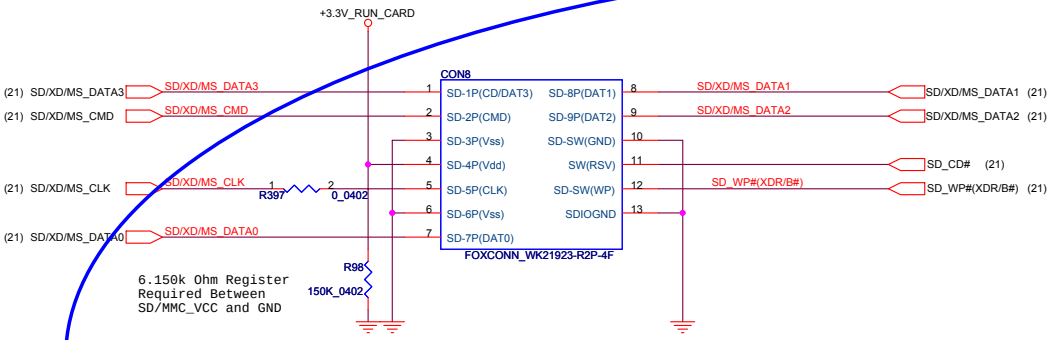
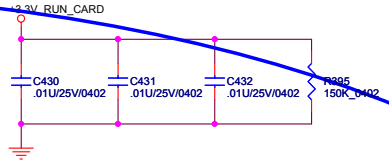
DO NOT INSERT SD/MMC SIMULTANEOUSLY.

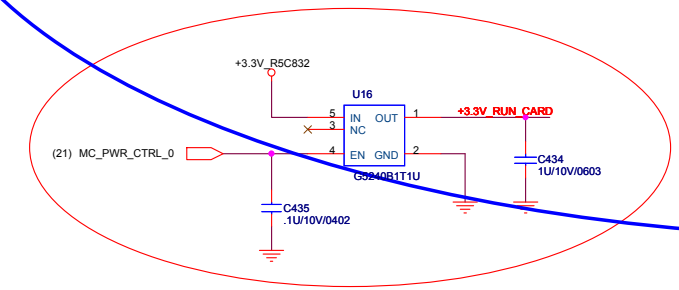
changed for SD/MMC/SDIO only





3 IN 1 CARD READER

For SD/MS power



QUANTA COMPUTER

Title	CARD READER CONN	
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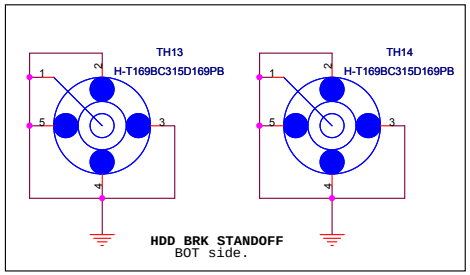
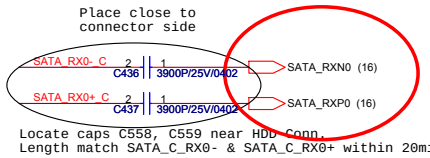
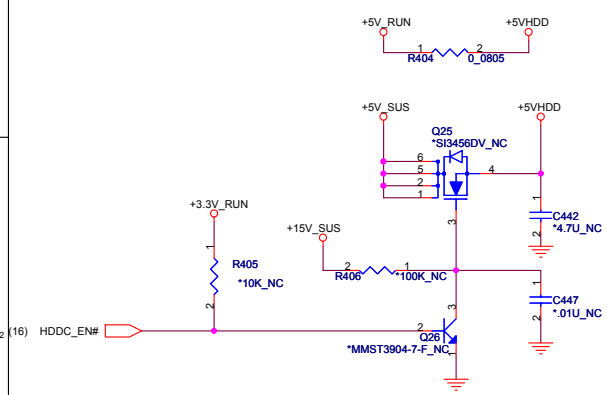
SATA HDD

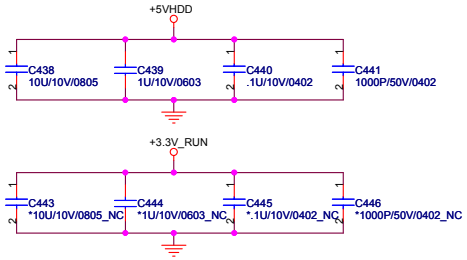


Place close to connector side

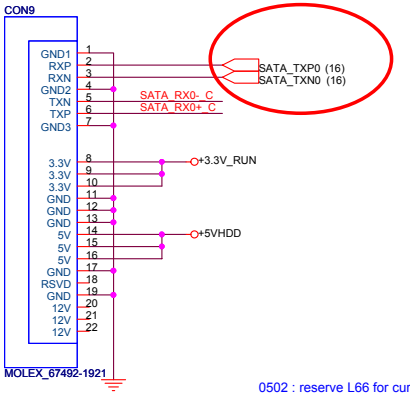


Locate caps C558, C559 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 20mils.



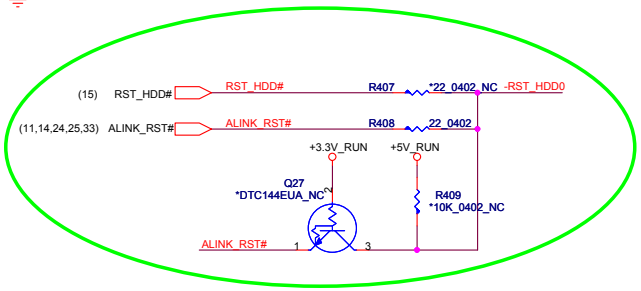


Place closed to HDD connector



SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.



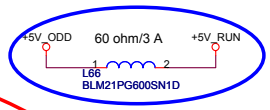
change name for ED5

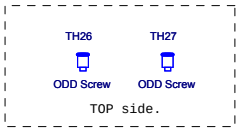
copy ED5 to FX2

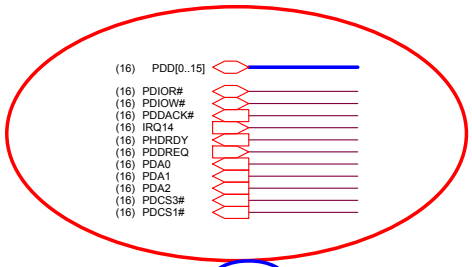
Waiting to check

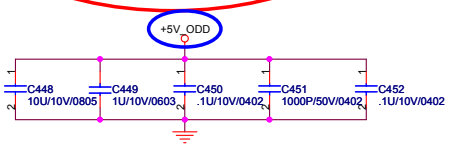
PATA ODD

0502 : reserve L66 for current measurement , can be removed and short directly after RTS ; and change +5V_RUN to +5V_ODD for ODD side power

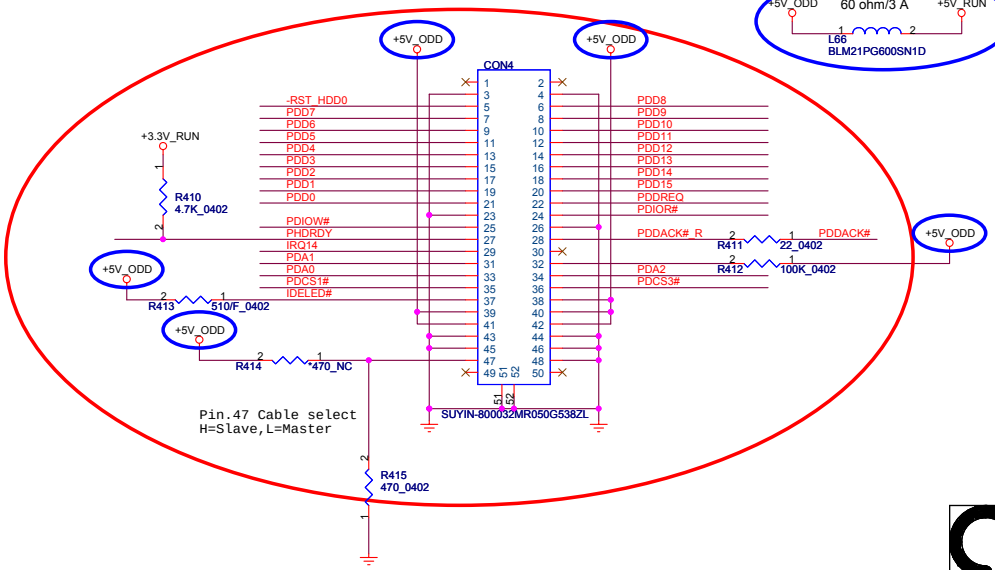








Place closed to MOD connector



Pin.47 Cable select
H=Slave,L=Master

QUANTA COMPUTER

Title	SATA HDD & PATA ODD	
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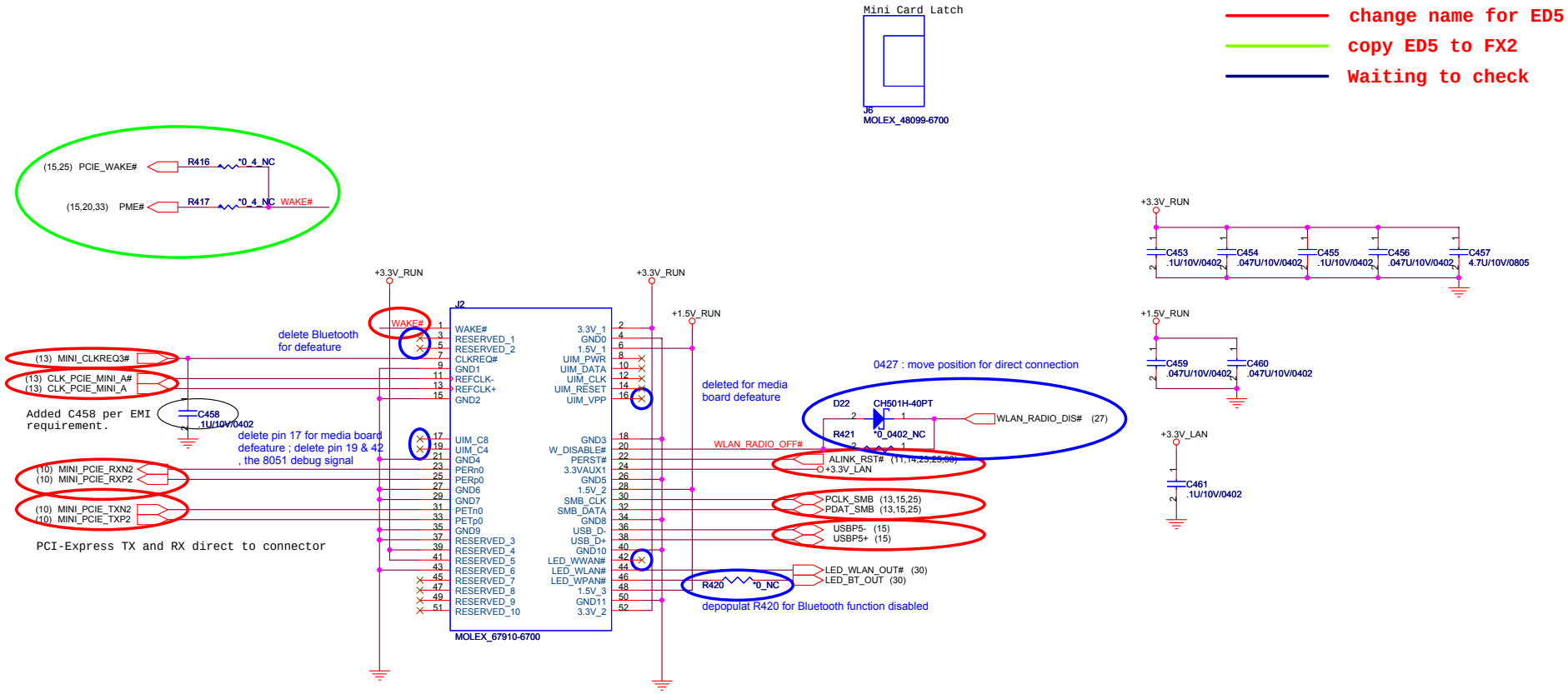
MINI CARD



QUANTA COMPUTER

Title	MINI Card	
Size	Document Number FX2	Rev 1A
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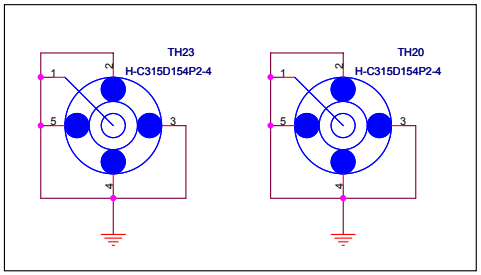
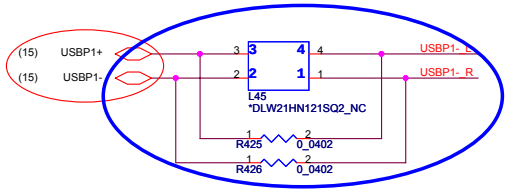
Express Card

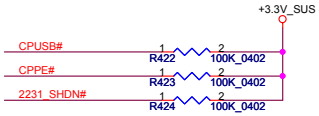


change name for ED5
copy ED5 to FX2
Waiting to check

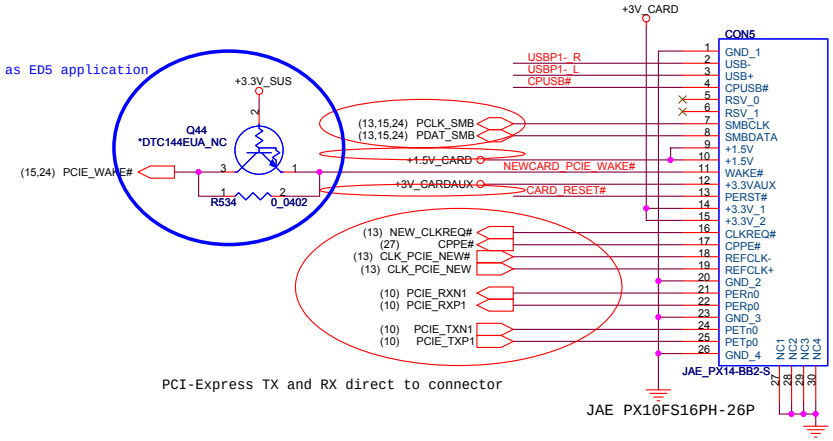
NEW CARD GUIDE POST
TOP side.

swap traces as "fx2_swap-0412"





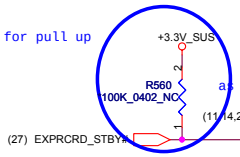
as ED5 application



PCI-Express TX and RX direct to connector

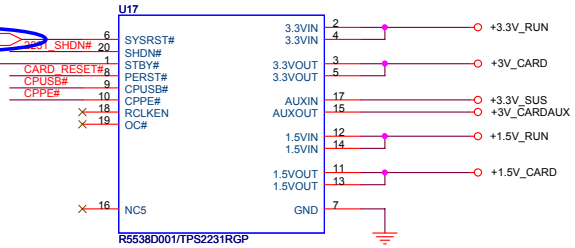
JAE PX10FS16PH-26P

reserve for pull up

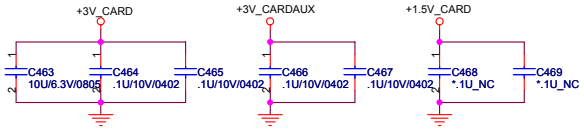


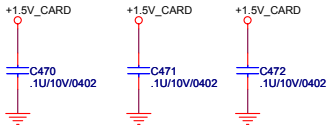
as ED5 application

+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

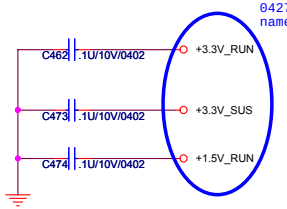


+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA





0427 : change from only net name to symbol "power point"



QUANTA COMPUTER

Title	Express Card	
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MDC INTERFACE

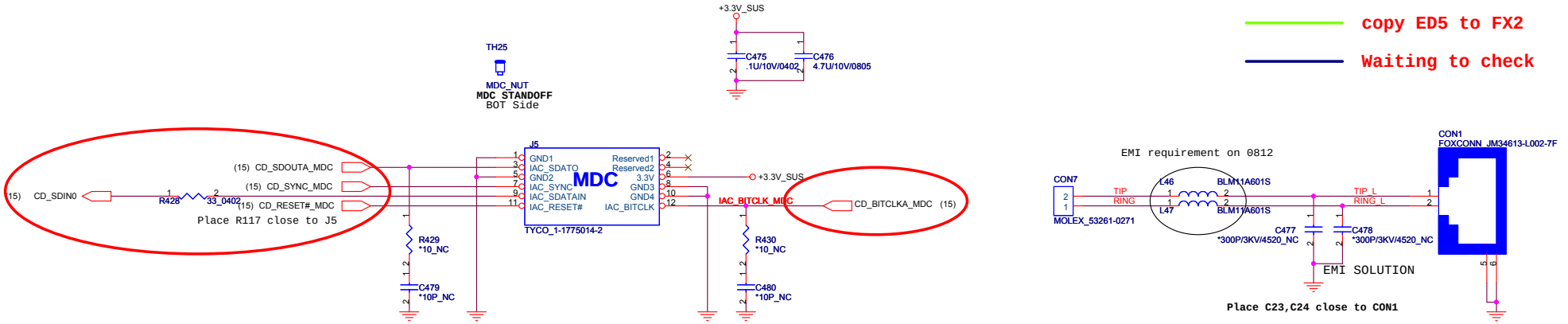
MDC Layout Notes

1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG
(stranded or twisted pair wire)

change name for ED5

copy ED5 to FX2

Waiting to check



delete Bluetooth
for defeature

QUANTA COMPUTER

Title	MDC CONN
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Date:	Friday, May 05, 2006
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EC pin updated as "FX2 KBC GPIO define v14"

add R468 for +3.3_SRC & R516 connected to +3.3V_ALW as power concern about the leakage; create +3.3V_97551.

delete pull up circuit of BT_PWERON#

+3.3V_SRC to +3.3V_97551

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

delete pull up circuit of RF_SW#, TV_SENSE#_D, MONITOR_PLUG#

SHBM=1: Enable shared memory with host BIOS

0502 : added as Loki's suggestion

modify for thermal protect

0427 : change from BREATH_LED to BREATH_LED#

as FM1

Instant on power switch input only

PBAT_SMBCLK/DAT : Charger, Battery
MBCLK/DATA : LCD, Password, CPU internal thermal diode

+3.3V_SRC to +3.3V_97551

U21
ST Micro M29W008AB/AMD-29LV081B/SST39VF080

delete PLCC32 connector

delete HWPG_1.8V

FOR 97551 ONLY

DIRECTLY 50 mS

HWPG_591 ===> NB_PWRGD ===> EC_PWRGD
NORTH BRIDGE SOUTH BRIDGE

EC & FALSH ROM

QUANTA COMPUTER

Title	PC97551 & FLASH	
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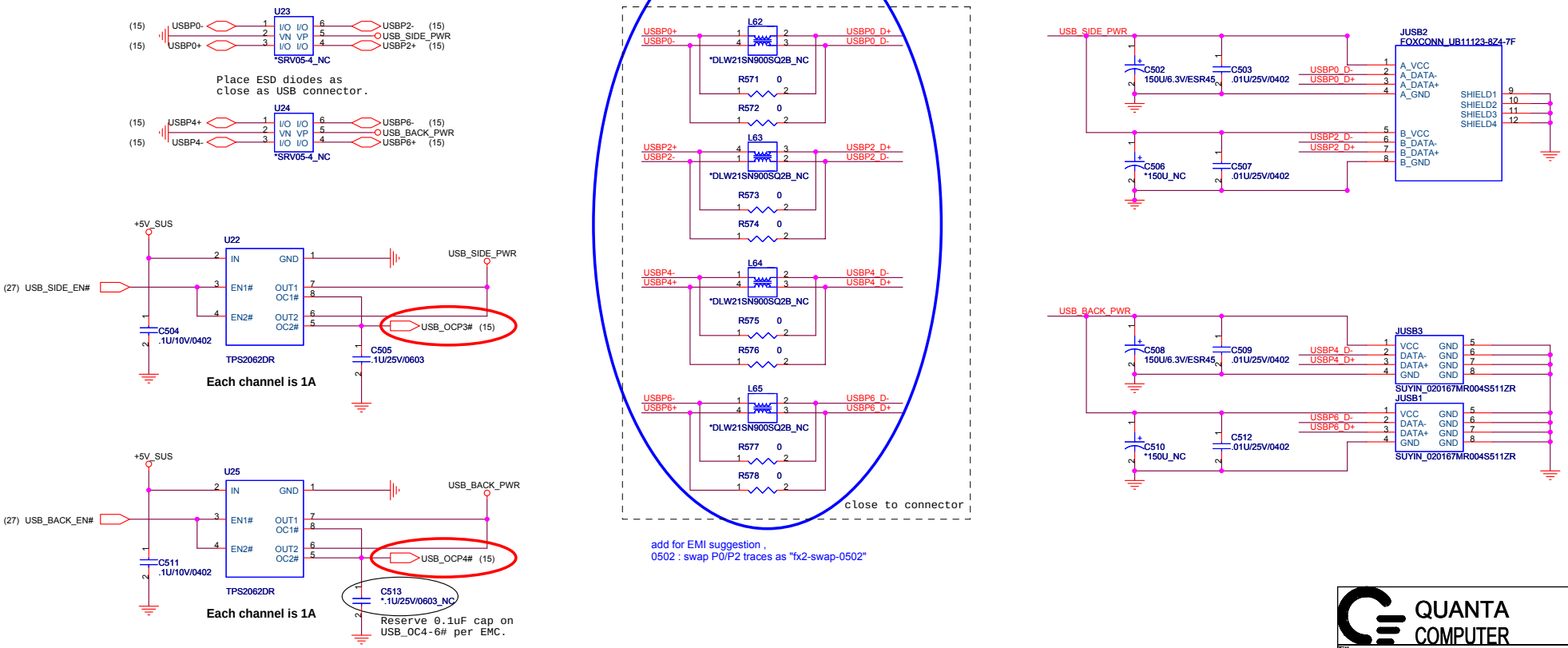
change name for ED5

copy ED5 to FX2

Waiting to check

8Mbit (1M Byte), SPI



QUANTA COMPUTER

Title	USB	
Size	Document Number FX2	Rev 1A
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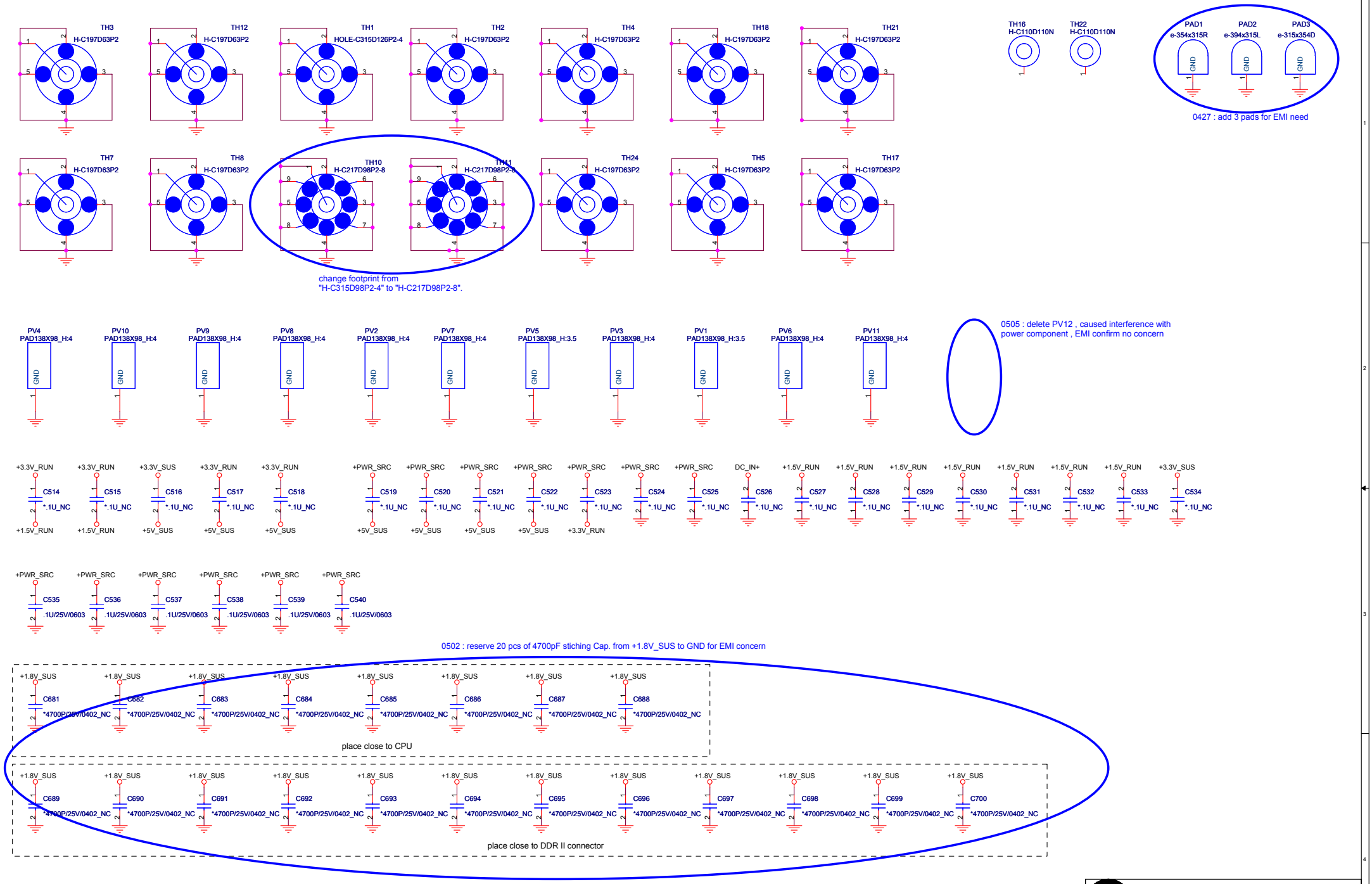

QUANTA COMPUTER

Title	EMI & Screw hole	
Size	Document Number FX2	Rev 1A
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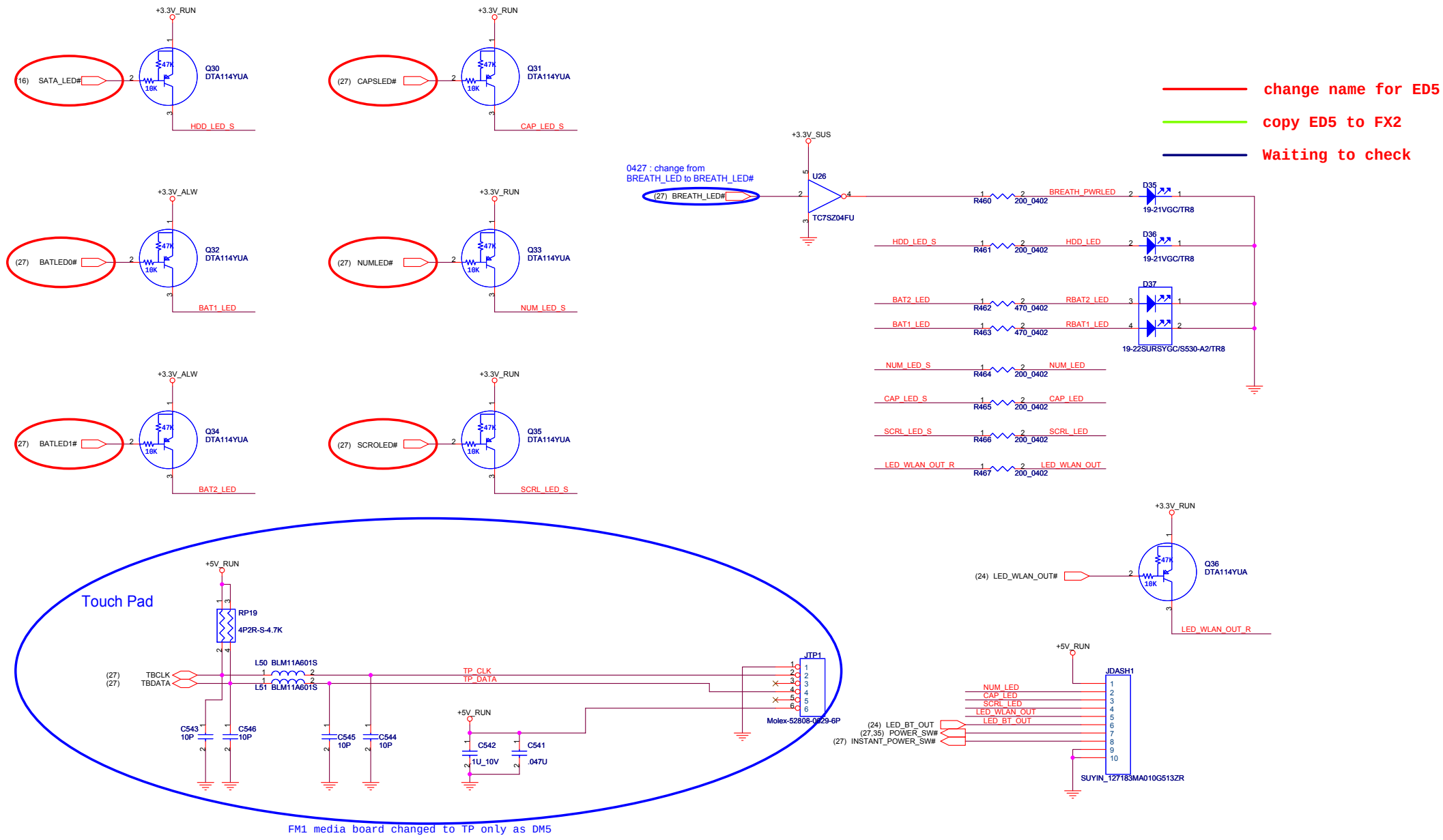

FM1 media board changed to TP only as DM5

QUANTA COMPUTER

Title	SWITCH & TP & LED	
Size	Document Number FX2	Rev 1A
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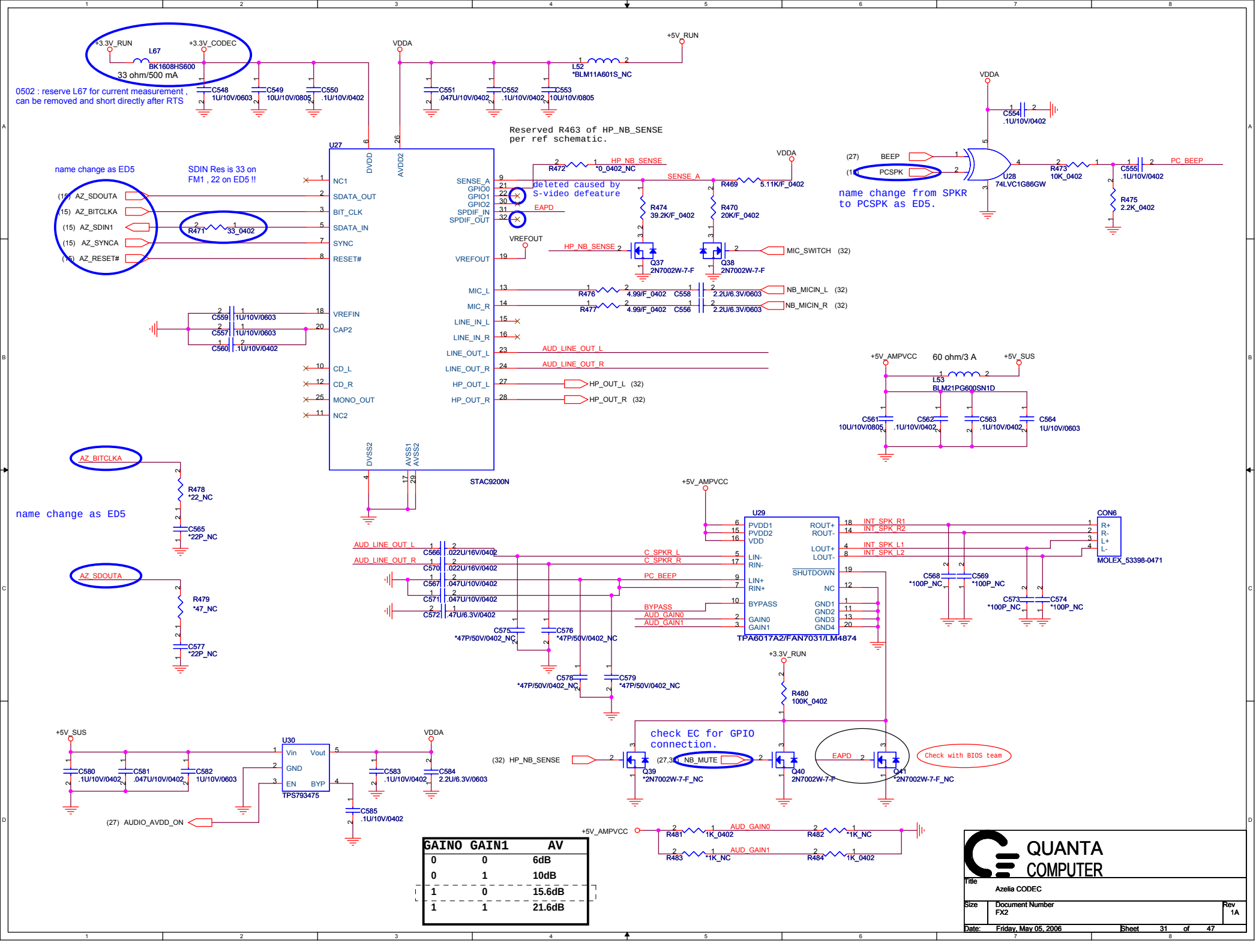
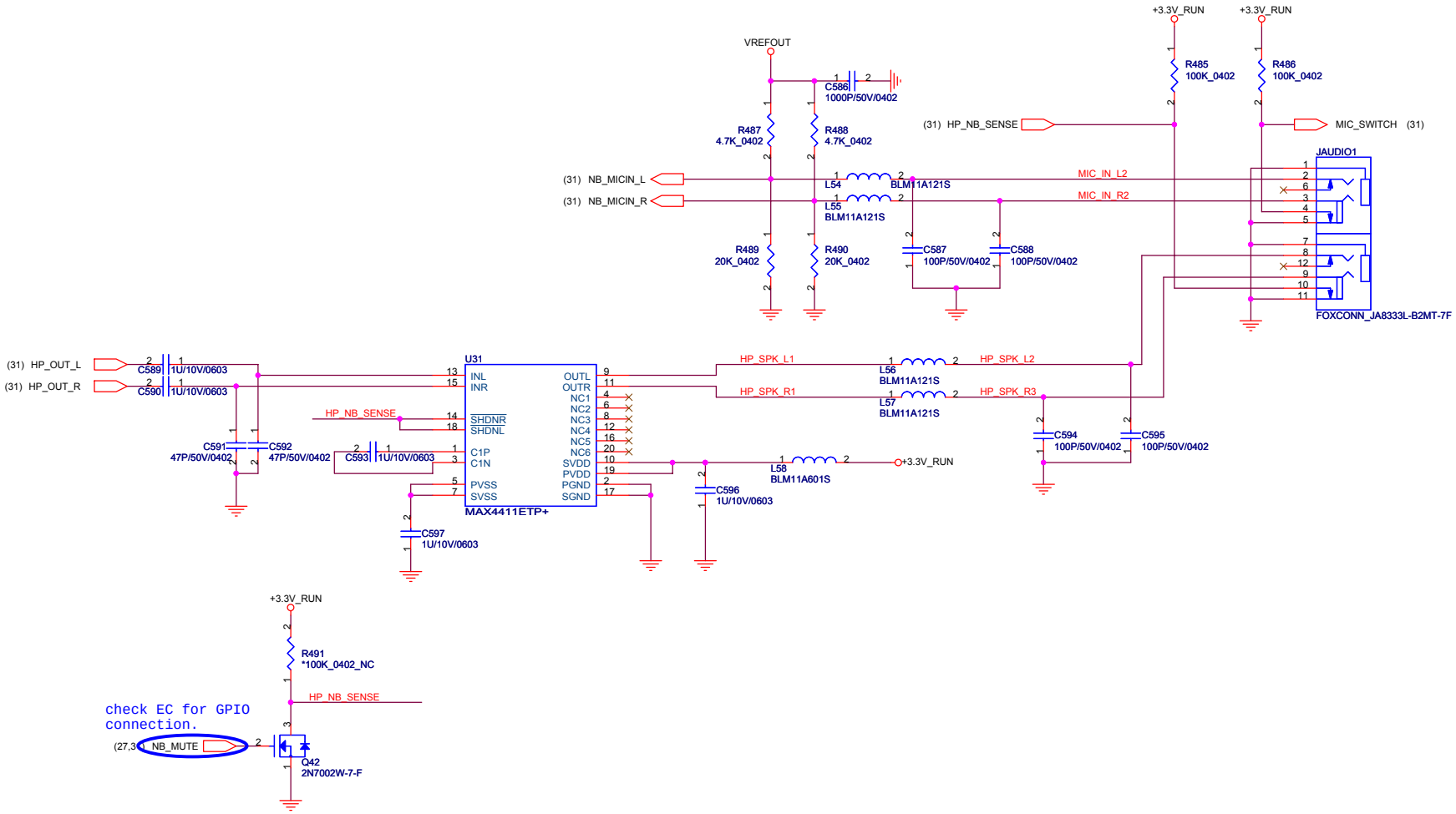


GAINO	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



QUANTA COMPUTER

Title	AUDIO CONN	
Size	Document Number FX2	Rev 1A
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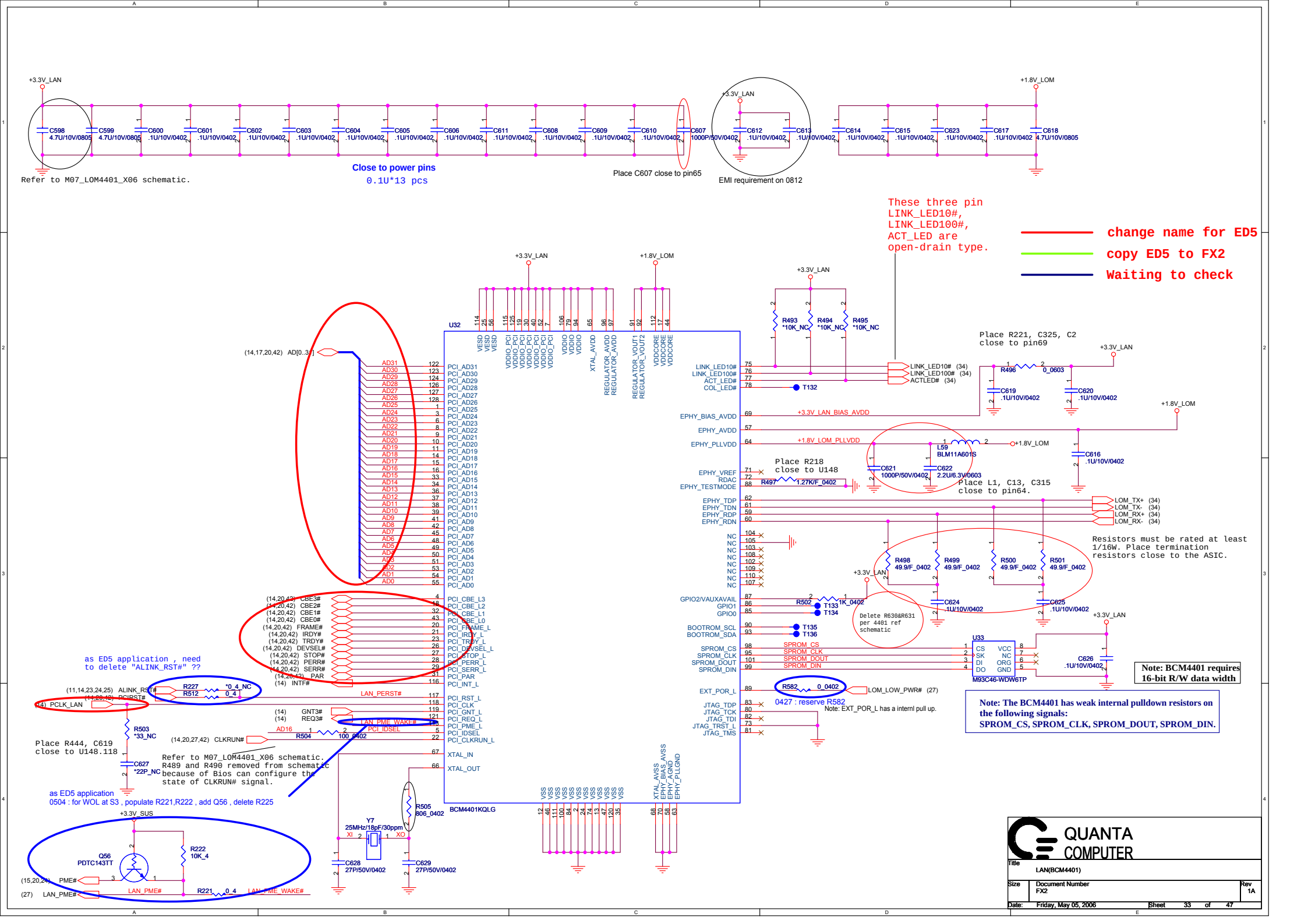
+3.3V_LAN
C598 4.7U/10V/0805
C599 4.7U/10V/0805
C600 .1U/10V/0402
C601 .1U/10V/0402
C602 .1U/10V/0402
C603 .1U/10V/0402
C604 .1U/10V/0402
C605 .1U/10V/0402
C606 .1U/10V/0402
C611 .1U/10V/0402
C608 .1U/10V/0402
C609 .1U/10V/0402
C610 .1U/10V/0402
C607 1000P/50V/0402
Refer to M07_LOM4401_X06 schematic.
Close to power pins
0.1U*13 pcs
Place C607 close to pin65
C612 .1U/10V/0402
C613 .1U/10V/0402
EMI requirement on 0812
+1.8V_LOM
C614 .1U/10V/0402
C615 .1U/10V/0402
C623 .1U/10V/0402
C617 .1U/10V/0402
C618 4.7U/10V/0805
These three pin LINK_LED10#, LINK_LED100#, ACT_LED are open-drain type.
change name for ED5
copy ED5 to FX2
Waiting to check
U32
BCM4401KQLG
R493 *10K_NC
R494 *10K_NC
R495 *10K_NC
Place R221, C325, C2 close to pin69
R496 0_0603
C619 .1U/10V/0402
C620 .1U/10V/0402
L59 BLM11A601S
C616 .1U/10V/0402
C621 1000P/50V/0402
C622 2.2U/6.3V/0603
Place R218 close to U148
R497 1.27K/F_0402
Place L1, C13, C315 close to pin64.
Resistors must be rated at least 1/16W. Place termination resistors close to the ASIC.
R498 49.9/F_0402
R499 49.9/F_0402
R500 49.9/F_0402
R501 49.9/F_0402
C624 .1U/10V/0402
C625 .1U/10V/0402
R502 1K_0402
Delete R630&R631 per 4401 ref schematic
U33
M93C46-WDW6TP
C626 .1U/10V/0402
Note: BCM4401 requires 16-bit R/W data width
R582 0_0402
0427 : reserve R582
Note: EXT_POR_L has a internl pull up.
Note: The BCM4401 has weak internal pulldown resistors on the following signals: SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.
as ED5 application , need to delete "ALINK_RST#" ??
R227 *0_4_NC
R512 0_4
R503 *33_NC
Place R444, C619 close to U148.118
C627 *22P_NC
R504 100_0402
Refer to M07_LOM4401_X06 schematic. R489 and R490 removed from schematic because of Bios can configure the state of CLKRUN# signal.
as ED5 application
0504 : for WOL at S3 , populate R221,R222 , add Q56 , delete R225
+3.3V_SUS
Q56 PDTC143TT
R222 10K_4
R221 0_4
Y7 25MHz/18pF/30ppm
R505 806_0402
C628 27P/50V/0402
C629 27P/50V/0402
QUANTA COMPUTER
Title LAN(BCM4401)
Size Document Number FX2
Rev 1A
Date: Friday, May 05, 2006
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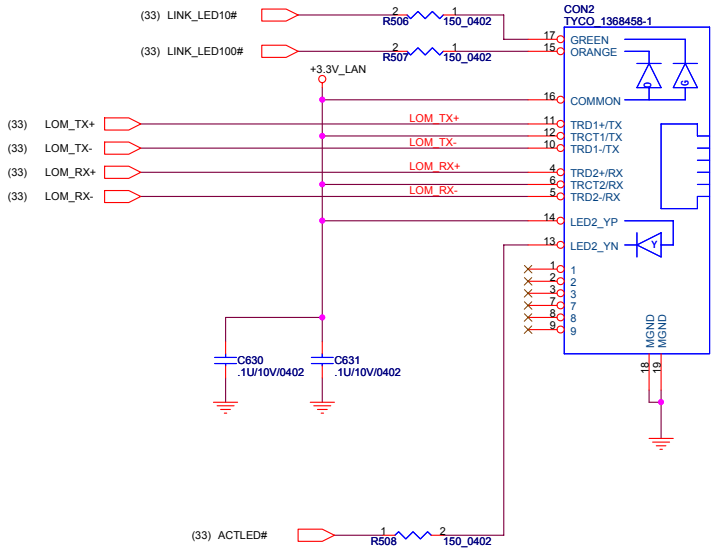
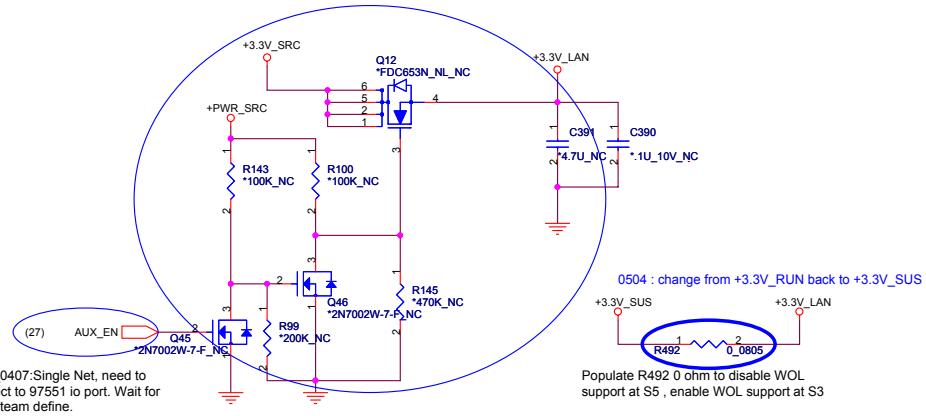


change name for ED5

copy ED5 to FX2

Waiting to check

copy DM5 to FX2



Cory_0407:Single Net, need to connect to 97551 io port. Wait for BIOS team define.

0504 : change from +3.3V_RUN back to +3.3V_SUS

Populate R492 0 ohm to disable WOL support at S5 , enable WOL support at S3

LAN POWER

QUANTA COMPUTER

Title	LAN JACK	
Size	Document Number FX2	Rev 1A
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add Thermal IC as FM1

H_THERMDA&h_THERMDC
trace routing = W:10/S:10

(5) CPU_TEST4_THERMDA
(5) CPU_TEST5_THERMDC

+3.3V_SUS
R536 7.5K/F_0402

(18,27) MBDATA
(18,27) MBCLK

U36
EMC4000

SMDATA
SMBCLK
LDO_SHDN#_ADDR
DP2
DN2
+3V_SUS
VSUS_PWRGD
+RTC_PWR3V
+3V_PWROK#
POWER_SW#
THERMTRIP1#
THERMTRIP2#
THERMTRIP3#
VSET
HW_LOCK#
VSS
FAN_DAC
FAN_OUT
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
ATF_INT#
VCP1
VCP2
LDO_POK
DN1
DP1
THERMTRIP_SIO
ACAvail_Clr
SYS_SHDN#
VDD_5V
LDO_OUT
LDO_OUT
LDO_IN
LDO_IN
DP3
DN3
LDO_SET

Place C653 close to U36
C653 2200P/50V/0402

+3.3V_SUS
R537 49.9/F_0402
+3VSUS_THRM
C655 .1U/10V/0402

VCCRTC
C658 .1U/10V/0402

SUSPWROK
R539 1K_0402
EC_PWRGD#
R540 1K_0402
(27,30) POWER_SW#
THERMTRIP1#

+3.3V_SUS
R554 10K_0402
C663 .1U/10V/0402
R542 147K/F_0402
R543 41.2K_0402
C664 2200P/50V/0402
R544 1K_0402
VSET
HW_LOCK#
FAN1_VOUT

Notes:
Vset=(Tp-70)/21
3.3*(R543/R542+R543)=(Tp-70)/21
Where Tp=70 to 101 degree C
Set trip point=85 degree C
Vset = (85-75)/16= 0.625 V
Guardian II temp-tolerance= +/-3 degree C

+3.3V_SUS
R552 10K_0402
ATF_INT# (27)

delete single net "VCP1" & "VCP2"

R55310K_0402
+3.3V_RUN

Place Q50 at bottom of CPU
REM_DIODE1_N & REM_DIODE1_P trace routing = W:10/S:10
REM_DIODE1_N
REM_DIODE1_P
Place C656 close to the pins as possible.
C656 2200P/50V/0402
Q50 MMST3904-7-F
C657 *2200P_NC
Place C657 close to the Q50

R541 10K_0402
+3.3V_ALW
THERMTRIP_SIO (27)
ACAV_IN (27,36)
R555 *10K_0402_NC
THERM_SYS_PWR# (27,38)
VCCRTC
+5V_RUN
+2.5V_RUN
R545 0_1210
+3.3V_RUN_IN
+3.3V_RUN

REM_DIODE3_N & REM_DIODE3_P trace routing = W:10/S:10
REM_DIODE3_P
REM_DIODE3_N
LDO_SET
C668 2200P/50V/0402
Q51 MMST3904-7-F
C669 *2200P_NC
Place C669 close to Q51
Place C668 close to U36
Place Q51 Near the SO-DIMM.

+3.3V_RUN
R535 10K_0402
FAN1_TACH (27)
R538 0_0402
FAN1
FAN1_VOUT
FAN1_TACH_FB
D39 *CH751H-40HPT_NC
C654 22U/10V/1206
J3
VCC
SIG
GND
MOLEX_53398-0371

+5V_RUN
C659 10U/10V/0805
C660 .1U/10V/0402
+2.5V_RUN
C661 10U/10V/0805
C662 .1U/10V/0402
Place C659~C662, C665~C667, close to U36

+3.3V_RUN_IN
C665 1U/10V/0603
C666 .1U/10V/0402
C667 *10U_NC

+3.3V_SUS
R546 100K_0402
EC_PWRGD#
(14,15,27) EC_PWRGD
Q52 2N7002W-7-F

+3.3V_SUS
R547 8.2K_0402
VLDT_RUN
THERMTRIP1#
R549 2.2K_0402
Q53 MMST3904-7-F
C670 .1U/10V/0402
(5) H_THERMTRIP#
C670 needs to be placed near Guardian IC.

+2.5V_RUN
R548 *31.5K_NC
LDO_SET
R550 1K_0603
Voltage margining circuit for LDO output.
For Vmargin, stuff R548 and R550=30K.
R550=1K for production

as FM1 keyboard matrix & "e0788.1104a_swap-0422"

JKB1
HRS_FH28D-50(25)SB-1SH(86)

(27) MY9
(27) MY10
(27) MY8
(27) MY13
(27) MY12
(27) MY14
(27) MY15
(27) MY11
(27) MY0
(27) MY2
(27) MY1
(27) MY3
(27) MY7
(27) MY5
(27) MY6
(27) MY4
(27) MY16
(27) MX7
(27) MX4
(27) MX6
(27) MX2
(27) MX5
(27) MX3
(27) MX1
(27) MX0

+3.3V_SUS
RP20 10KX8
MX0 MX1 MX3 MX5
MX7 MX4 MX6 MX2
RP21 10KX8
MY16 MY4 MY6 MY5
MY2 MY1 MY3 MY7
RP22 10KX8
MY0 MY11 MY15 MY14
MY10 MY8 MY13 MY12

CA1 *220PX4_NC
CA2 *220PX4_NC
CA3 *220PX4_NC
CA4 *220PX4_NC
CA5 *220PX4_NC
CA6 *220PX4_NC

+3.3V_SUS
R513 10K_0402
MY9
C638 *220P/50V/0402_NC

KBC

wait to discuss !!

(27,38,39,40) SUSON
+1.8V_SUS
+3.3V_ALW
+3.3V_SUS
R557 10K_0402
R556 100K_0402
Q54 3904
C672 1U/50V/0603
U38 TC7SZ04FU
C671 *.047U_NC
U39 TC7SZ08FU
SUSPWROK

0427 : change Q54 from 2N7002W-7-F to 3904 ; C672 from .1U/10V/0402 to .1U/50V/0603 as voltage level & timing concern

QUANTA COMPUTER

Title	KB & THERMAL & FAN	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 35 of 47	

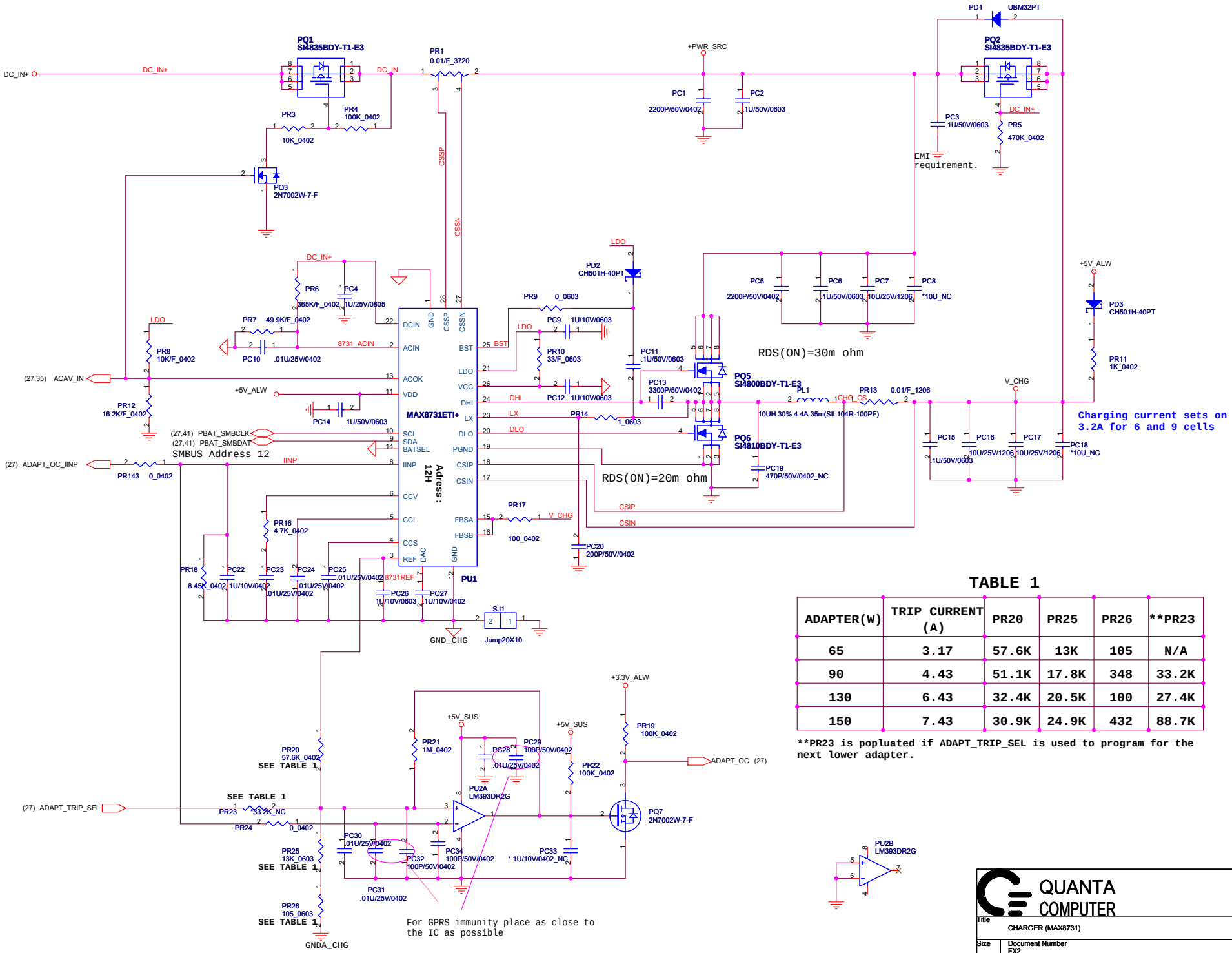


TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR20	PR25	PR26	**PR23
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K

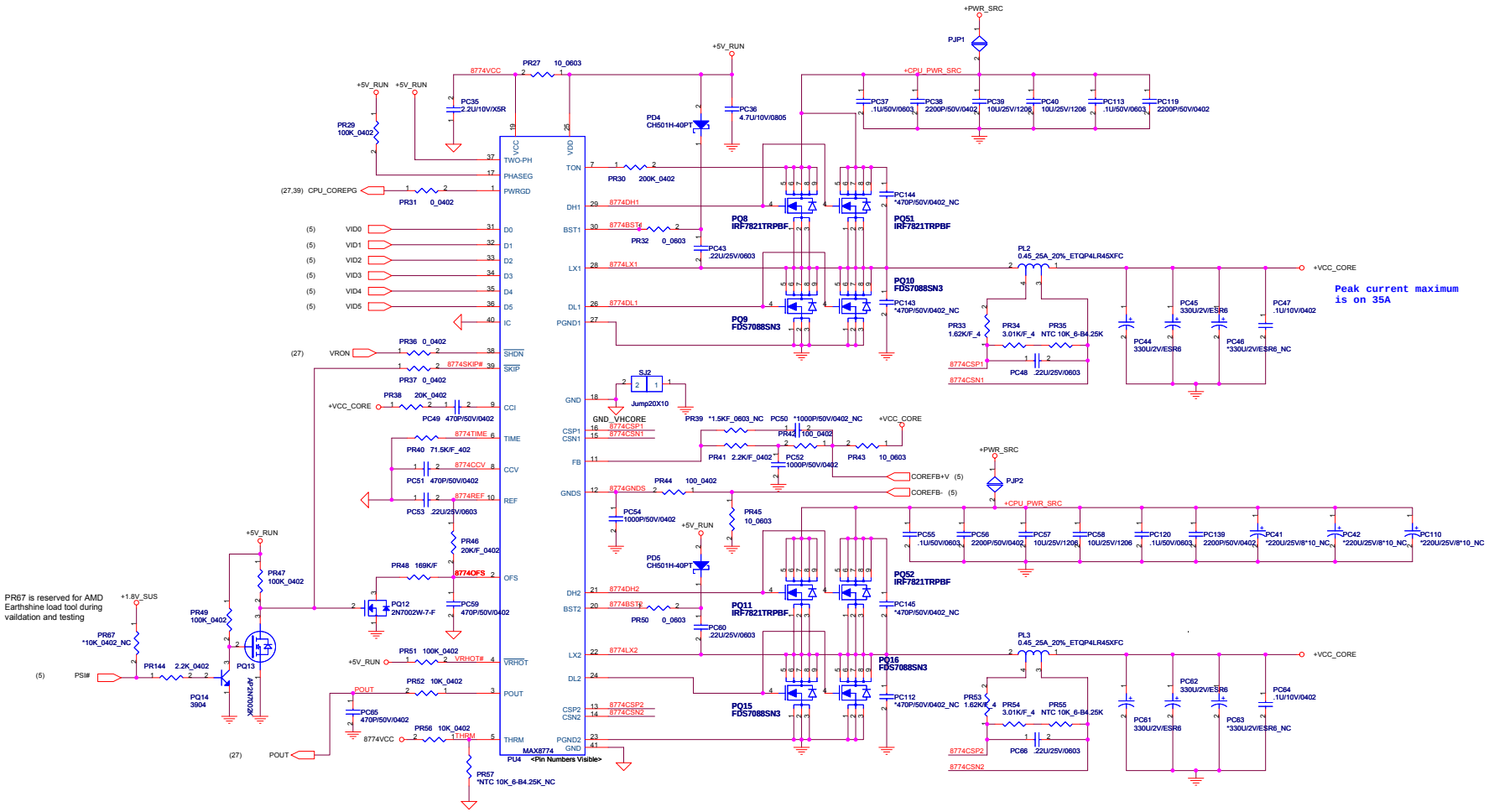
**PR23 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

QUANTA COMPUTER

Title: CHARGER (MAX8731)

Size | Document Number: FX2 | Rev: 1A

Date: 2005/4/21 | Sheet 36 of 47

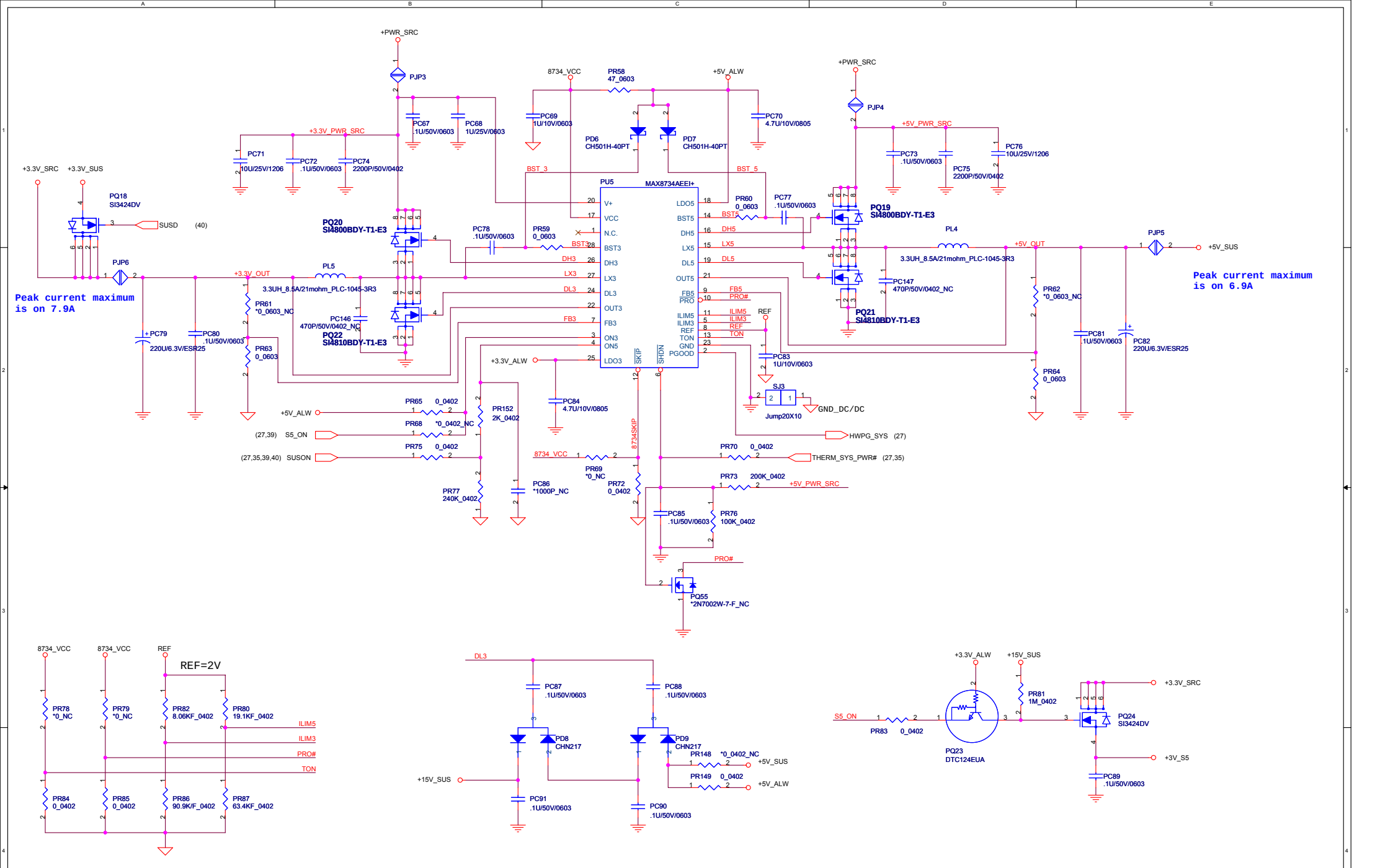


D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V
0	0	0	0	0	1	1.5250V
0	0	0	0	1	0	1.5000V
0	0	0	0	1	1	1.4750V
0	0	0	1	0	0	1.4500V
0	0	0	1	0	1	1.4250V
0	0	0	1	1	0	1.4000V
0	0	0	1	1	1	1.3750V
0	0	1	0	0	0	1.3500V
0	0	1	0	0	1	1.3250V
0	0	1	0	1	0	1.3000V
0	0	1	0	1	1	1.2750V
0	0	1	1	0	0	1.2500V
0	0	1	1	0	1	1.2250V
0	0	1	1	1	0	1.2000V
0	0	1	1	1	1	1.1750V
0	1	0	0	0	0	1.1500V
0	1	0	0	0	1	1.1250V
0	1	0	0	1	0	1.1000V
0	1	0	0	1	1	1.0750V
0	1	0	1	0	0	1.0500V
0	1	0	1	0	1	1.0250V
0	1	0	1	1	0	1.0000V
0	1	0	1	1	1	0.9750V
0	1	1	0	0	0	0.9500V
0	1	1	0	0	1	0.9250V
0	1	1	0	1	0	0.9000V
0	1	1	0	1	1	0.8750V
0	1	1	1	0	0	0.8500V
0	1	1	1	0	1	0.8250V
0	1	1	1	1	0	0.8000V
0	1	1	1	1	1	0.7750V

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	0.7625V
1	0	0	0	0	1	0.7500V
1	0	0	0	1	0	0.7375V
1	0	0	0	1	1	0.7250V
1	0	0	1	0	0	0.7125V
1	0	0	1	0	1	0.7000V
1	0	0	1	1	0	0.6875V
1	0	0	1	1	1	0.6750V
1	0	1	0	0	0	0.6625V
1	0	1	0	0	1	0.6500V
1	0	1	0	1	0	0.6375V
1	0	1	0	1	1	0.6250V
1	0	1	1	0	0	0.6125V
1	0	1	1	0	1	0.6000V
1	0	1	1	1	0	0.5875V
1	0	1	1	1	1	0.5750V
1	1	0	0	0	0	0.5625V
1	1	0	0	0	1	0.5500V
1	1	0	0	1	0	0.5375V
1	1	0	0	1	1	0.5250V
1	1	0	1	0	0	0.5125V
1	1	0	1	0	1	0.5000V
1	1	0	1	1	0	0.4875V
1	1	0	1	1	1	0.4750V
1	1	1	0	0	0	0.4625V
1	1	1	0	0	1	0.4500V
1	1	1	0	1	0	0.4375V
1	1	1	0	1	1	0.4250V
1	1	1	1	0	0	0.4125V
1	1	1	1	0	1	0.4000V
1	1	1	1	1	0	0.3875V
1	1	1	1	1	1	0.3750V

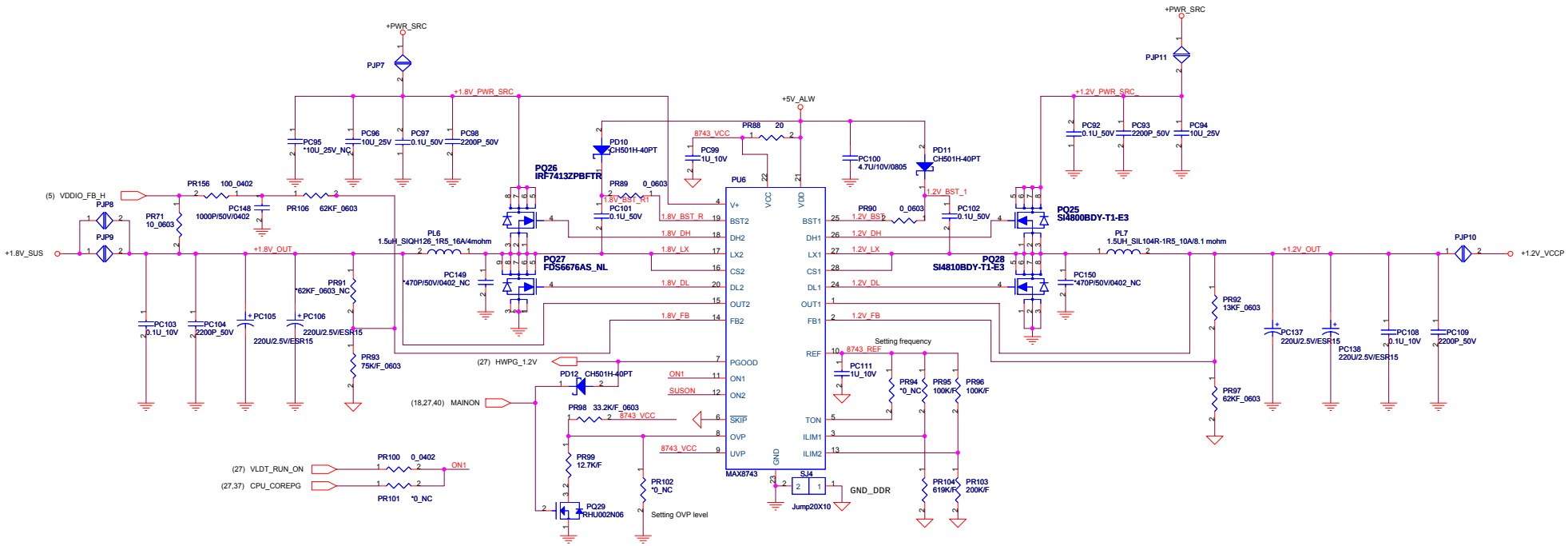
QUANTA COMPUTER

Title	VHCORE (MAX8774)	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 37 of 47	

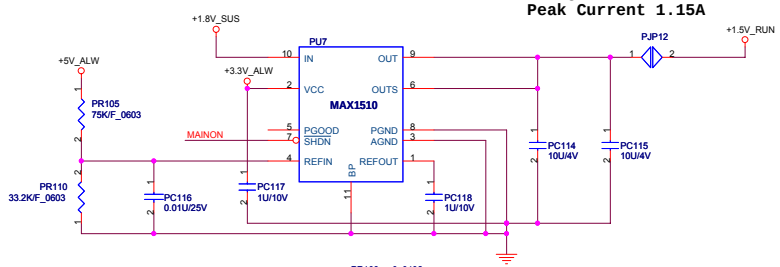


QUANTA COMPUTER

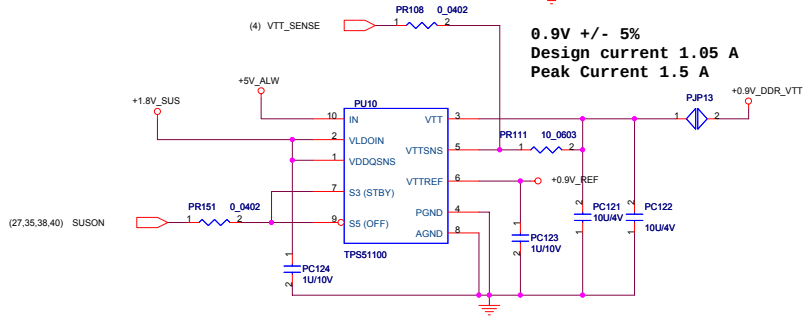
Title	SYSTEM (MAX8734)	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 38 of 47	

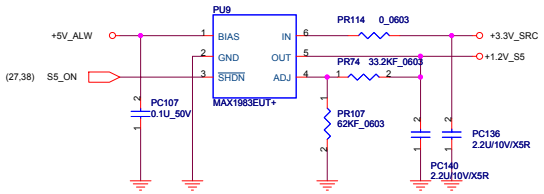


1.5 Volt +/- 5%
Design current 0.7A
Peak Current 1.15A



0.9V +/- 5%
Design current 1.05 A
Peak Current 1.5 A





QUANTA COMPUTER

Title	VCCP	
Size	Document Number FX2	Rev 1A
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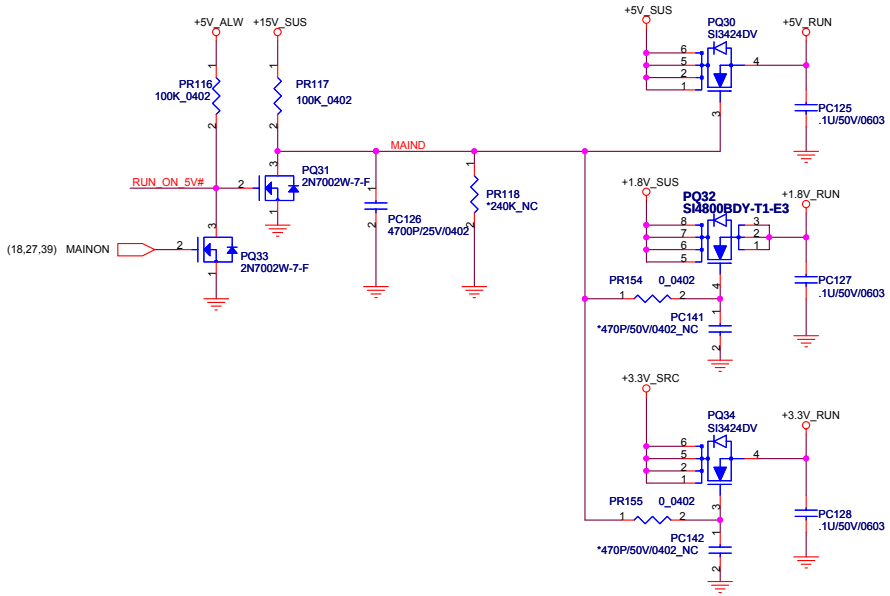
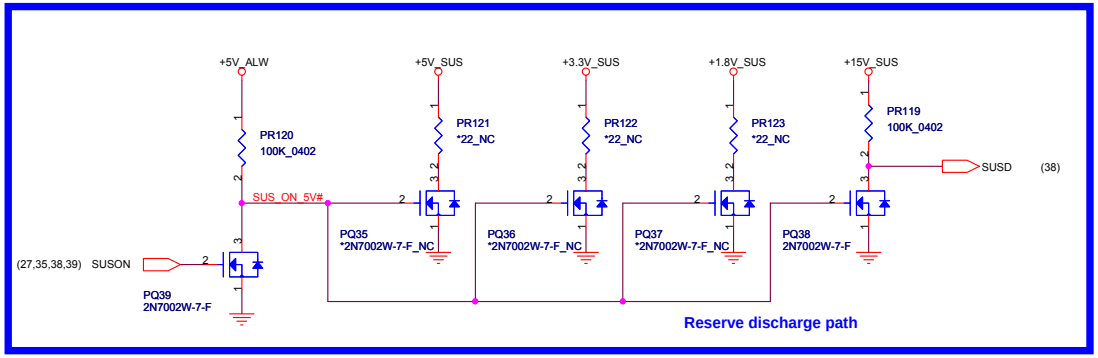
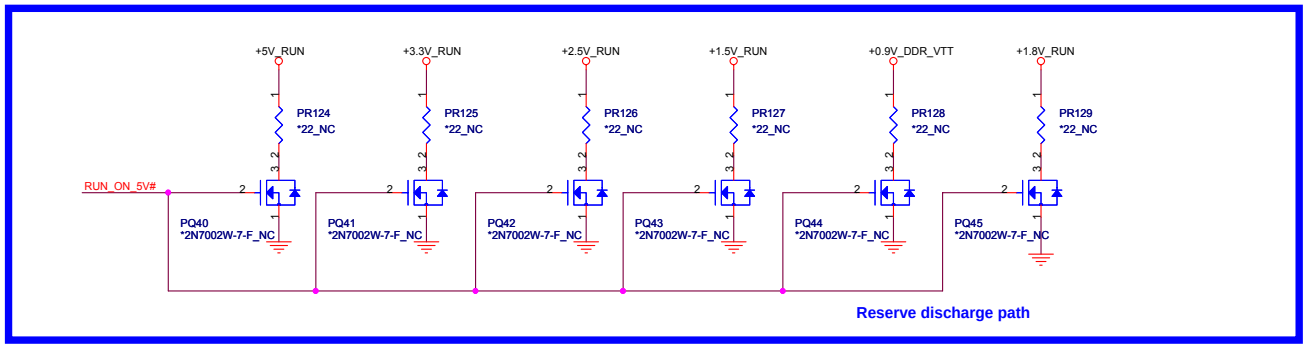
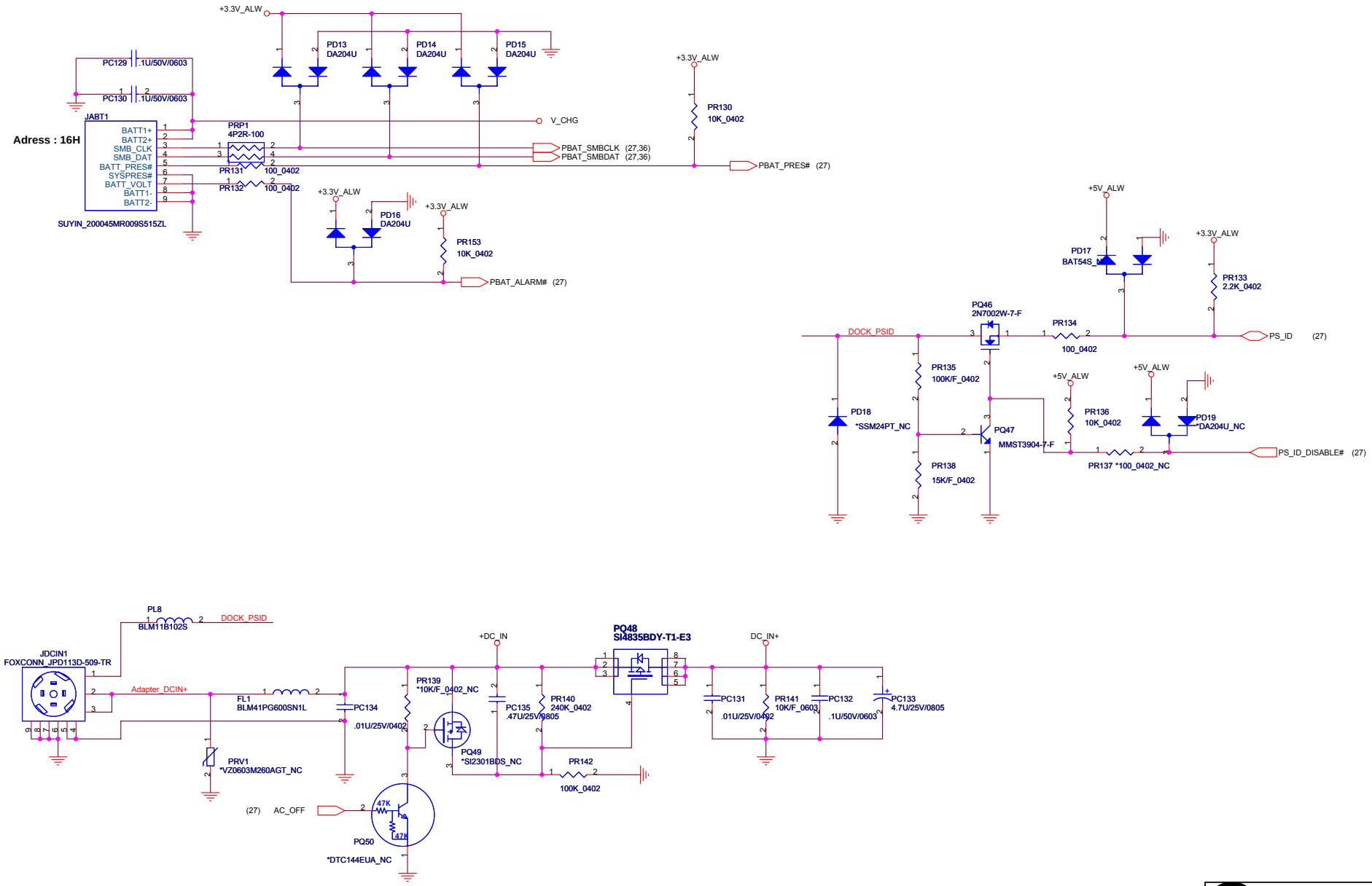






QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 40 of 47	

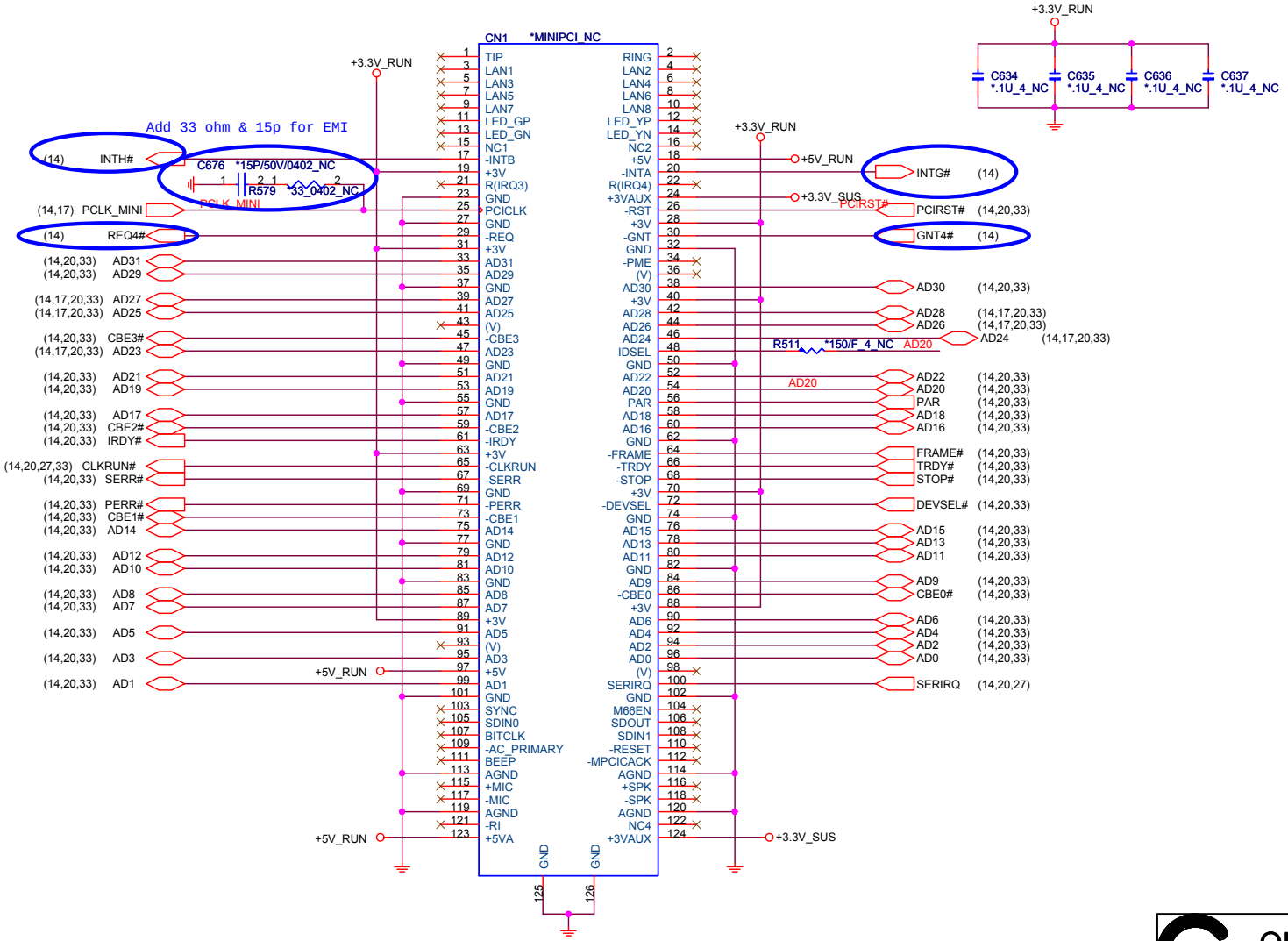


QUANTA COMPUTER

Title	DCIN,Batt	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 41 of 47	

ID Select : AD20
Interrupt Pin : INTG# , INTH#
Request Indicate : REQ4#
Grant Indicate : GNT4#

DEBUG PURPOSE ONLY



MPC

QUANTA COMPUTER

Title	MINI PCI(for debug)
Size	Document Number FX2
Rev	1A
Date:	Friday, May 05, 2006
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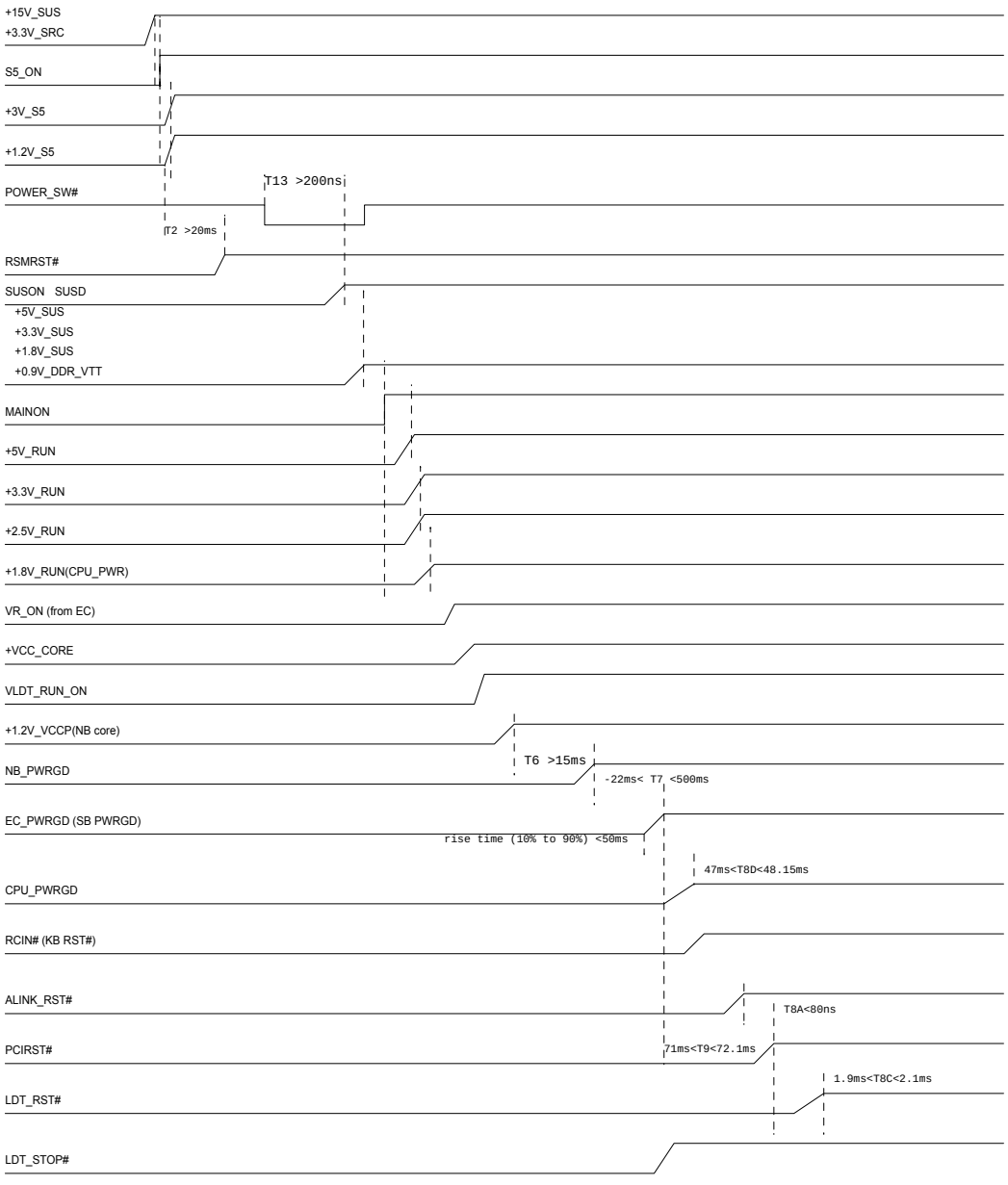
Power On Sequence

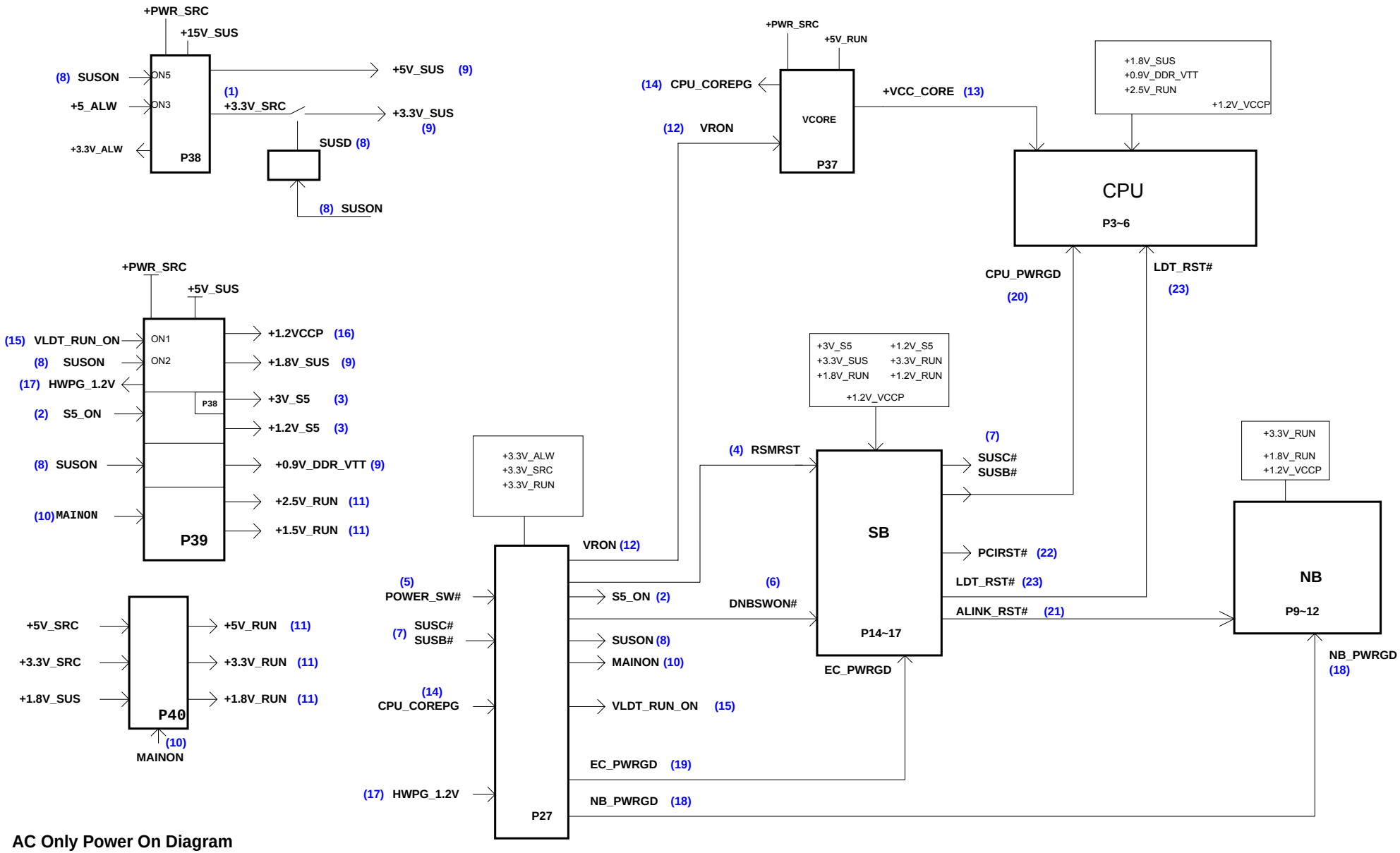


T6: NB core voltage to NB_PWRGD
T7: NB_PWRGD to SB_PWRGD
T8D: SB_PWRGD to CPU_PWRGD

T8A: ALINK_RST# to PCIRST#
T9: SB_PWRGD to PCIRST#
T8C: PCIRST# to LDT_RST#

QUANTA COMPUTER

Title	Power On Sequence	
Size	Document Number FX2	Rev 1A
Date: Wednesday, May 10, 2006	Sheet 43 of 47	

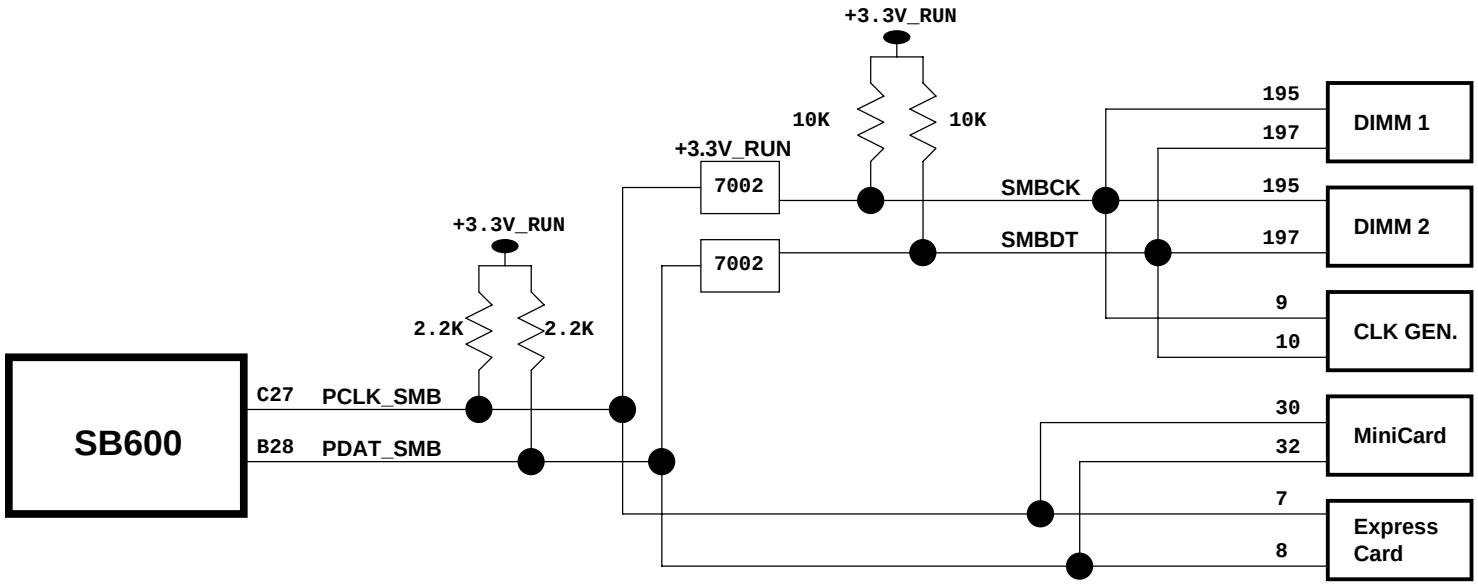


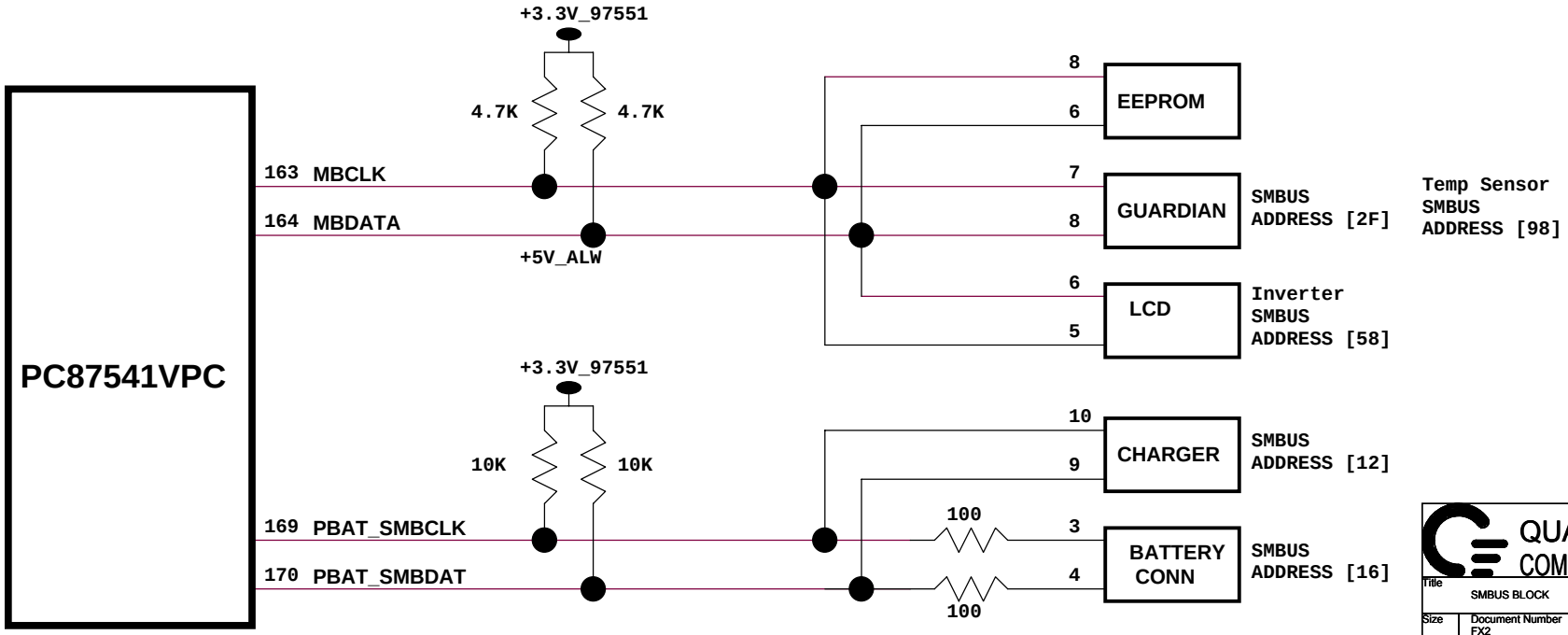
AC Only Power On Diagram

(1) +3.3V_SRC
(2) S5_ON
(3) +3V_S5, +1.2V_S5
(4) RSMRST
(5) POWER_SW#
(6) DNBSWON#
(7) SUSC#, SUSB#
(8) SUSON, SUSD
(9) +5V_SUS
+0.9V_DDR_VTT, +3.3V_SUS, +1.8V_SUS
(10) MAINON
(11) +5V_RUN, +3.3V_RUN
+2.5V_RUN, +1.8V_RUN, +1.5V_RUN
(12) VRON
(13) +VCC_CORE
(14) CPU_COREPG
(15) VLDT_RUN_ON
(16) +1.2_VCCP
(17) HWPG_1.2V
(18) NB_PWRGD
(19) EC_PWRGD
(20) CPU_PWRGD
(21) ALINK_RST#
(22) PCI_RST#
(23) LDT_RST#

QUANTA COMPUTER

Title	Power On Diagram	
Size	Document Number FX2	Rev 1A
Date: Thursday, May 04, 2006	Sheet 44 of 47	





QUANTA COMPUTER

Title	SMBUS BLOCK	
Size	Document Number FX2	Rev 1A
Date: Friday, May 05, 2006	Sheet 45 of 47	