

Compal Confidential

Schematic Document

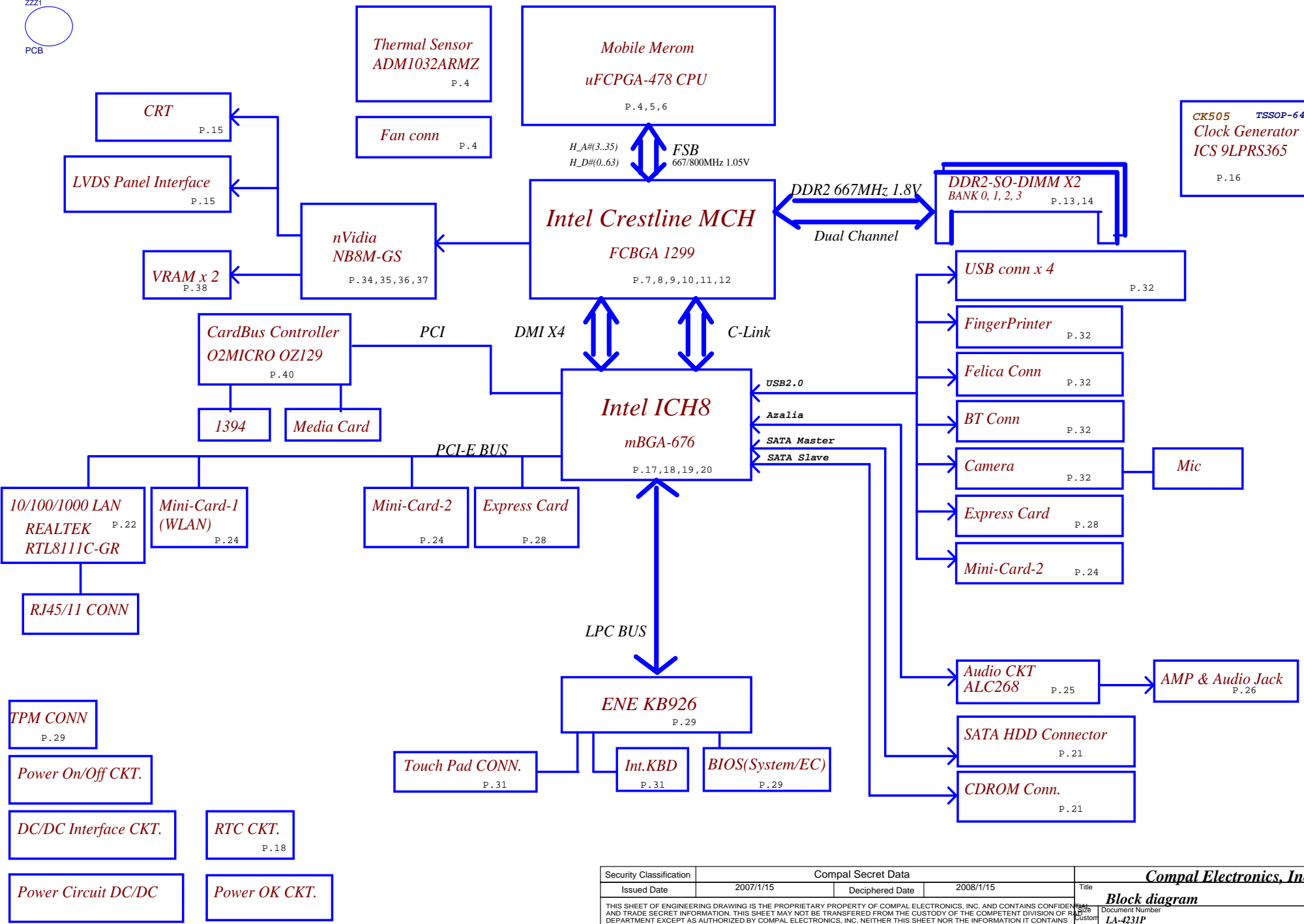
Crestline + ICH8

2007 / 11 / 14 Rev:0.2

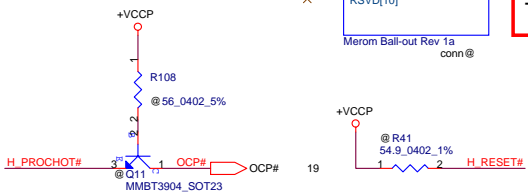
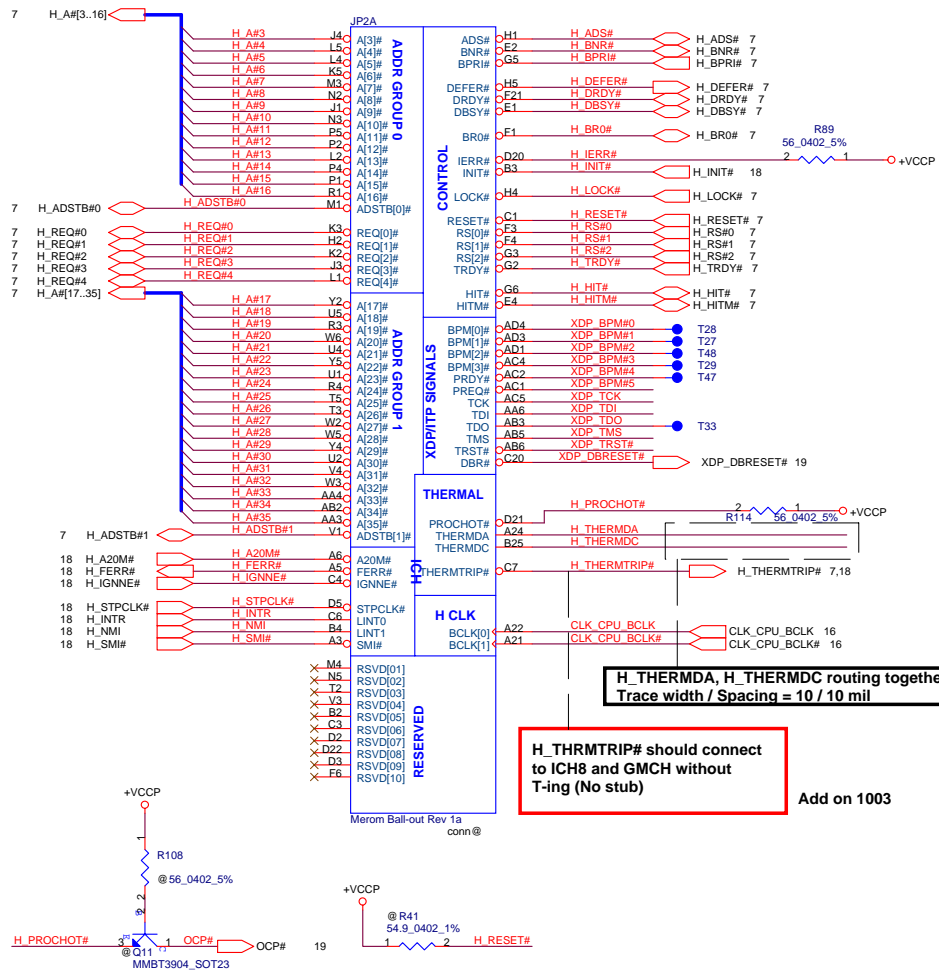
Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i>	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	Cover Sheet
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				Customer	LA-4231P

SMB 13.3

File Name : LA-4231P



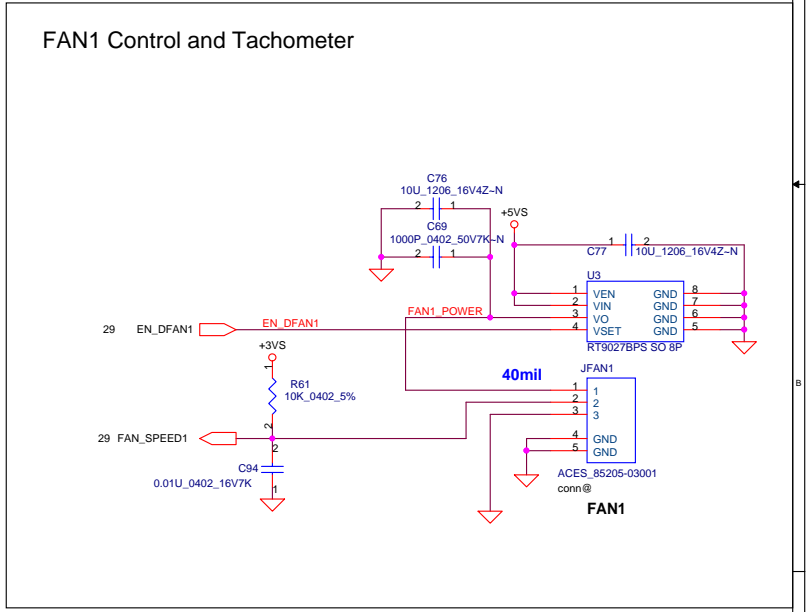
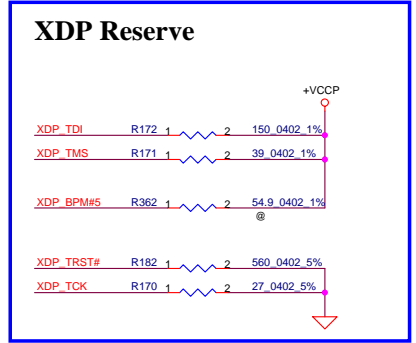
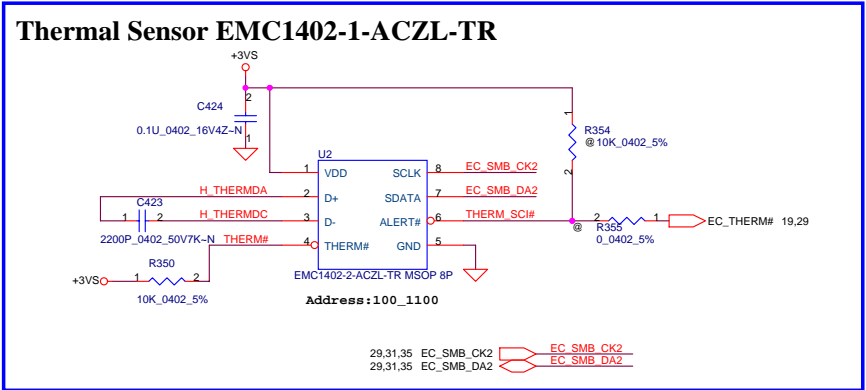
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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Block diagram	
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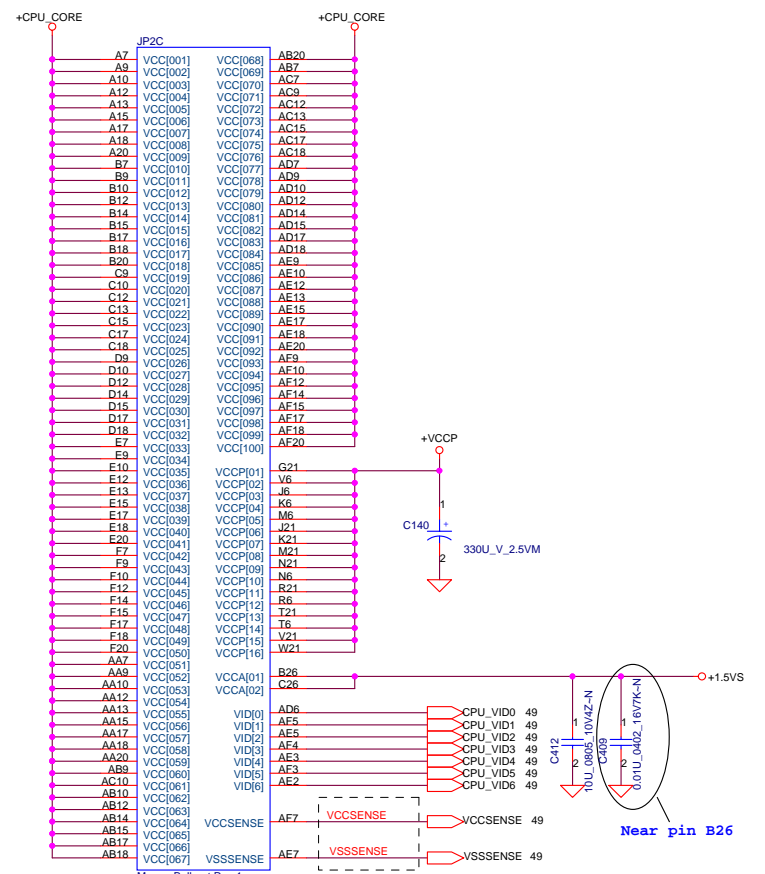
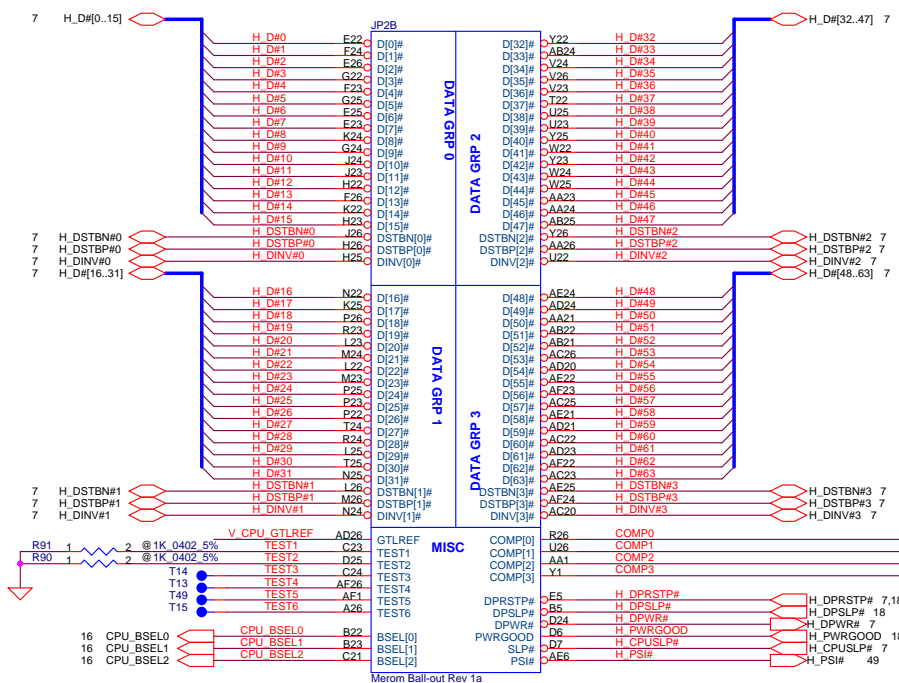
H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

H_THRMTRIP# should connect to ICH8 and GMCH without T-ing (No stub)

Add on 1003



Security Classification	Compal Secret Data		Title	
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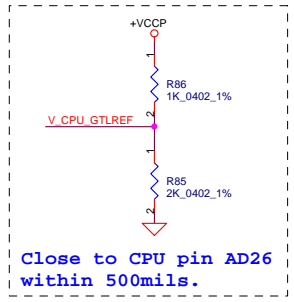


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

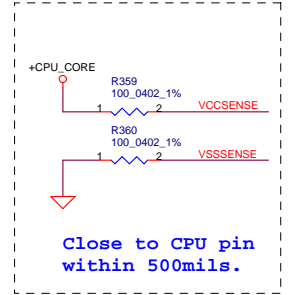
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AD26 within 500mils.

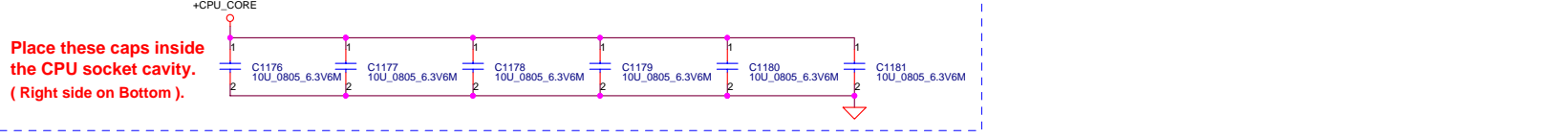
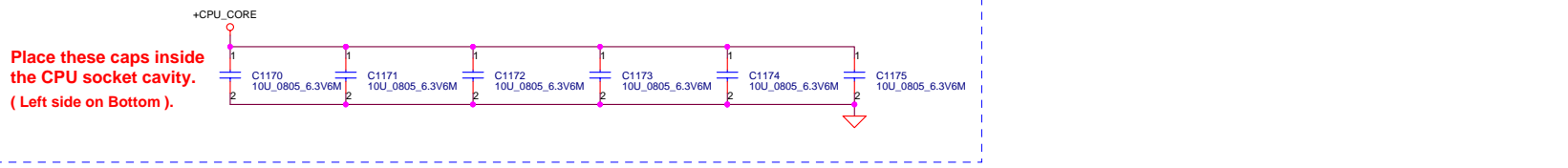
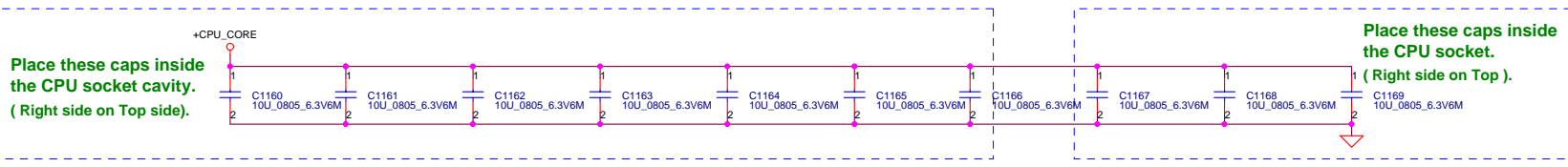
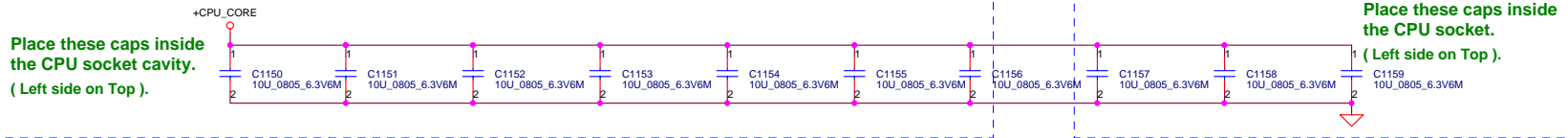


Close to CPU pin within 500mils.

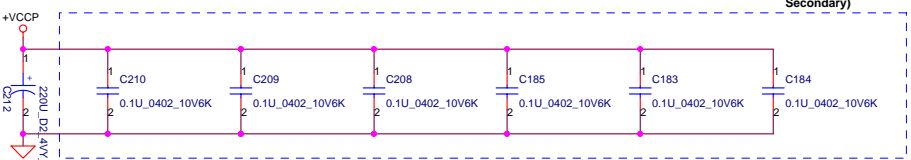
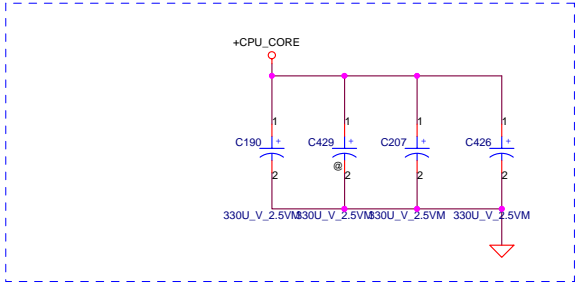
High Frequency Decoupling

10uF 0805 X5R -> 85 degree.

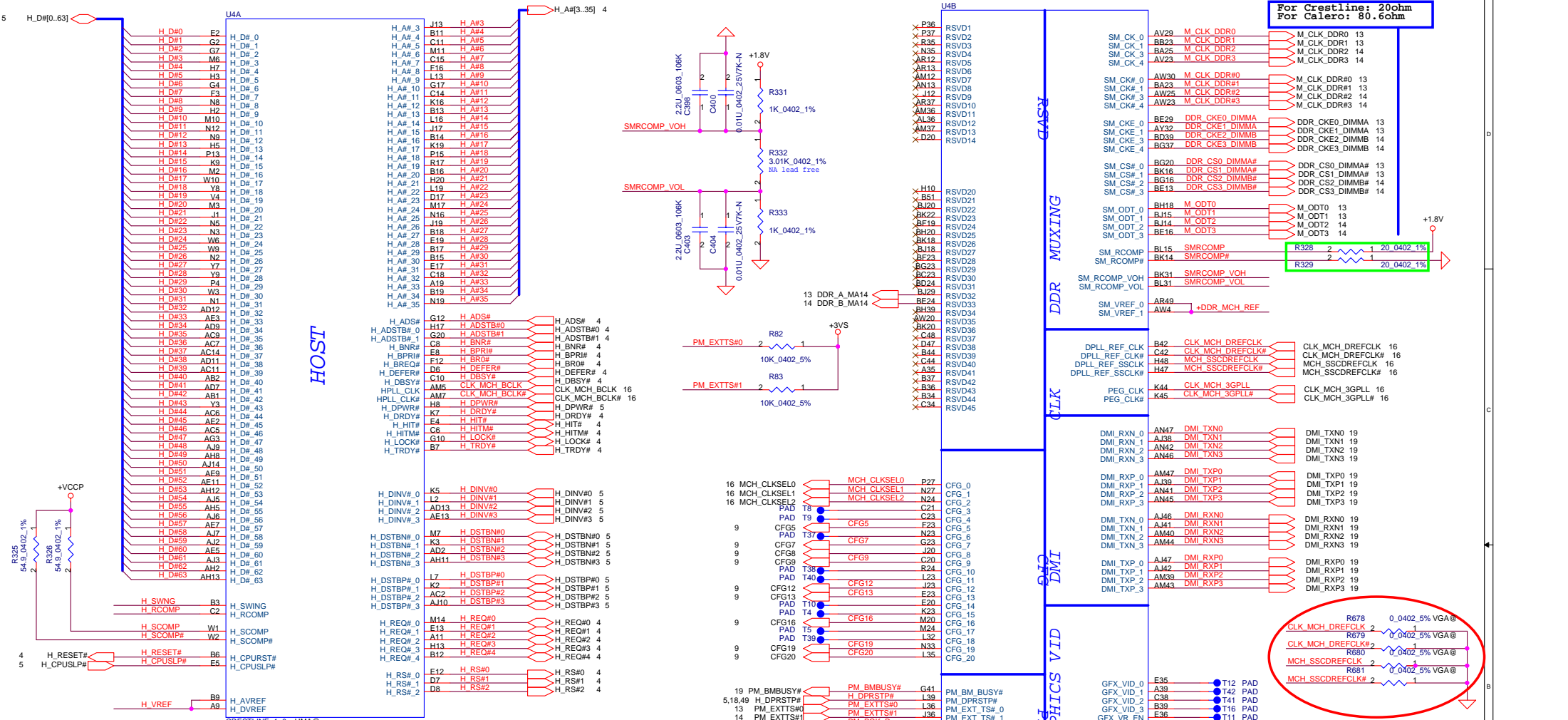
A4	JP2D	VSS[001]	P6
A8	VSS[002]	VSS[082]	P21
A11	VSS[003]	VSS[083]	P24
A14	VSS[004]	VSS[084]	R2
A16	VSS[005]	VSS[085]	R5
A19	VSS[006]	VSS[086]	R22
A23	VSS[007]	VSS[087]	R25
AE2	VSS[008]	VSS[088]	T1
BE	VSS[009]	VSS[089]	T4
BA	VSS[010]	VSS[090]	T14
B11	VSS[011]	VSS[091]	T23
B13	VSS[012]	VSS[092]	T26
B16	VSS[013]	VSS[093]	U3
B19	VSS[014]	VSS[094]	U6
B21	VSS[015]	VSS[095]	U21
B24	VSS[016]	VSS[096]	U24
C5	VSS[017]	VSS[097]	V2
C8	VSS[018]	VSS[098]	V5
C11	VSS[019]	VSS[099]	V22
C14	VSS[020]	VSS[100]	V25
C16	VSS[021]	VSS[101]	W1
C19	VSS[022]	VSS[102]	W4
C2	VSS[023]	VSS[103]	W23
C22	VSS[024]	VSS[104]	W26
C25	VSS[025]	VSS[105]	Y3
D1	VSS[026]	VSS[106]	Y6
D4	VSS[027]	VSS[107]	Y21
D8	VSS[028]	VSS[108]	Y24
D11	VSS[029]	VSS[109]	AA2
D13	VSS[030]	VSS[110]	AA5
D16	VSS[031]	VSS[111]	AA8
D19	VSS[032]	VSS[112]	AA11
D23	VSS[033]	VSS[113]	AA14
D26	VSS[034]	VSS[114]	AA16
E3	VSS[035]	VSS[115]	AA19
E6	VSS[036]	VSS[116]	AA22
E8	VSS[037]	VSS[117]	AA25
F11	VSS[038]	VSS[118]	AB1
F14	VSS[039]	VSS[119]	AB4
F16	VSS[040]	VSS[120]	AB8
F19	VSS[041]	VSS[121]	AB11
F21	VSS[042]	VSS[122]	AB13
F24	VSS[043]	VSS[123]	AB16
F5	VSS[044]	VSS[124]	AB19
F8	VSS[045]	VSS[125]	AB23
F11	VSS[046]	VSS[126]	AB26
F13	VSS[047]	VSS[127]	AC3
F16	VSS[048]	VSS[128]	AC6
F19	VSS[049]	VSS[129]	AC8
F2	VSS[050]	VSS[130]	AC11
F22	VSS[051]	VSS[131]	AC14
F25	VSS[052]	VSS[132]	AC16
G4	VSS[053]	VSS[133]	AC19
G1	VSS[054]	VSS[134]	AC21
G23	VSS[055]	VSS[135]	AC24
G26	VSS[056]	VSS[136]	AD2
H3	VSS[057]	VSS[137]	AD5
H6	VSS[058]	VSS[138]	AD8
H21	VSS[059]	VSS[139]	AD11
H24	VSS[060]	VSS[140]	AD13
J2	VSS[061]	VSS[141]	AD16
J5	VSS[062]	VSS[142]	AD19
J22	VSS[063]	VSS[143]	AD22
J25	VSS[064]	VSS[144]	AD25
K1	VSS[065]	VSS[145]	AE1
K4	VSS[066]	VSS[146]	AE4
K23	VSS[067]	VSS[147]	AE8
K26	VSS[068]	VSS[148]	AE11
L3	VSS[069]	VSS[149]	AE14
L6	VSS[070]	VSS[150]	AE16
L24	VSS[071]	VSS[151]	AE19
M2	VSS[072]	VSS[152]	AE23
M5	VSS[073]	VSS[153]	AE26
M22	VSS[074]	VSS[154]	A2
M25	VSS[075]	VSS[155]	AF6
N1	VSS[076]	VSS[156]	AF8
N4	VSS[077]	VSS[157]	AF11
N23	VSS[078]	VSS[158]	AF13
N26	VSS[079]	VSS[159]	AF16
P3	VSS[080]	VSS[160]	AF19
	VSS[081]	VSS[161]	AF21
		VSS[162]	A25
		VSS[163]	AF25



Near CPU CORE regulator
ESR <= 1.5m ohm
Capacitor > 1980uF



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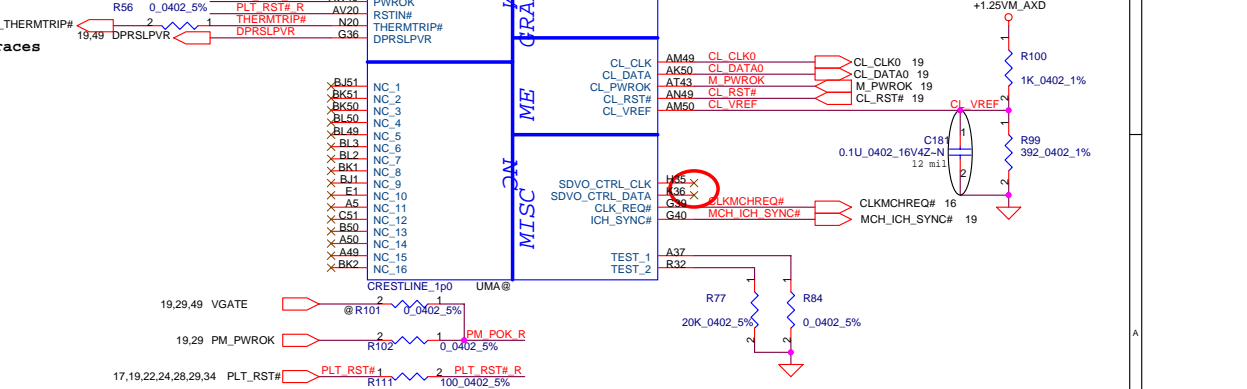
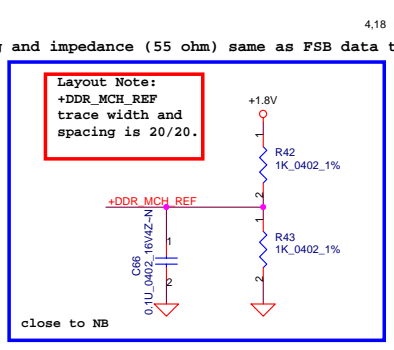
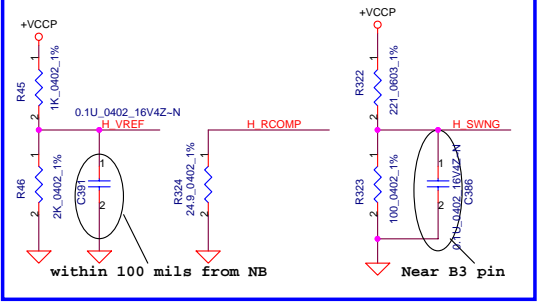


For Crestline: 20ohm
For Calero: 80.6ohm

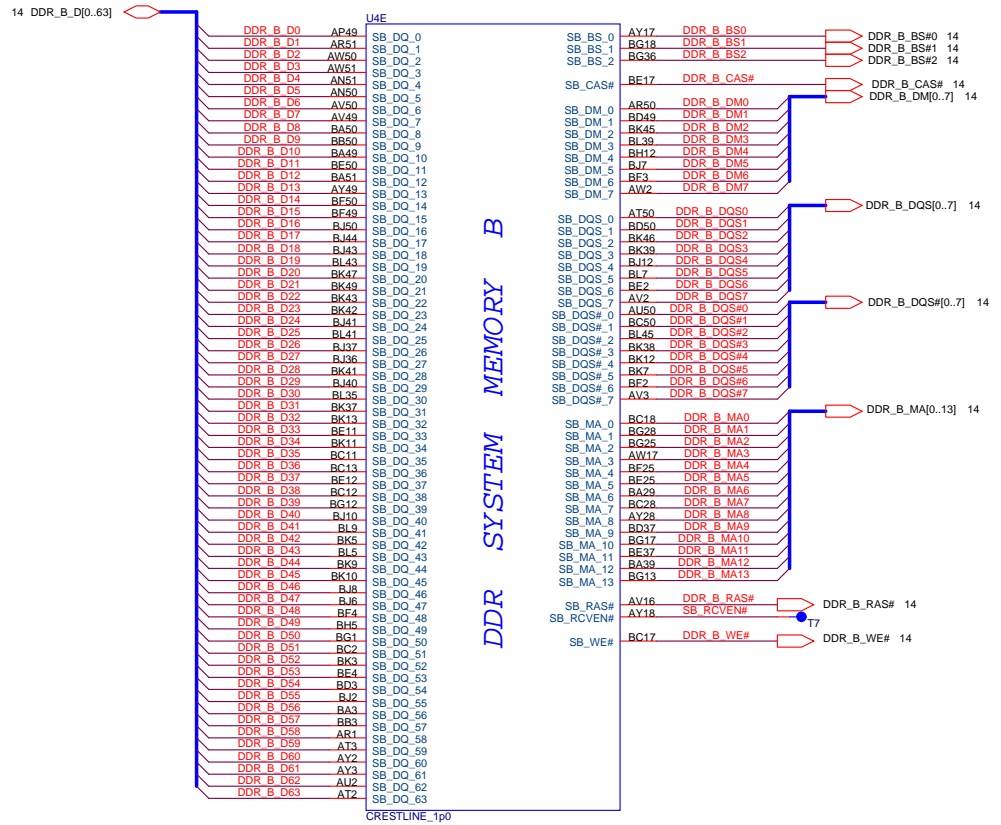
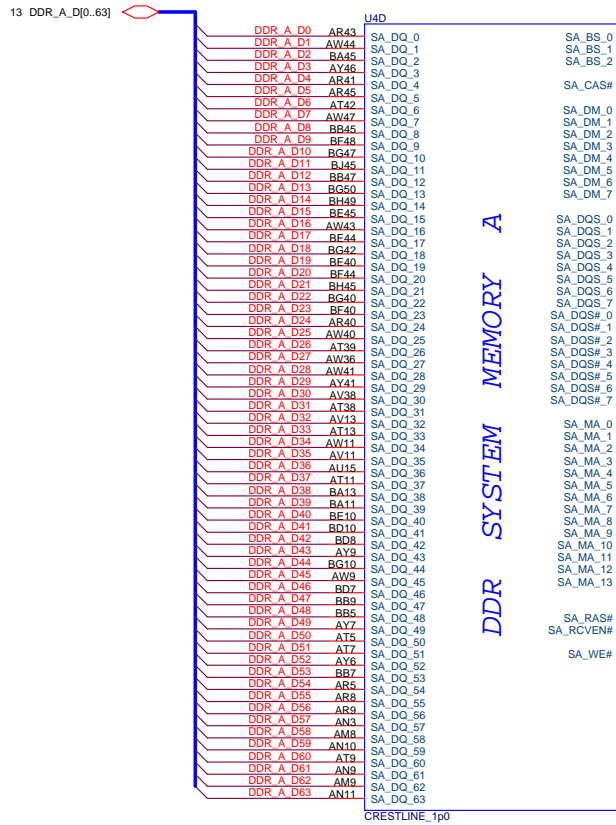
layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

Layout Note:
+DDR_MCH_REF
trace width and spacing is 20/20.

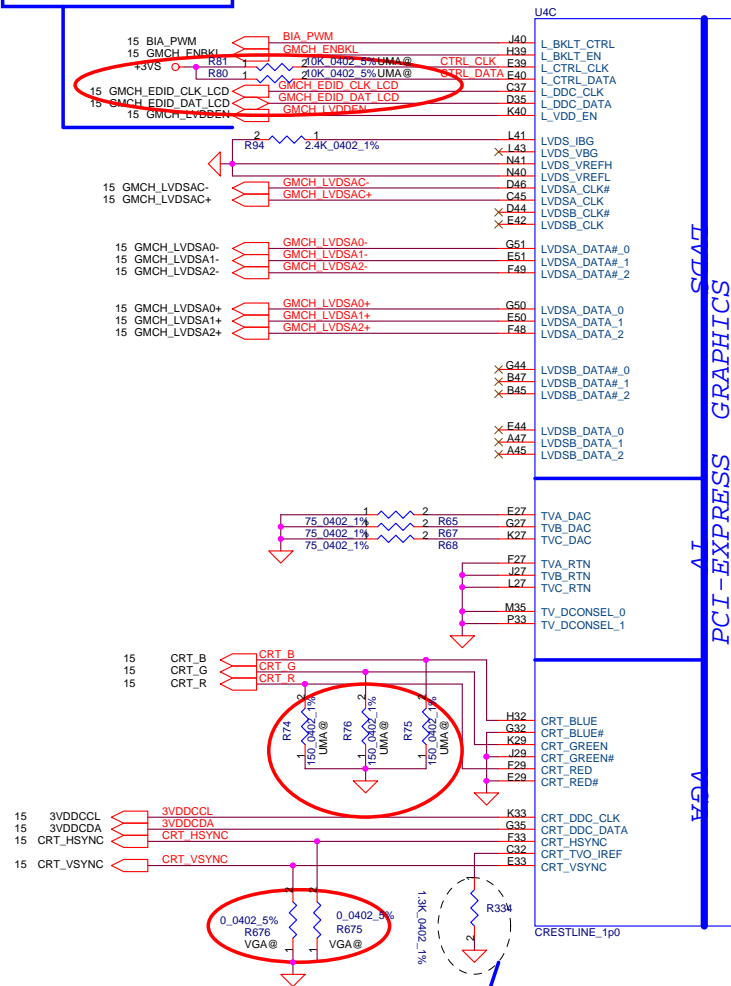


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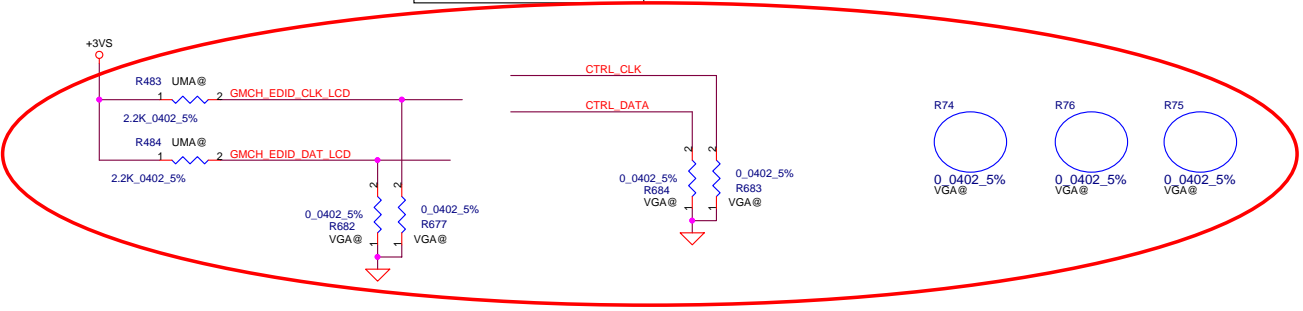


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Issued Date	2007/1/15	Deciphered Date	2008/1/15	CRESTLINE((2/6)-DDR2 A/B CH
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For Crestline: 2.4kohm
For Calero: 1.5kohm

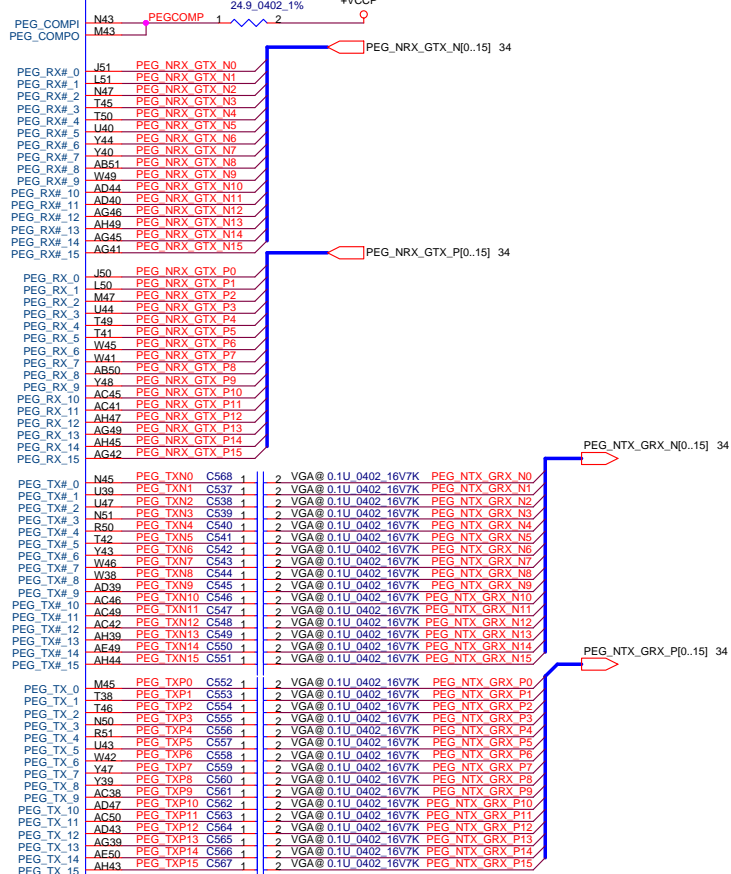


For Crestline: 1.3kohm
For Calero: 255ohm



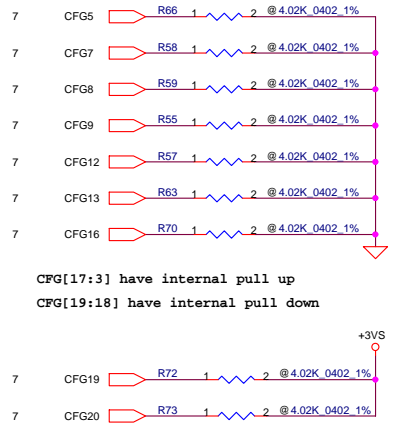
Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

PEGCOMP trace width and spacing is 20/25 mils.

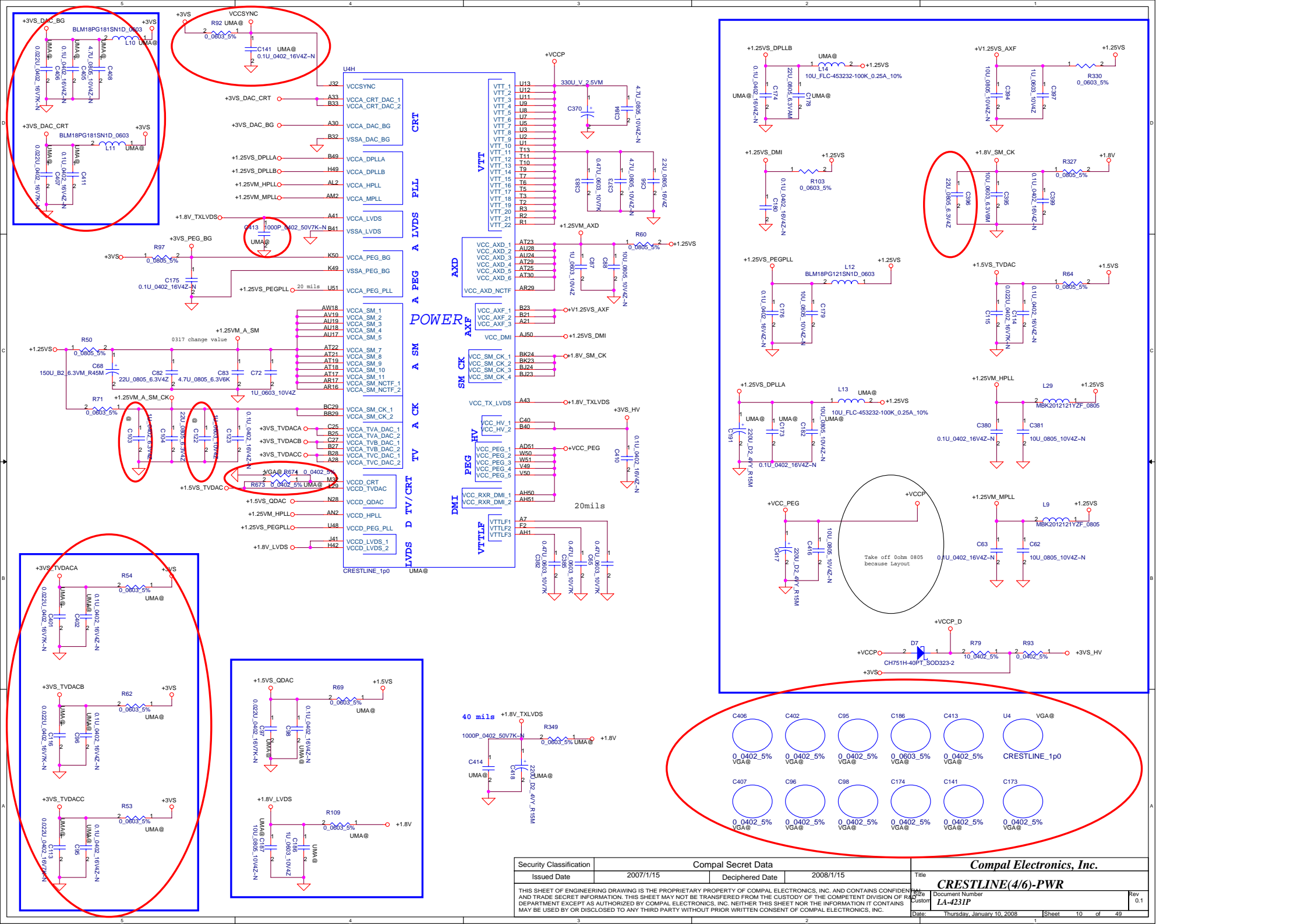


Strap Pin Table

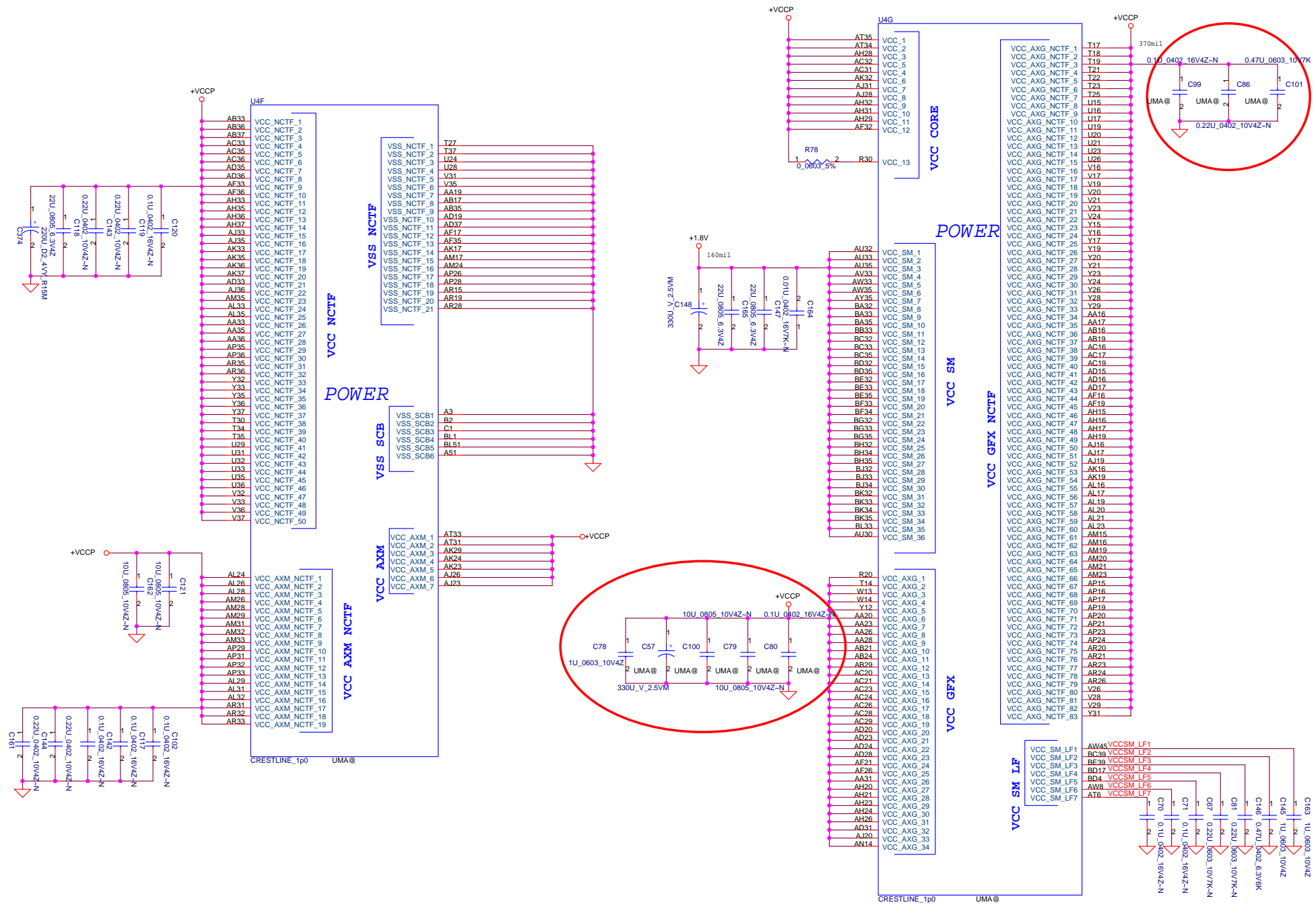
CFG	Function	Options
CFG[2:0]	FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5	(DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6		Reserved
CFG7	(CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8	(Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9	(PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]		Reserved
CFG[13:12]	(XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]		Reserved
CFG16	(FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]		Reserved
SDVO_CTRLDATA		0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19	(DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20	(PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu. *



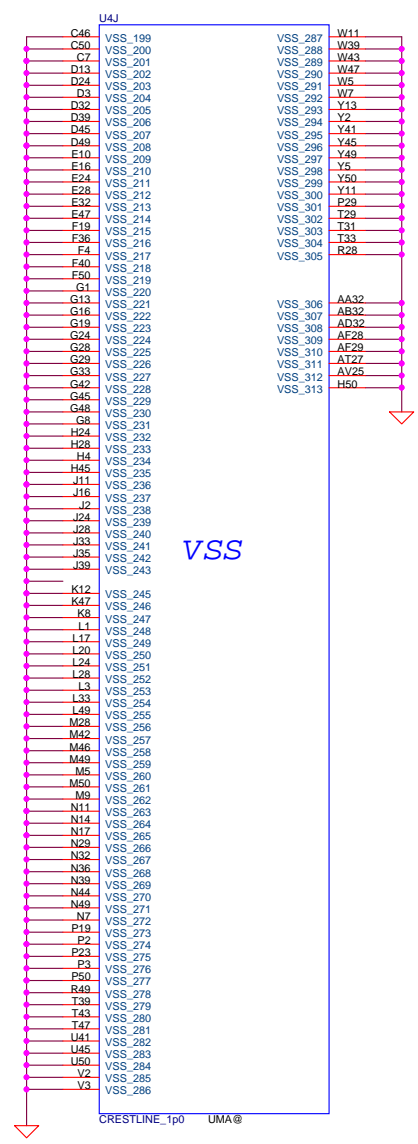
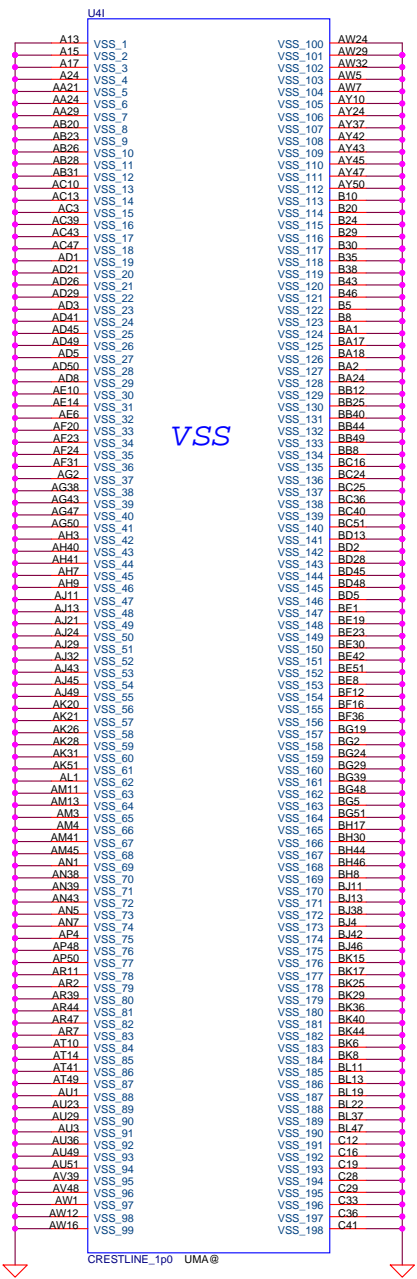
CFG[17:3] have internal pull up
CFG[19:18] have internal pull down



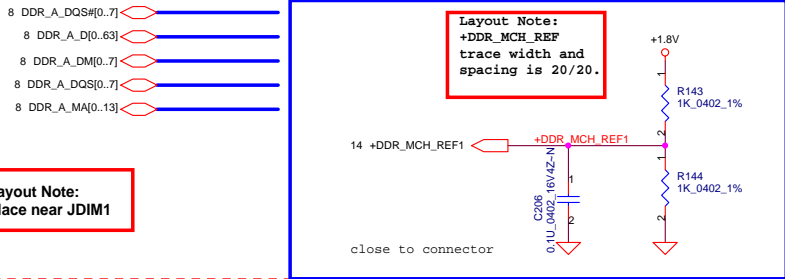
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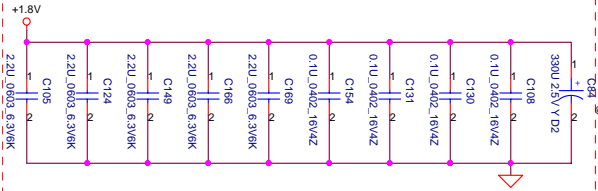
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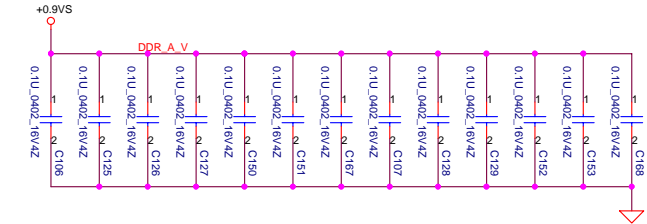
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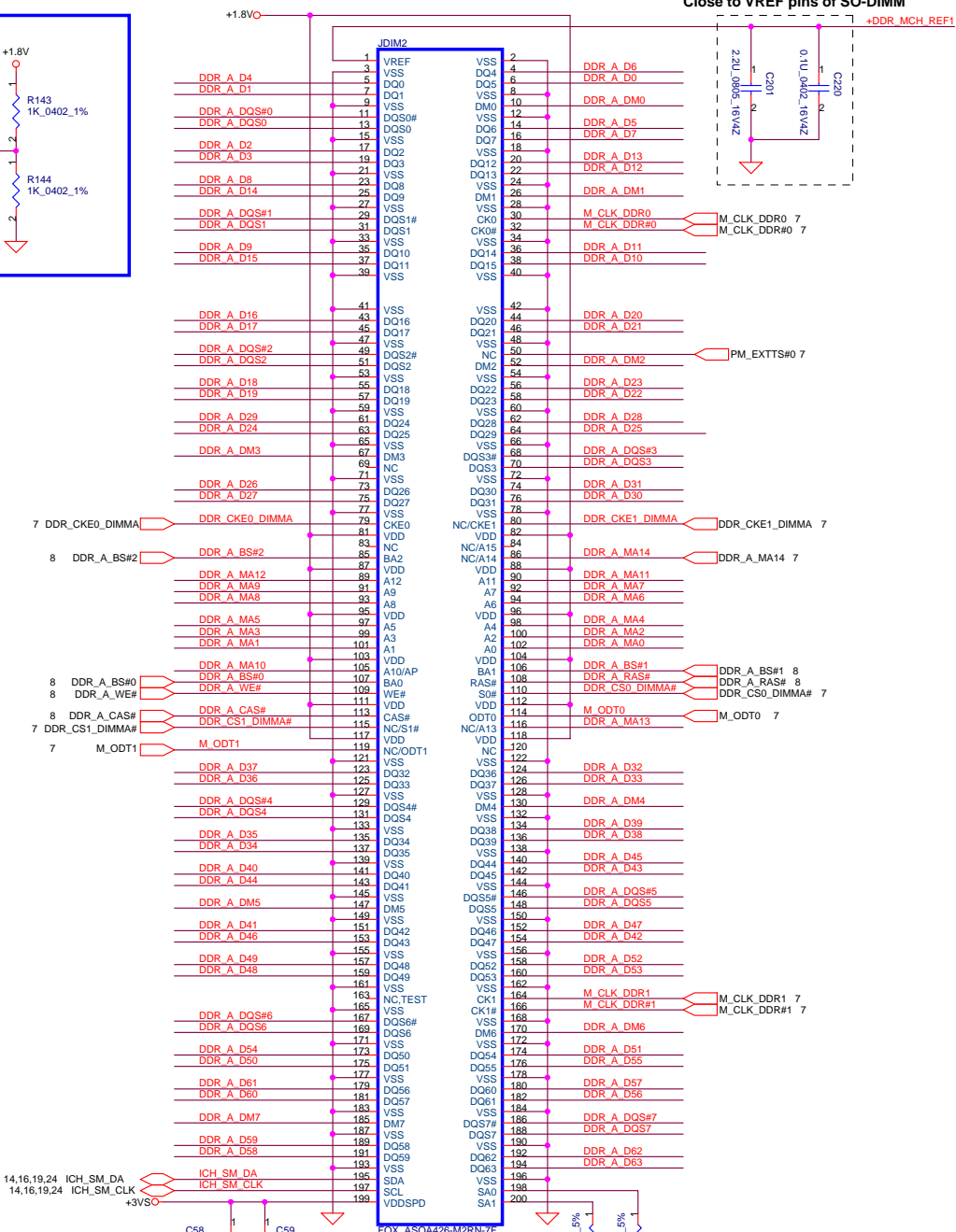
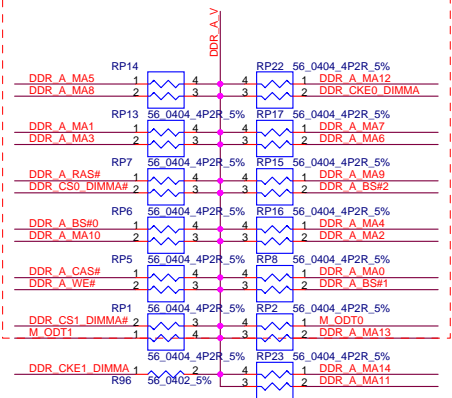
Layout Note:
Place near JDIM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

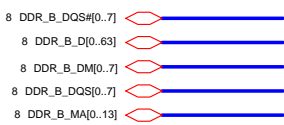


Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"

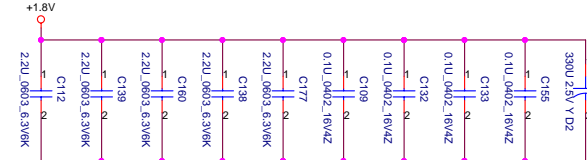


**SO-DIMM A
REVERSE
Bottom side**

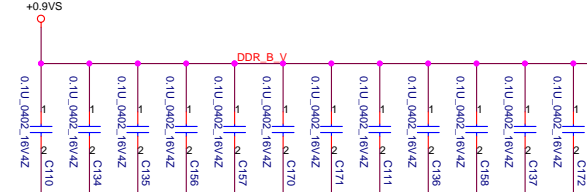
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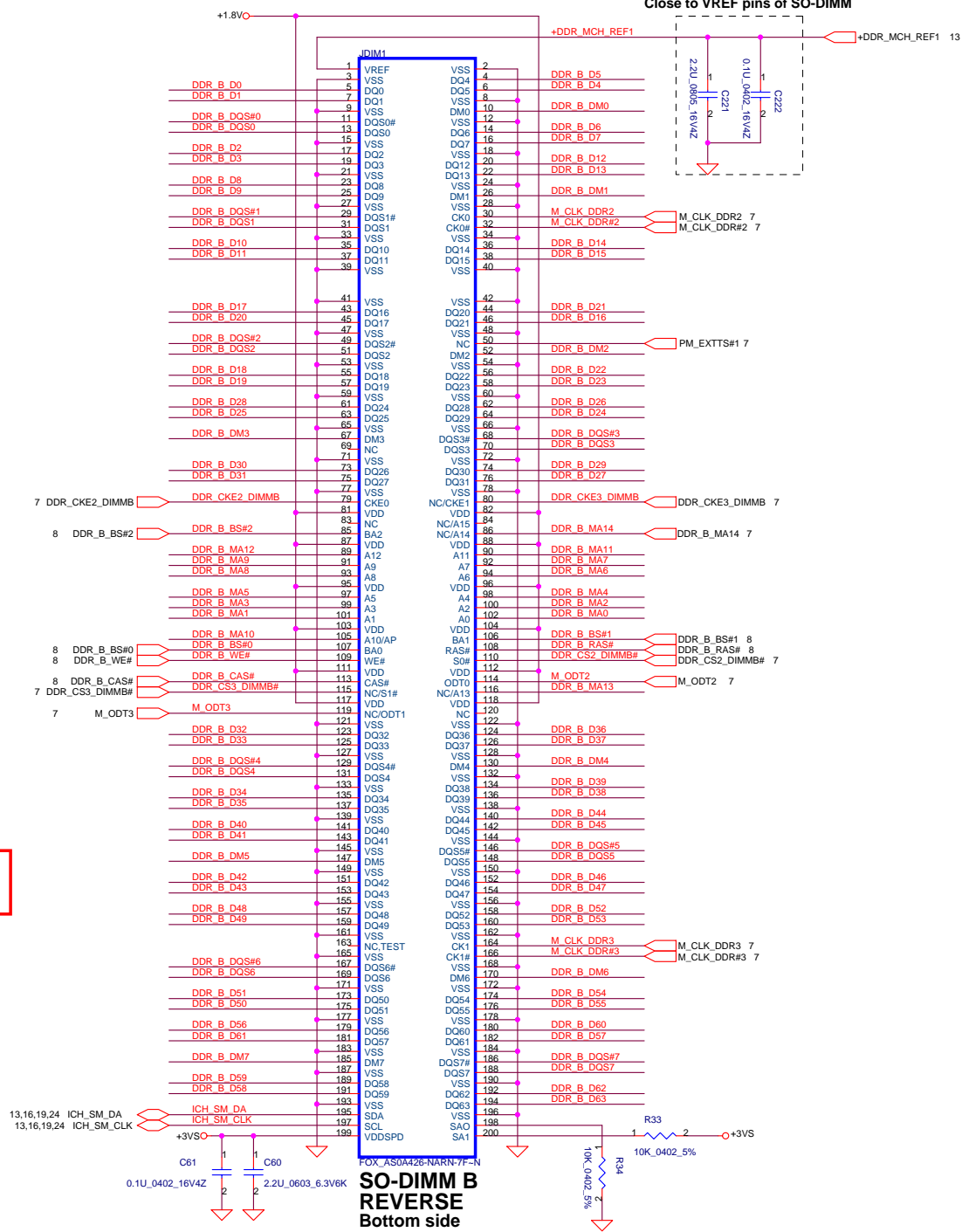
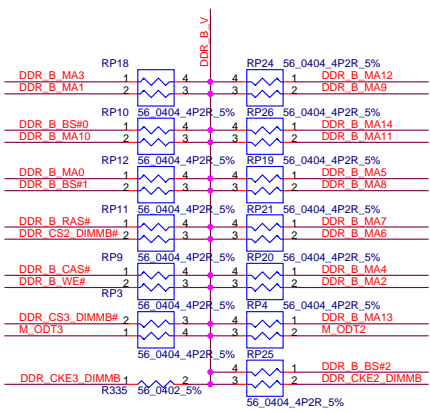
Layout Note:
Place near JDIM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



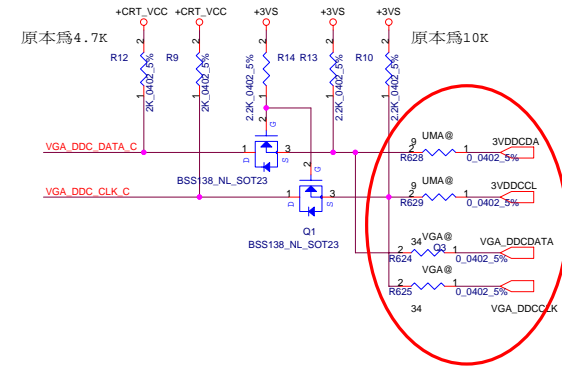
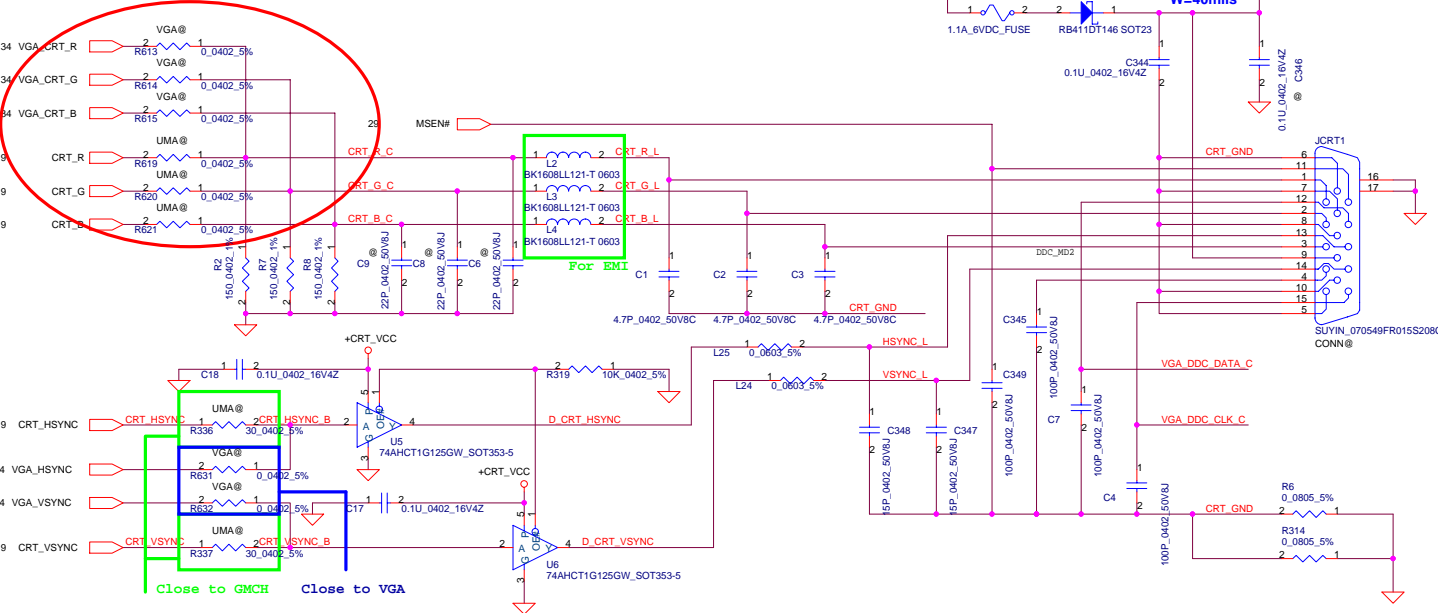
Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"



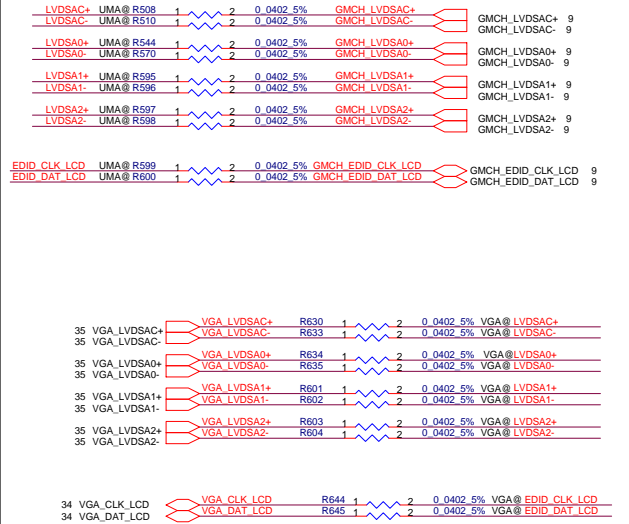
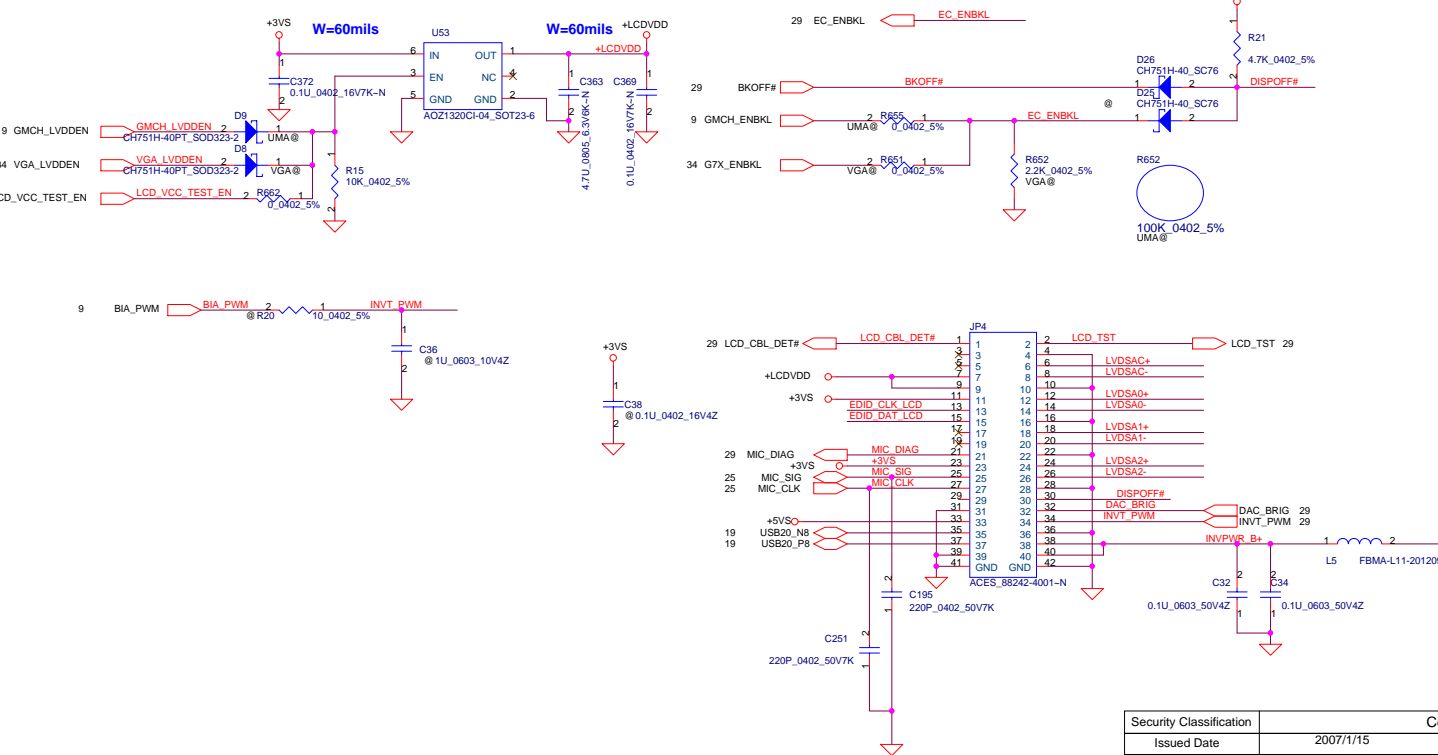
**SO-DIMM B
REVERSE
Bottom side**

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CRT



LCD

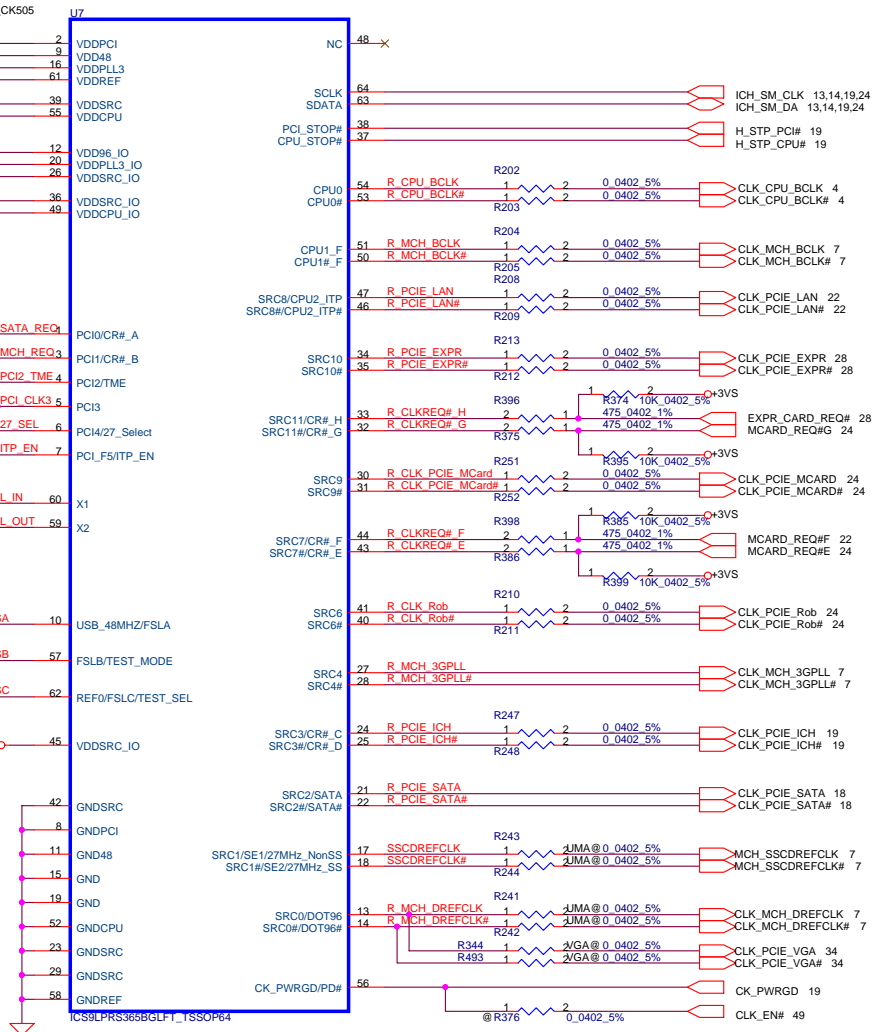
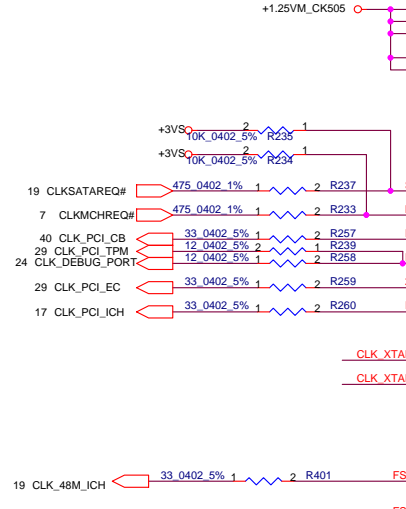
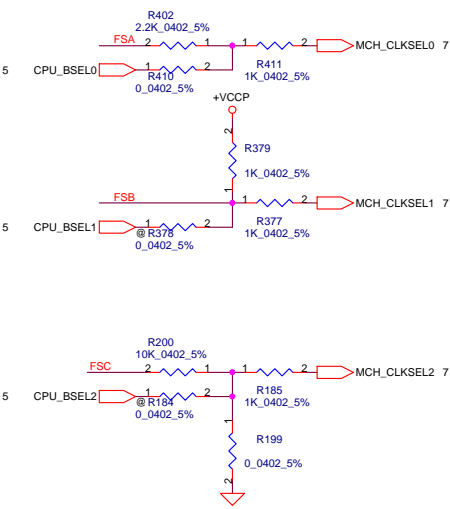
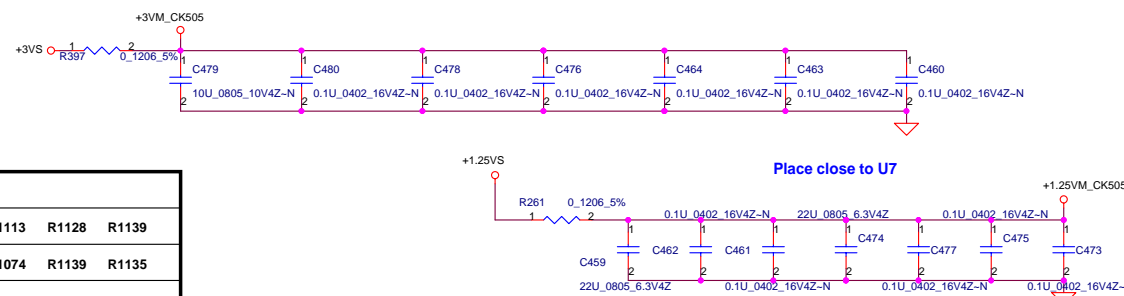


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Size	Customer	Document Number	LA-4231P	Rev	0.1
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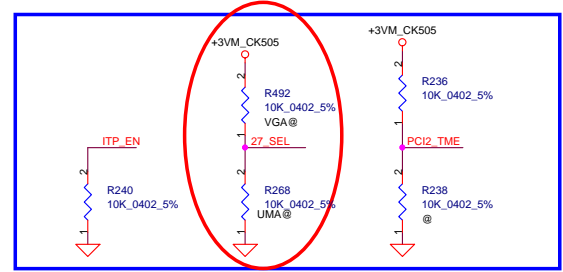
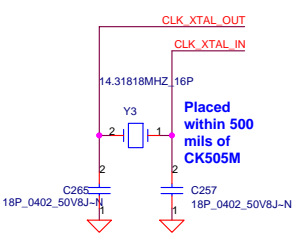
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1107	R1135	R1083
*(Default)	No Stuff	R1074	R1086	R1098
	Stuff	R1113	R1128	R1139
667MHz	Stuff	R1086	R1139	R1135
	No Stuff	R1107	R1128	R1098
800MHz	Stuff	R1135	R1139	
	No Stuff	R1083	R1086	R1098

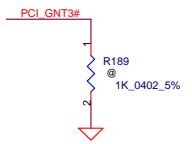
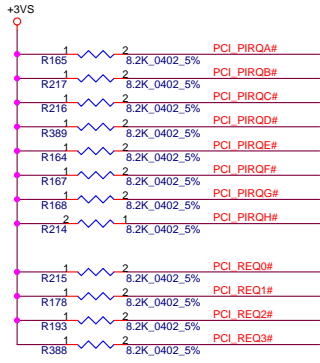
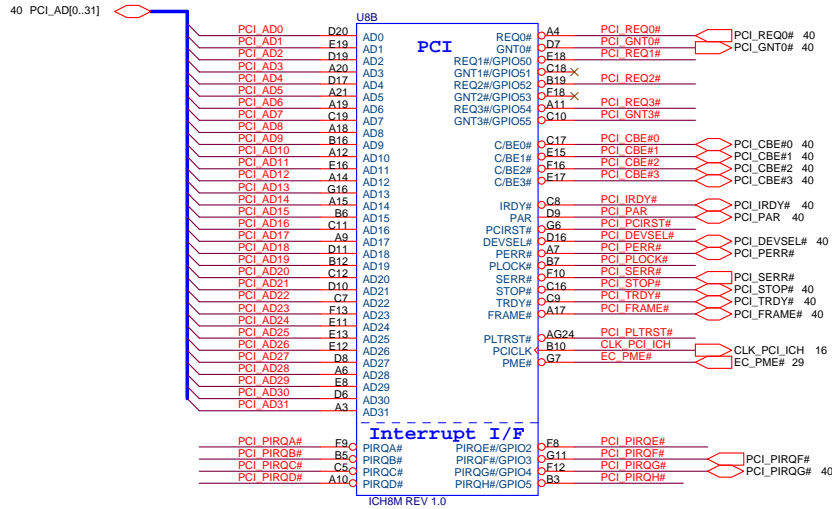
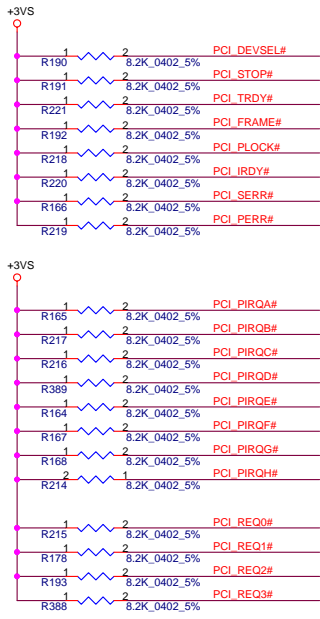


For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
 For 27_SEL, 0 = Enable DOT96 & SRC1, 1 = Enable SRC0 & 27MHz
 For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed, 1 = Overclocking of CPU and SRC NOT allowed



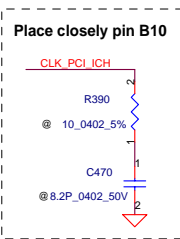
Routing the trace at least 10mil

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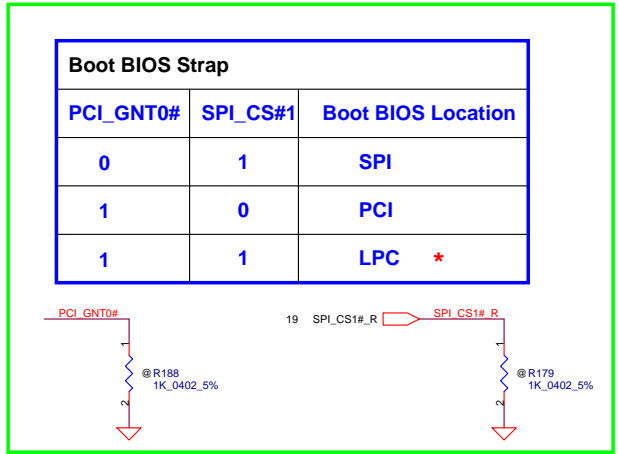


A16 swap override Strap

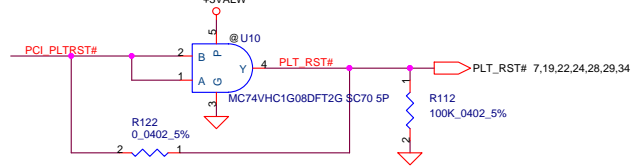
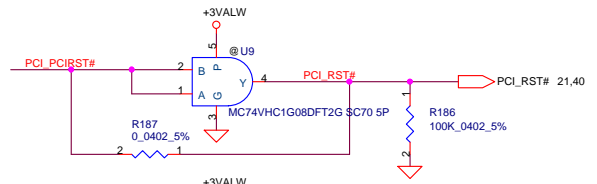
PCI_GNT3#	Low= A16 swap override Enable High= Default*
-----------	-------------------------------------------------

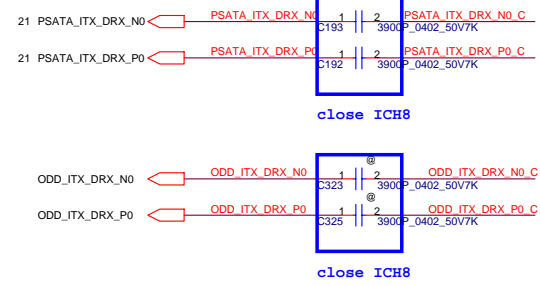
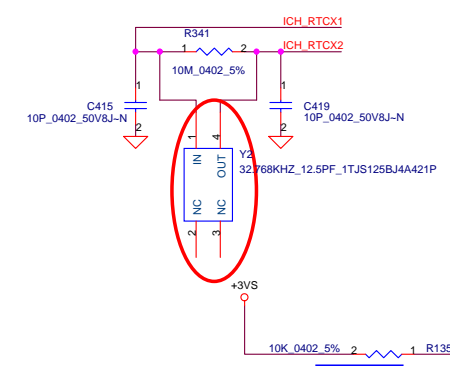
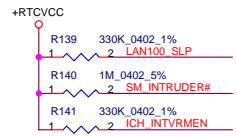


Check if use LPC?



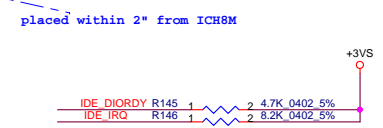
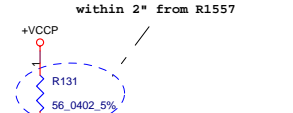
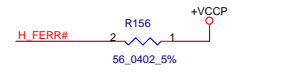
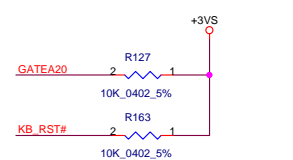
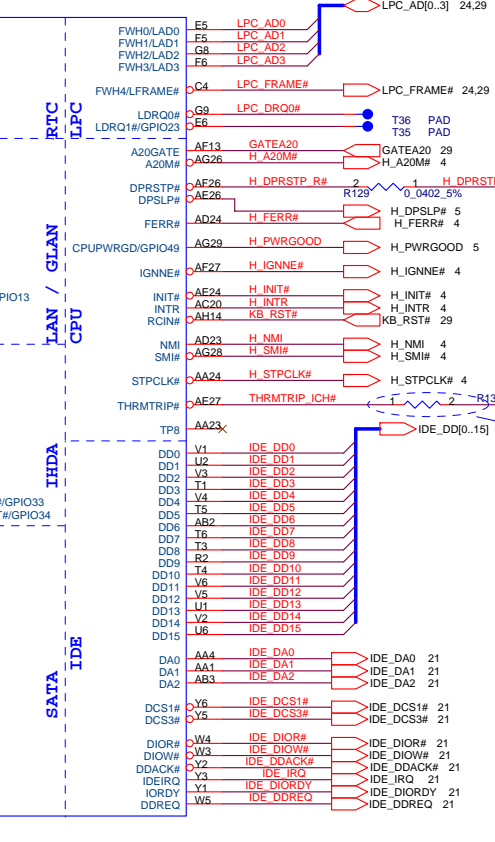
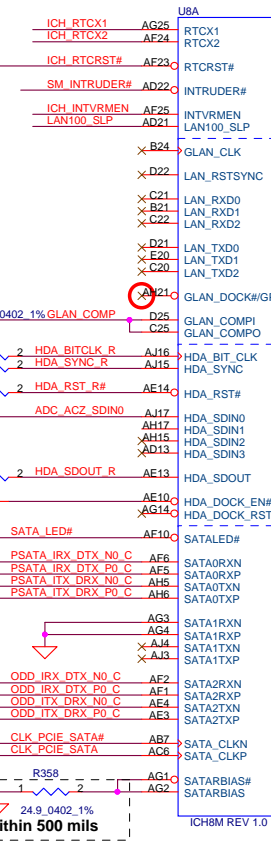
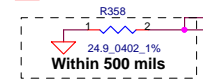
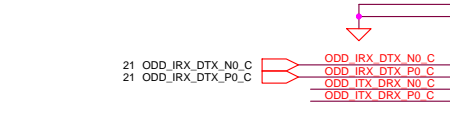
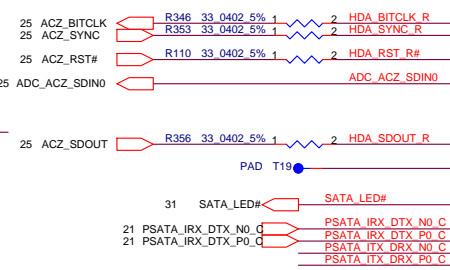
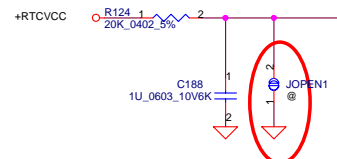
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

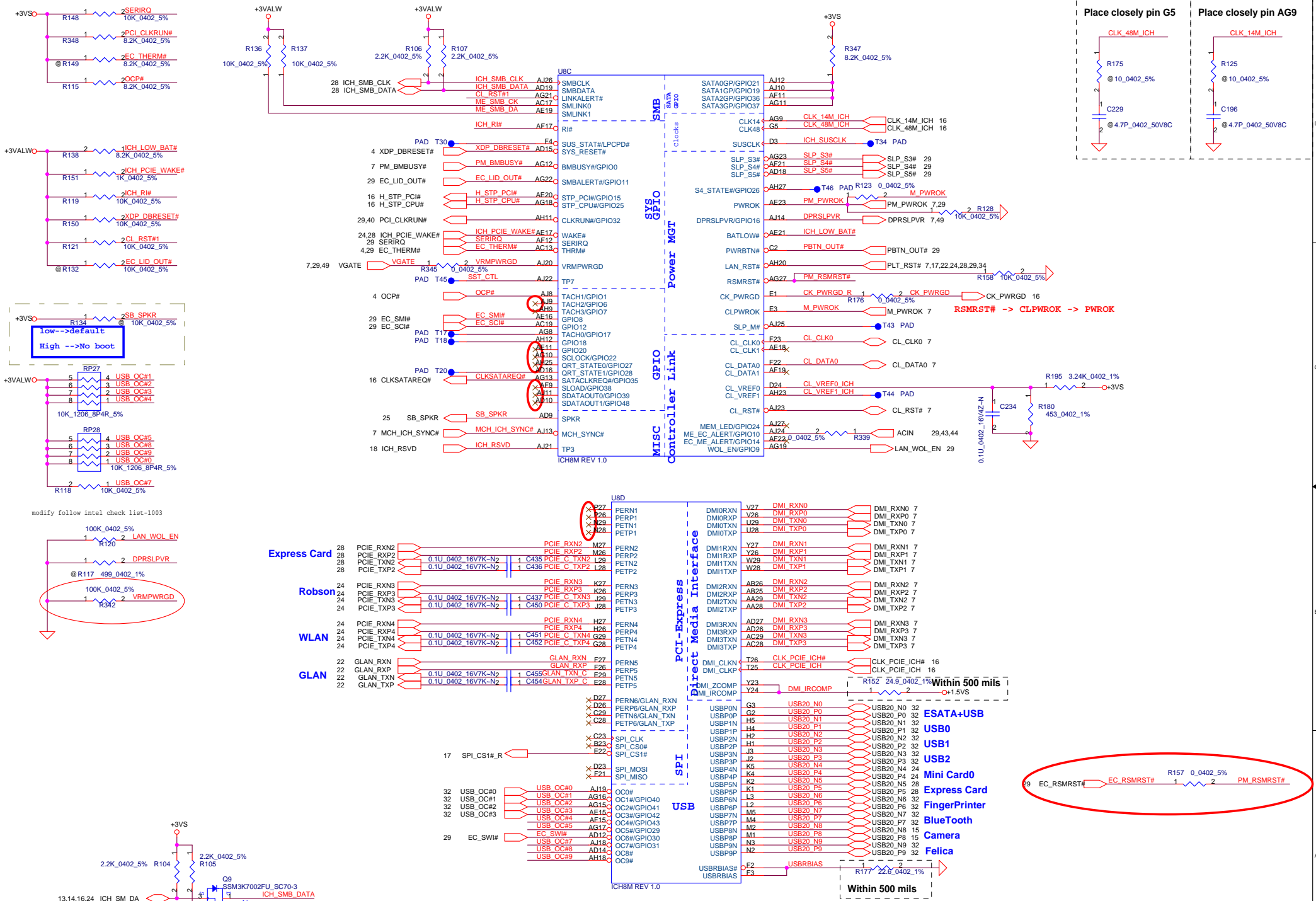




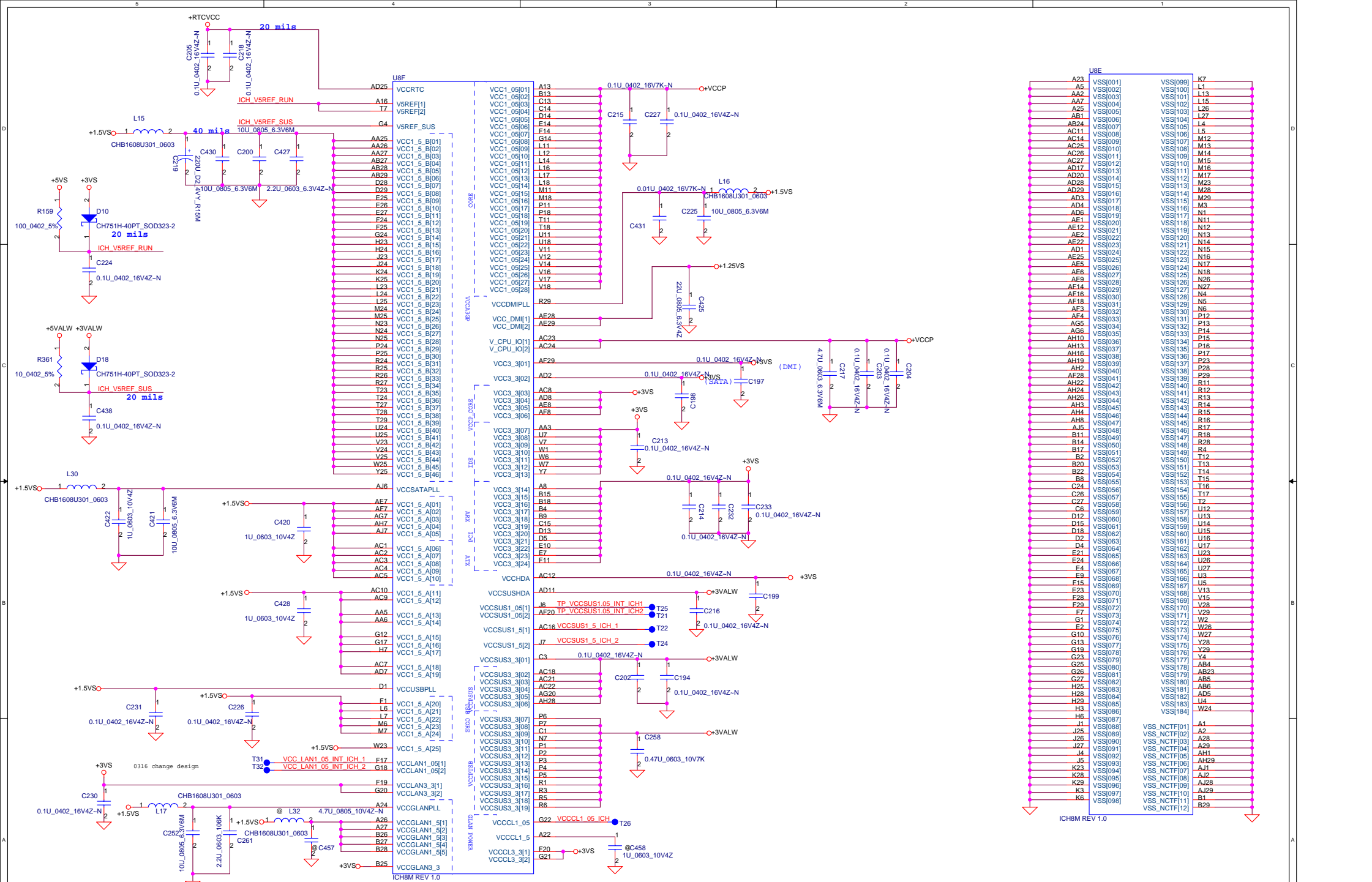
XOR CHAIN ENTRANCE STRAP:RSVD

ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1





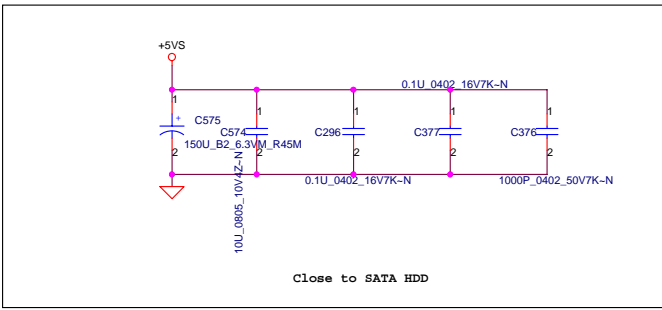
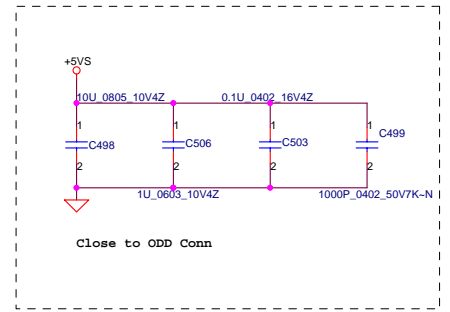
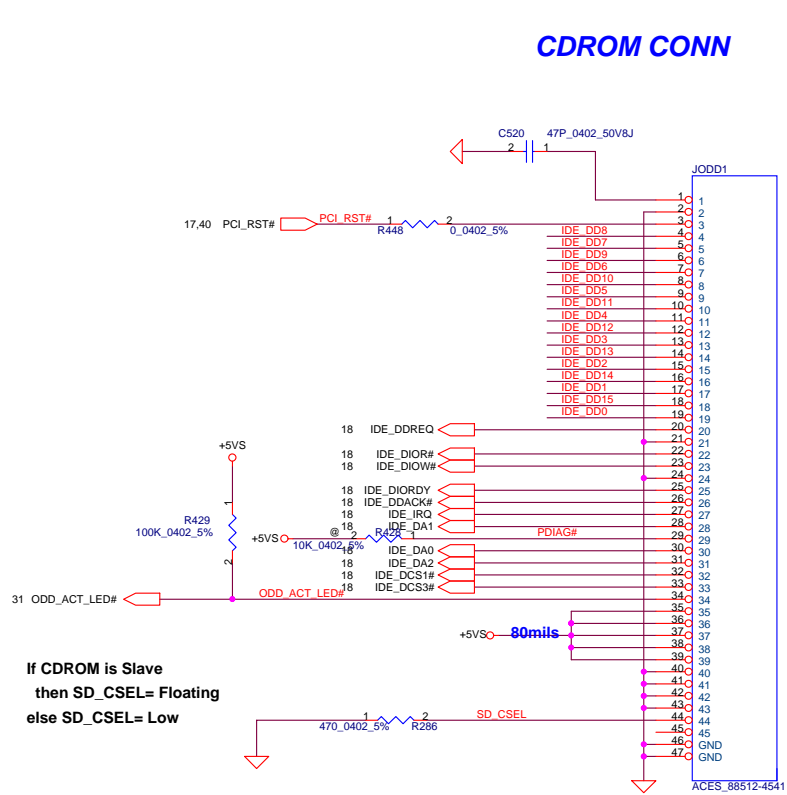
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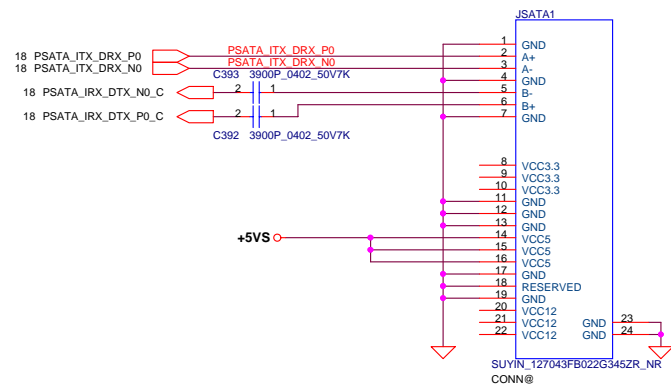
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Issued Date	2007/1/15	Deciphered Date
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Compal Electronics, Inc.	
ICH8(44) POWER&GND	
Title	Document Number
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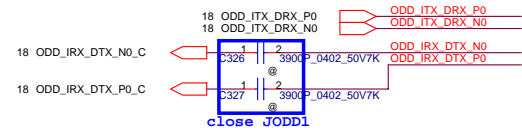
CDROM CONN



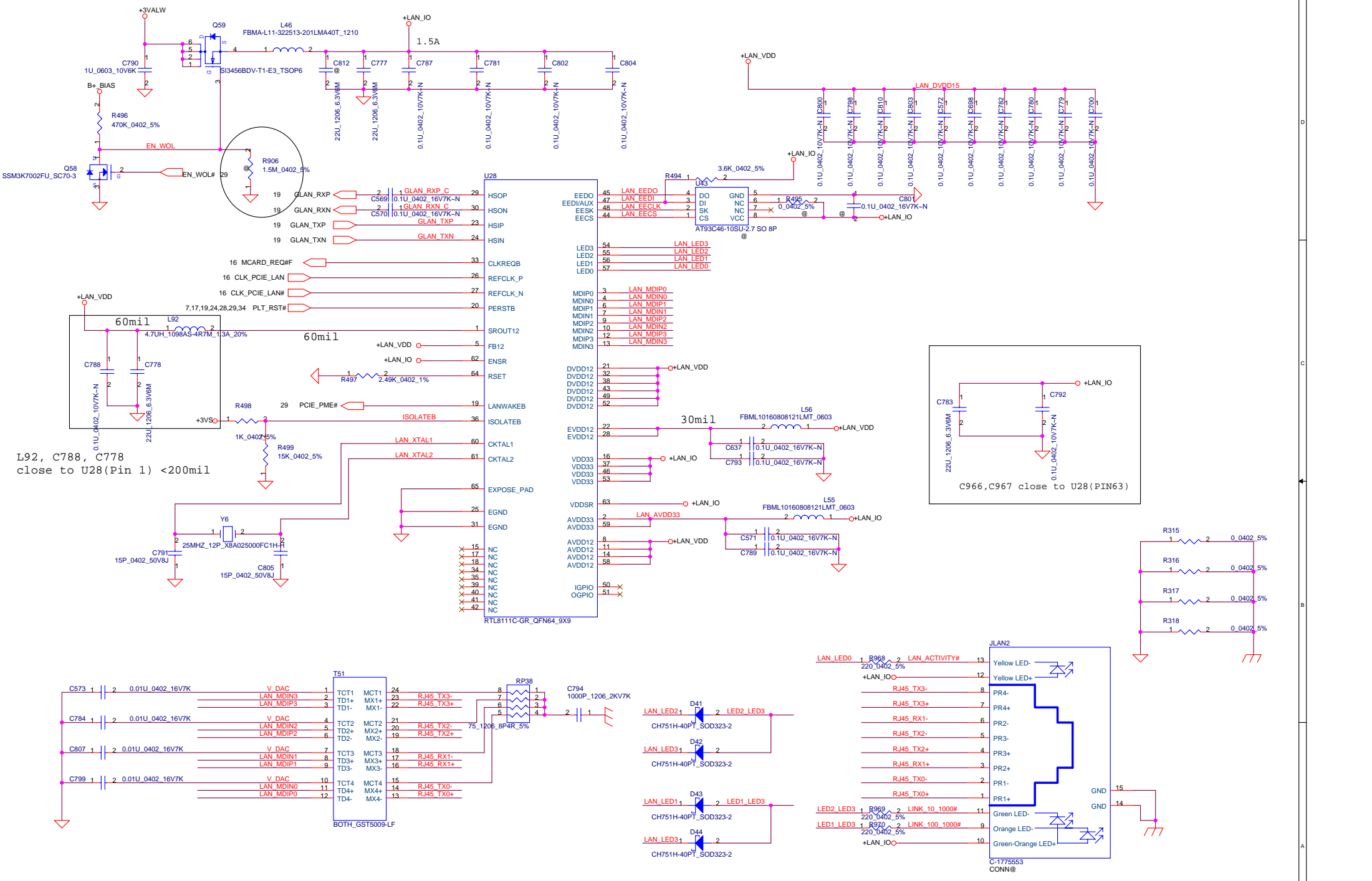
SATA HDD CONN



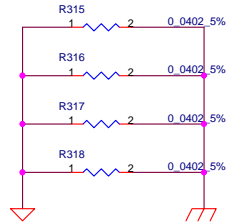
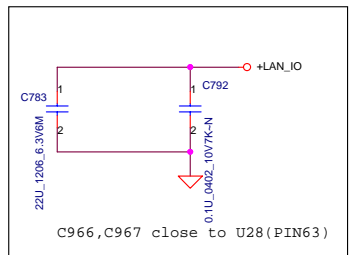
RESERVE(SATA ODD NET)



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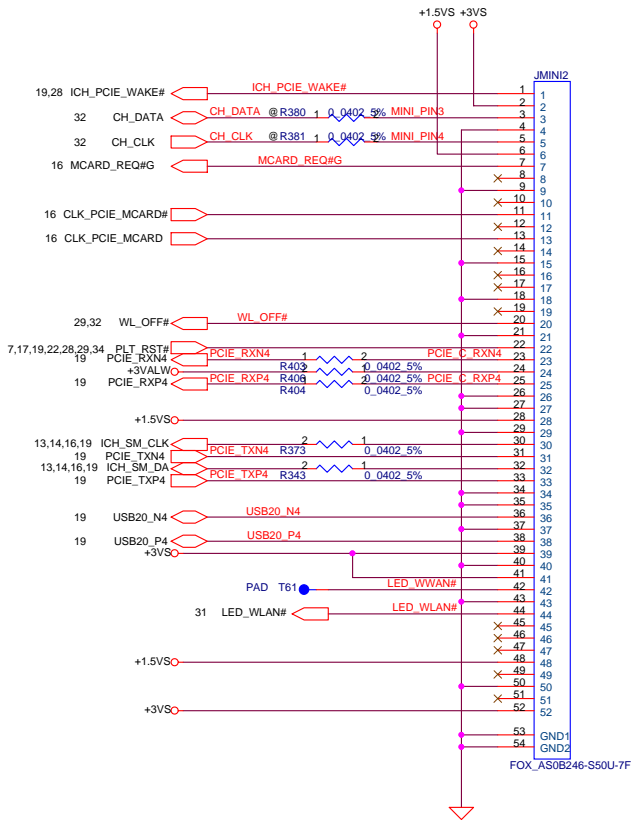


L92, C788, C778
close to U28 (Pin 1) <200mil

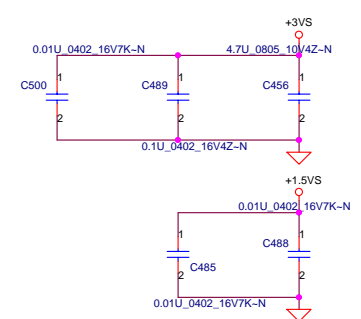
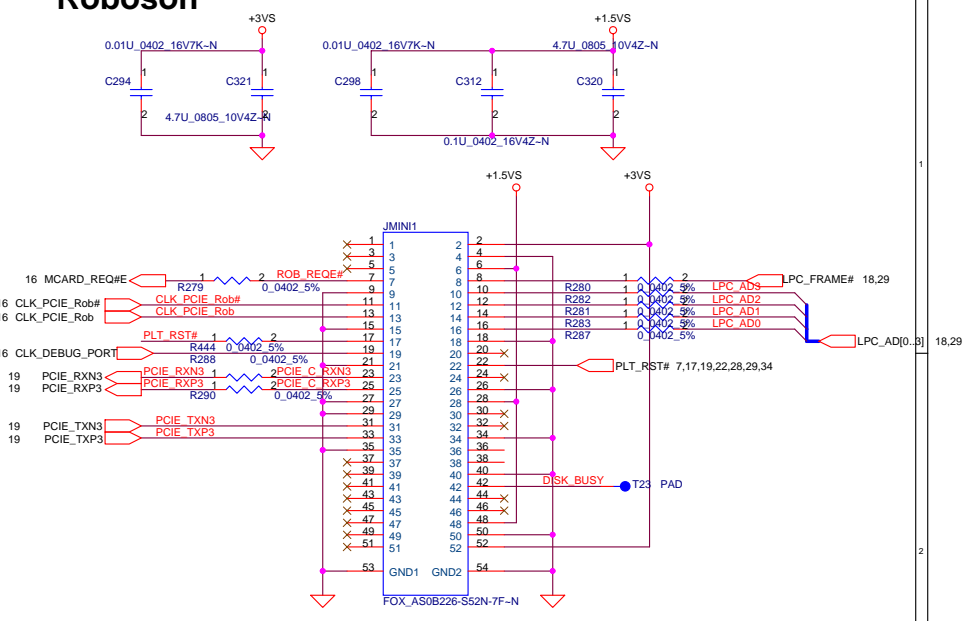


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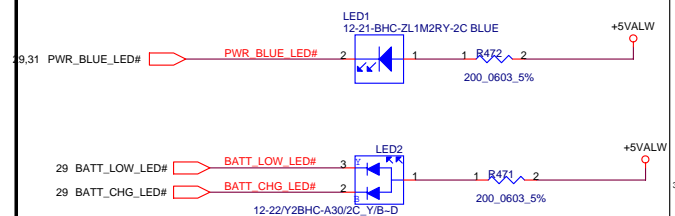
Mini-Express Card---WLAN



Roboson

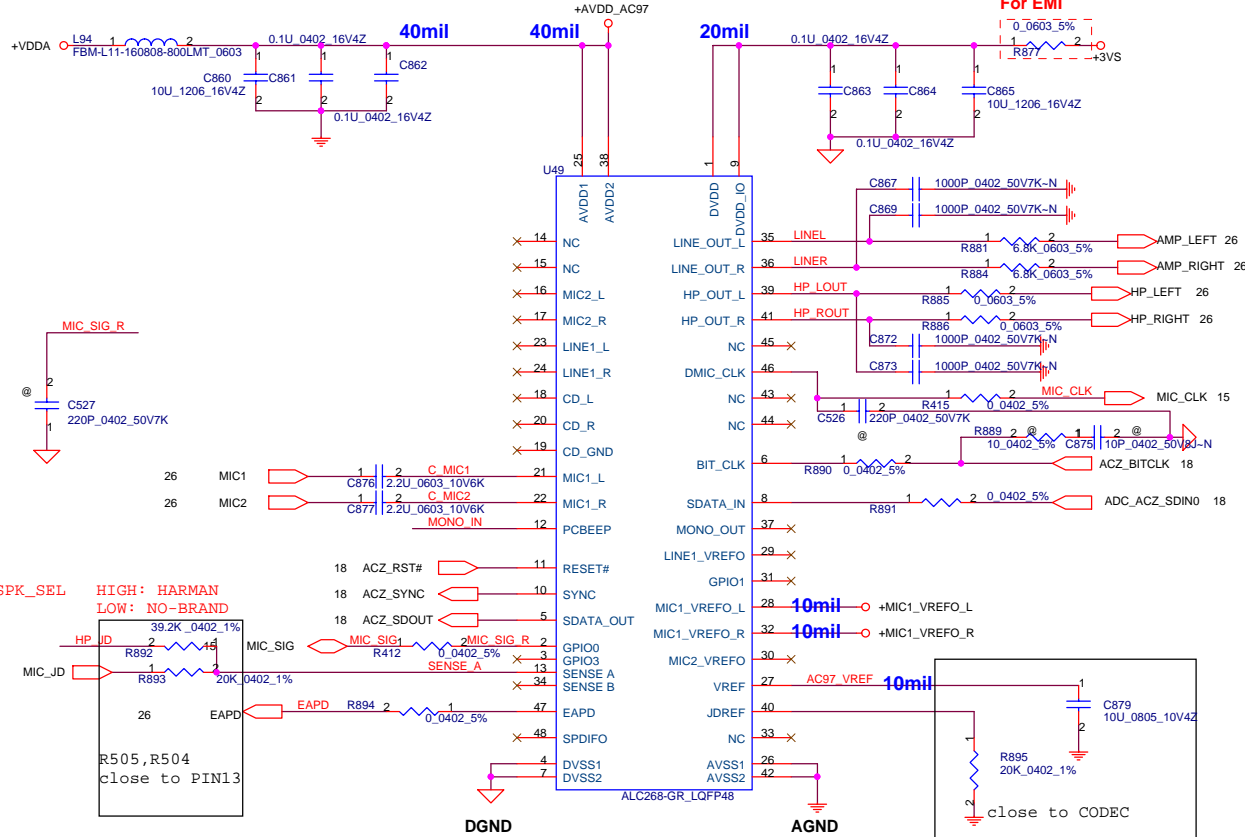


Power status(Left)

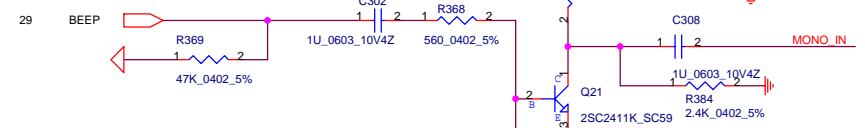


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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Mini-Card/LED	
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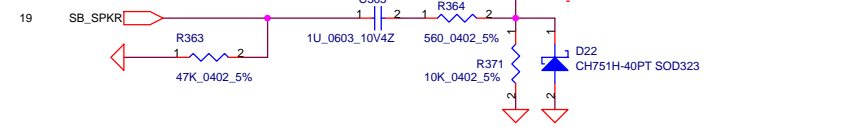
HD Audio Codec



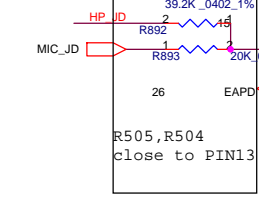
EC Bleep



ICH Bleep

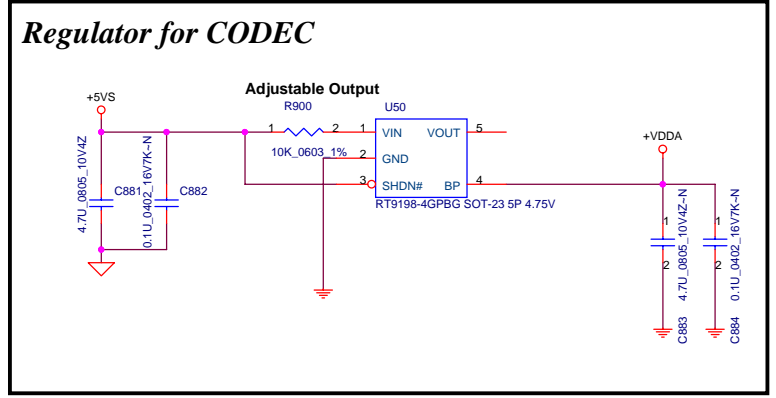
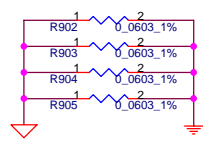


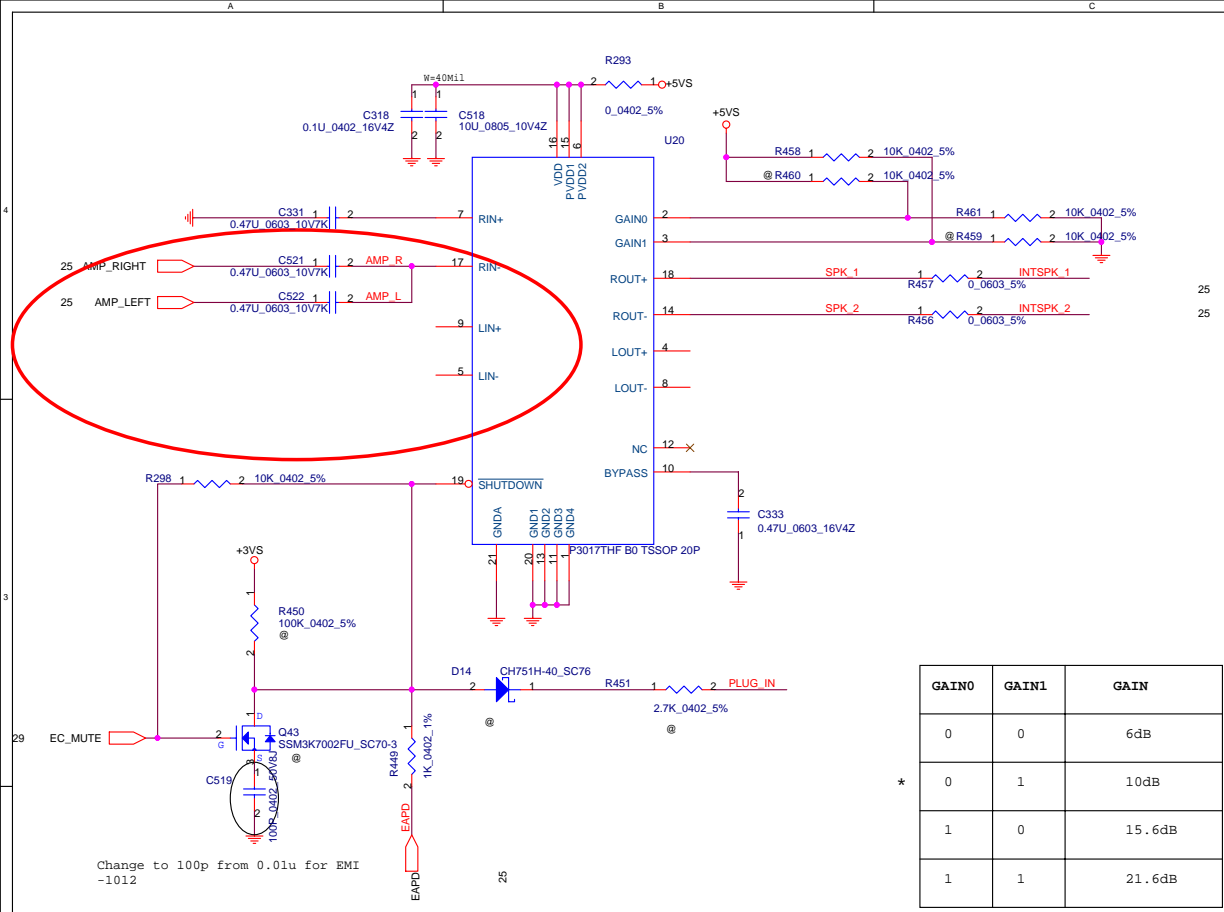
SPK_SEL
HIGH: HARMAN
LOW: NO-BRAND



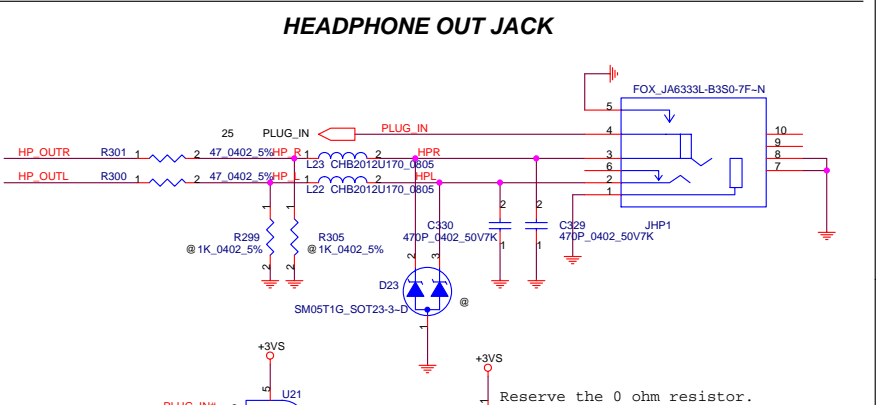
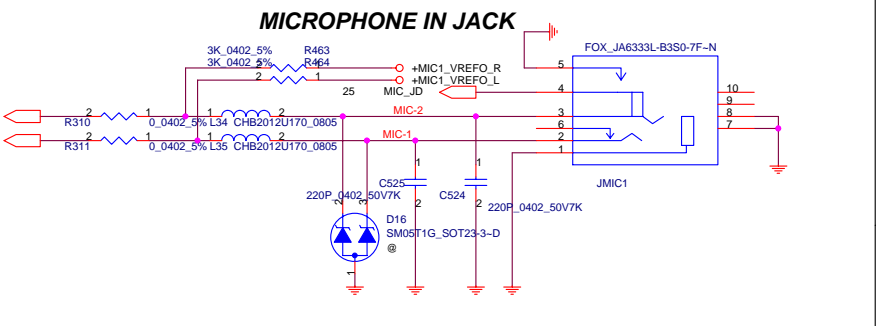
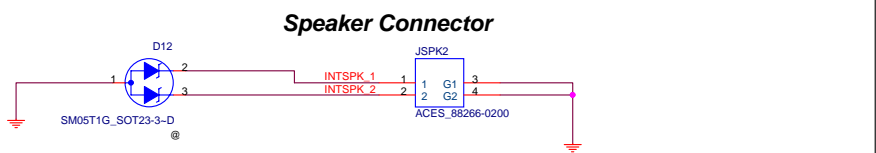
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
SENSE B	5.1K	PORT-D (PIN 35, 36)
	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Moat Bridge

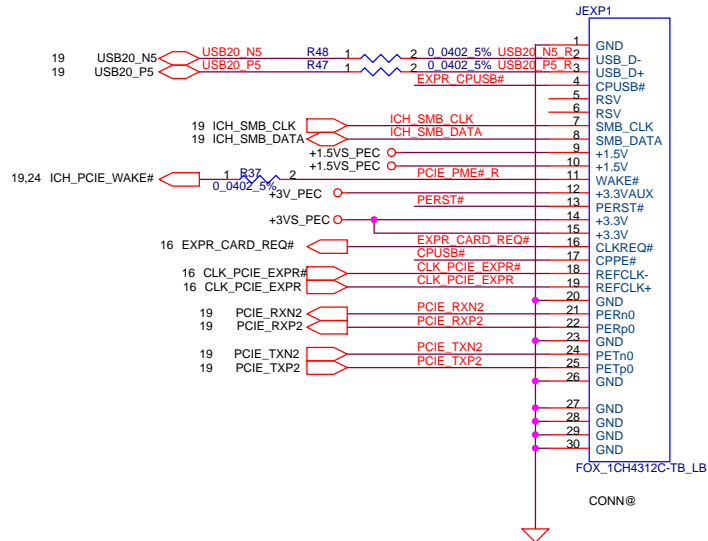
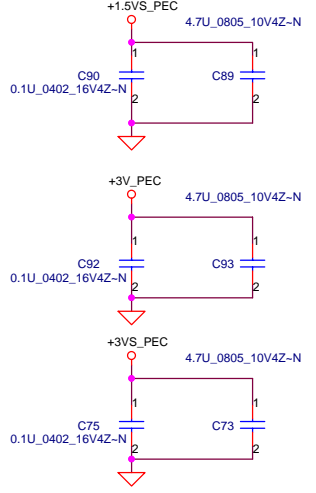
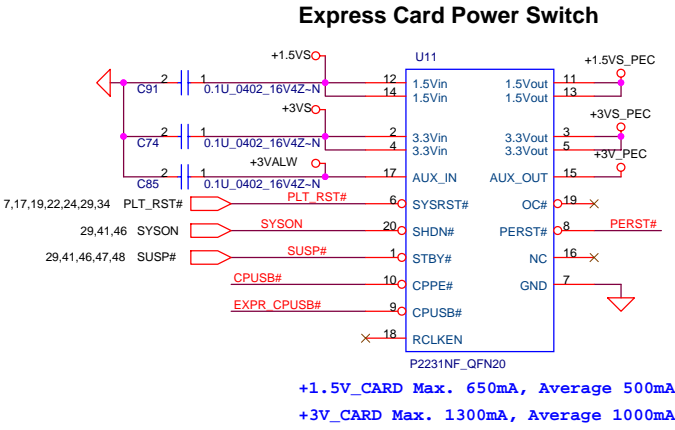




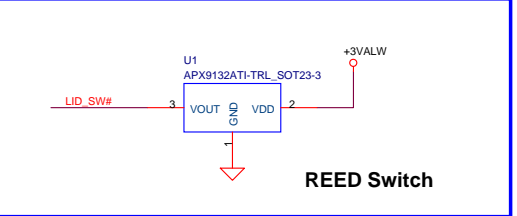
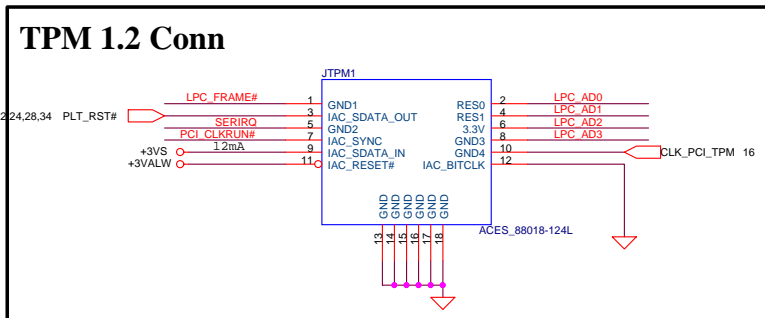
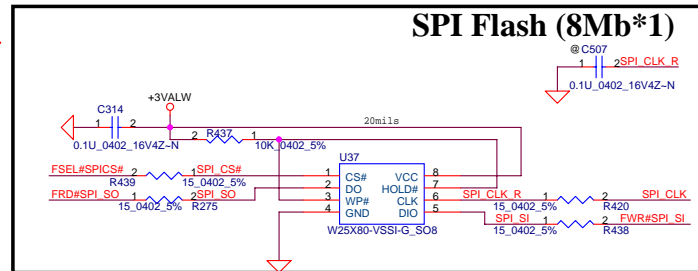
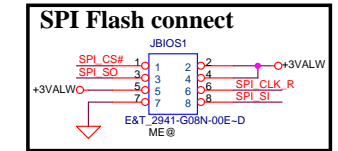
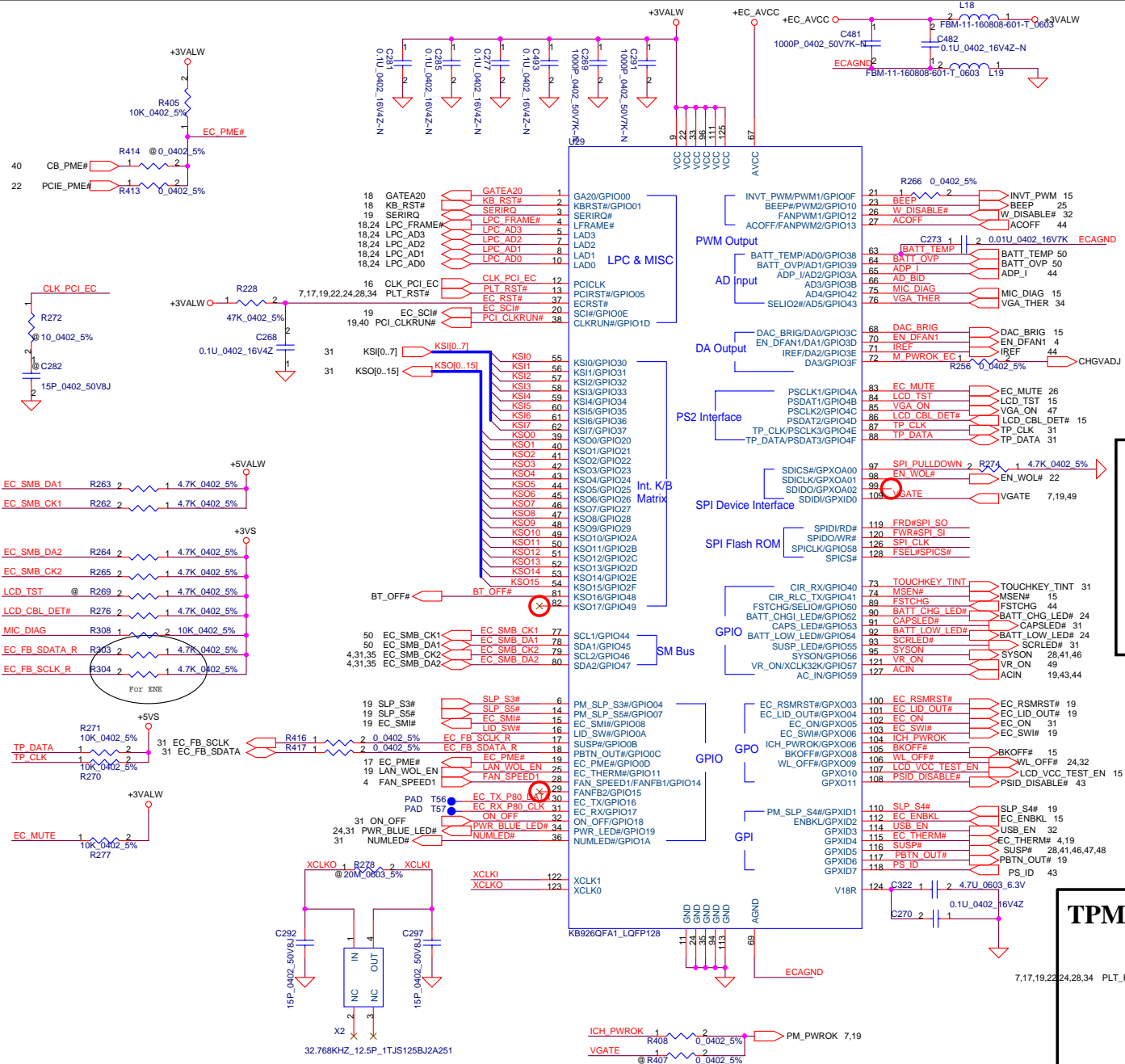
GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



Express card

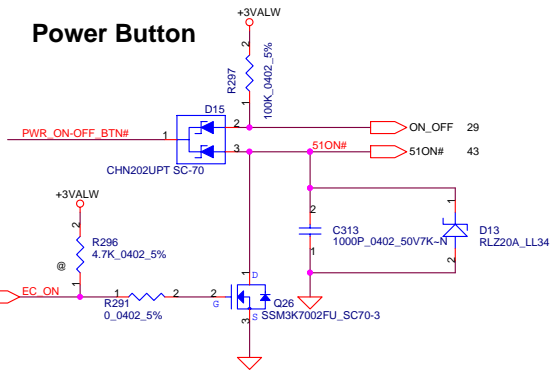


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				Rev	0.1

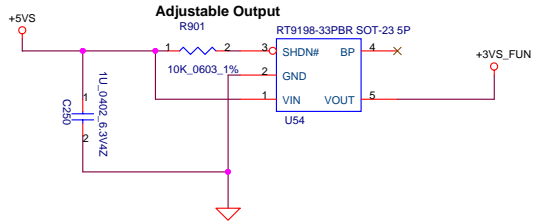


Security Classification	Compal Secret Data		0.5A pc	Compal Electronics, Inc.	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	
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				LA-4231P	0.1
				Date: Thursday, January 10, 2008	Sheet 29 of 49

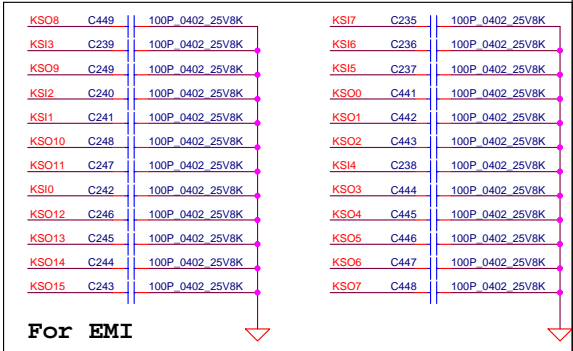
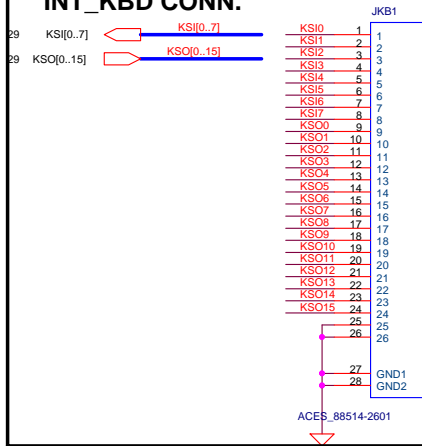
Power Button



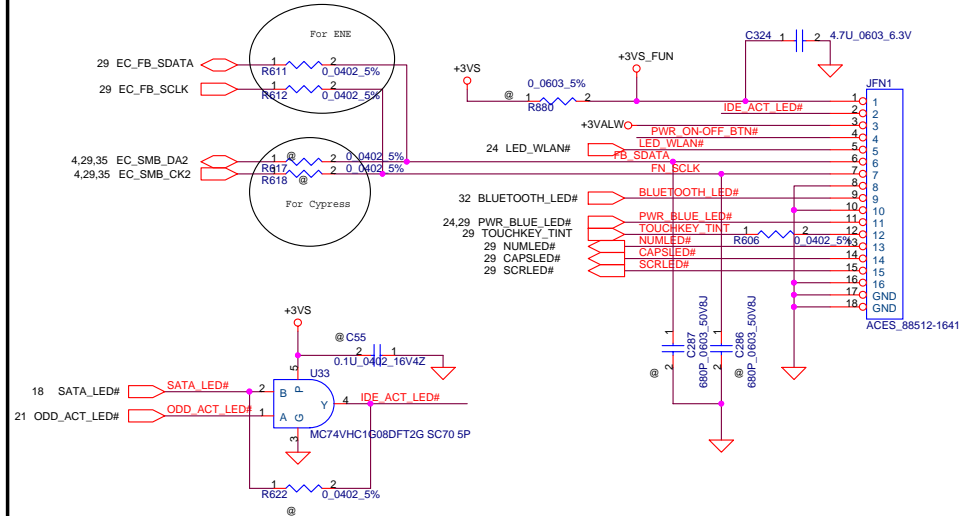
Regulator for ENE sensor



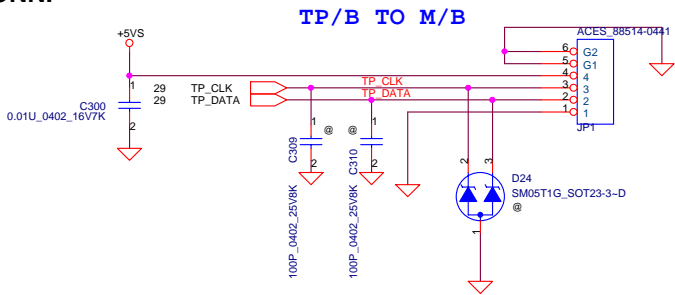
INT_KBD CONN.

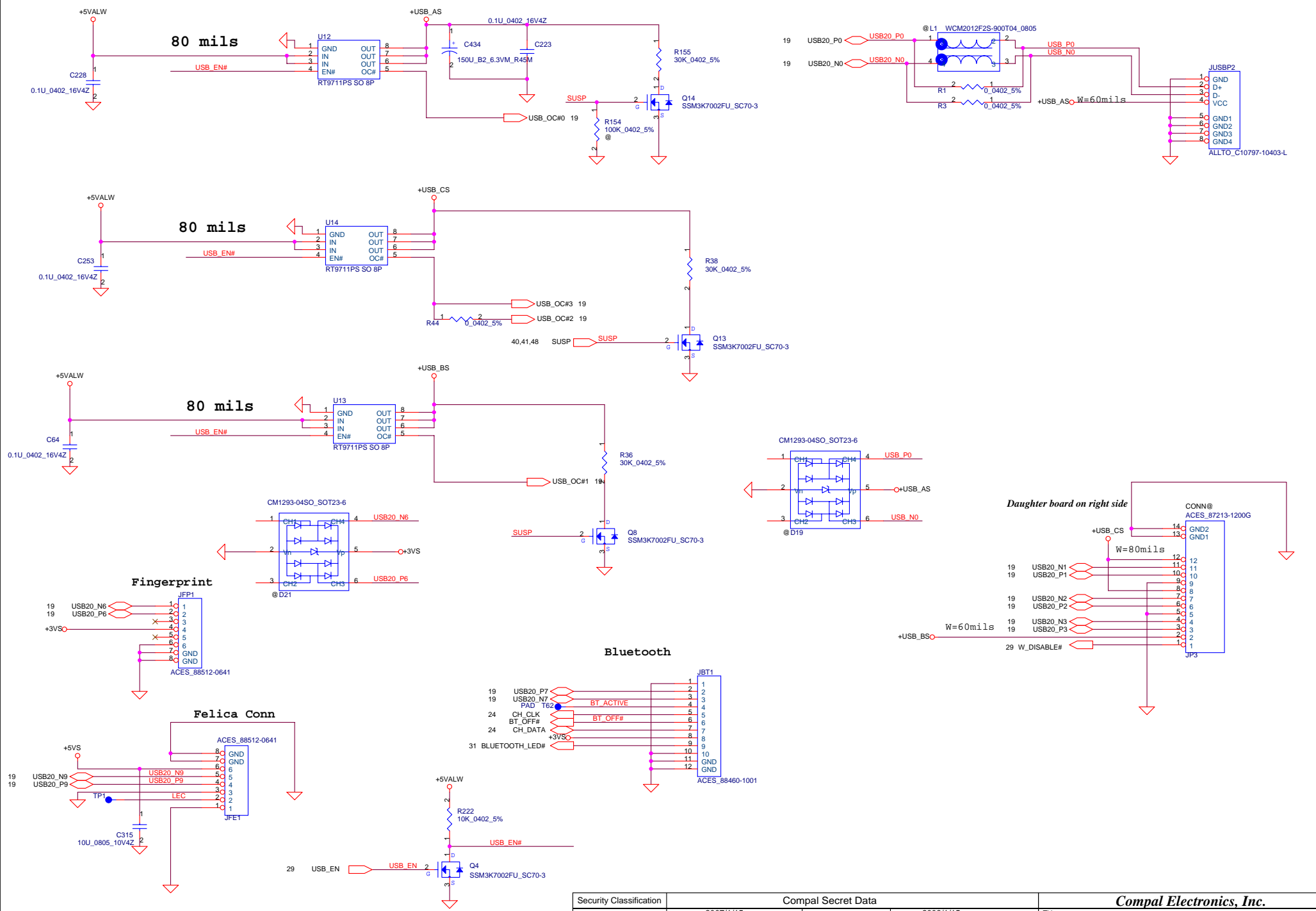


Function/B CONN.



Touch PAD/B CONN.





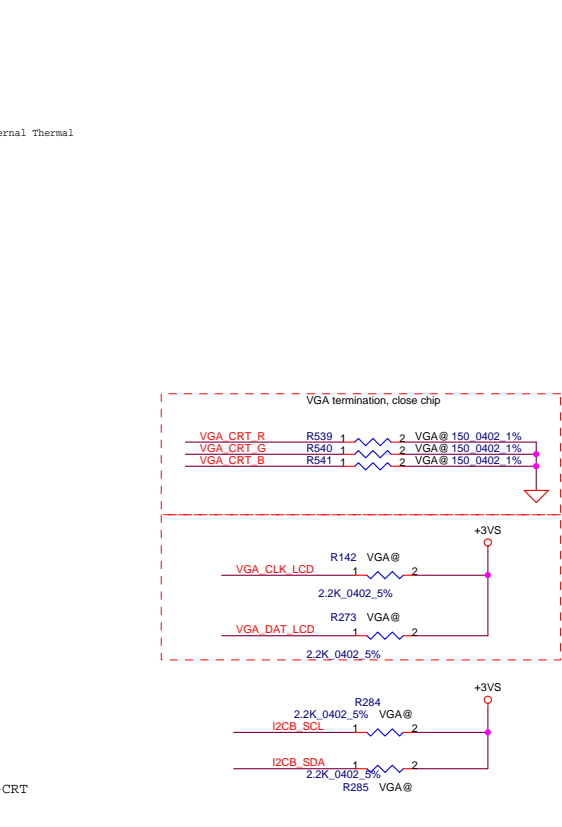
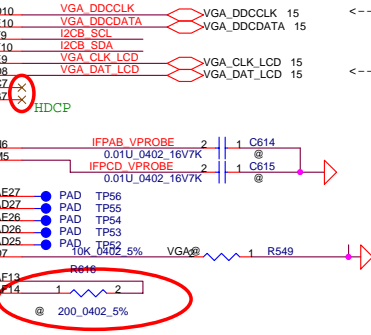
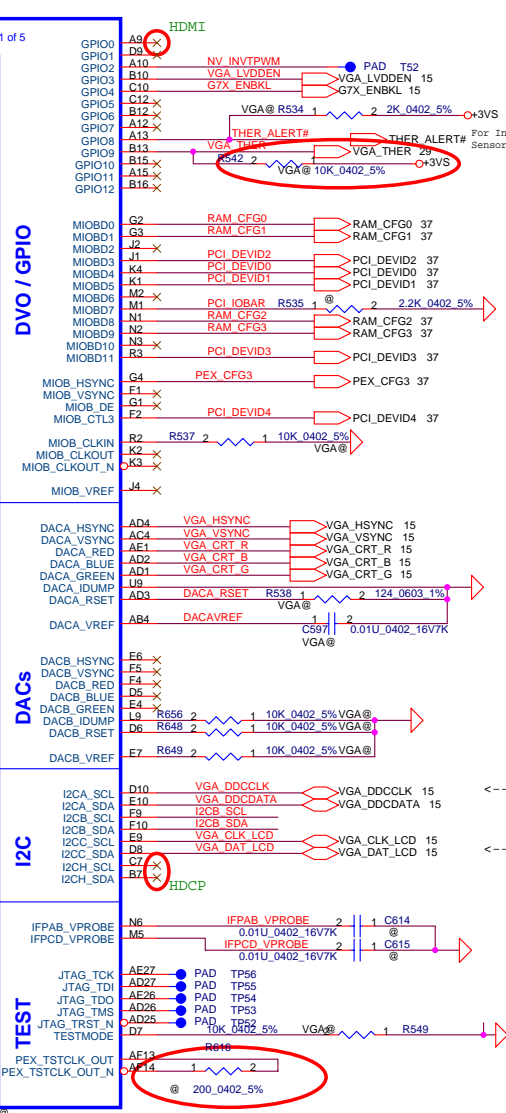
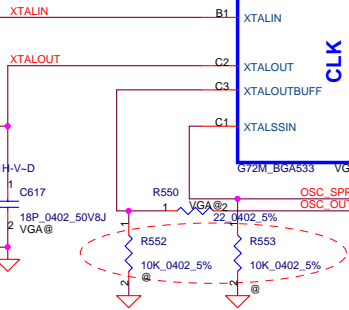
Security Classification	Compal Secret Data		Title	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	USB/BlueTooth/FP/Felcia
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Date:	Thursday, January 10, 2008	Sheet	32	of 49

9 PEG_NRX_GTX_P[0..15] ← PEG_NRX_GTX_P[0..15]
 9 PEG_NRX_GTX_N[0..15] ← PEG_NRX_GTX_N[0..15]
 9 PEG_NTX_GRX_P[0..15] ← PEG_NTX_GRX_P[0..15]
 9 PEG_NTX_GRX_N[0..15] ← PEG_NTX_GRX_N[0..15]

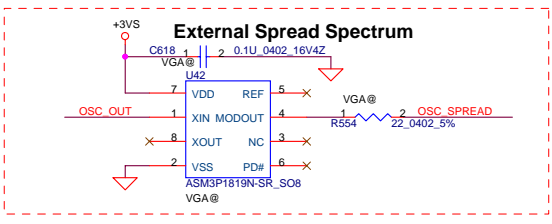
U38A
 PEG_NTX_GRX_P0 AF1
 PEG_NTX_GRX_P1 AG2
 PEG_NTX_GRX_P2 AG3
 PEG_NTX_GRX_P3 AG4
 PEG_NTX_GRX_P4 AF5
 PEG_NTX_GRX_P5 AG6
 PEG_NTX_GRX_P6 AF7
 PEG_NTX_GRX_P7 AF8
 PEG_NTX_GRX_P8 AG9
 PEG_NTX_GRX_P9 AG10
 PEG_NTX_GRX_P10 AF11
 PEG_NTX_GRX_P11 AG12
 PEG_NTX_GRX_P12 AF13
 PEG_NTX_GRX_P13 AG14
 PEG_NTX_GRX_P14 AF15
 PEG_NTX_GRX_P15 AG16
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 PEG_NTX_GRX_P17 AG18
 PEG_NTX_GRX_P18 AF19
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 PEG_NTX_GRX_P26 AF27

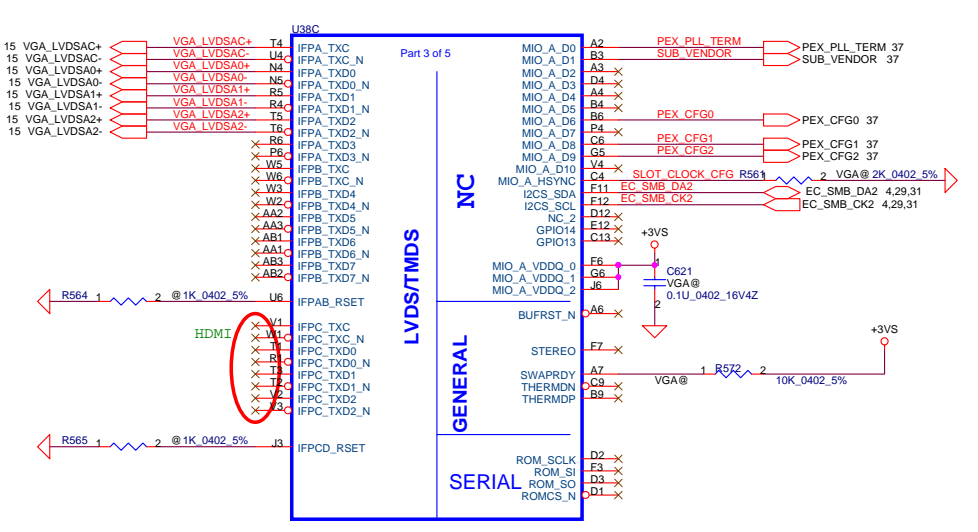
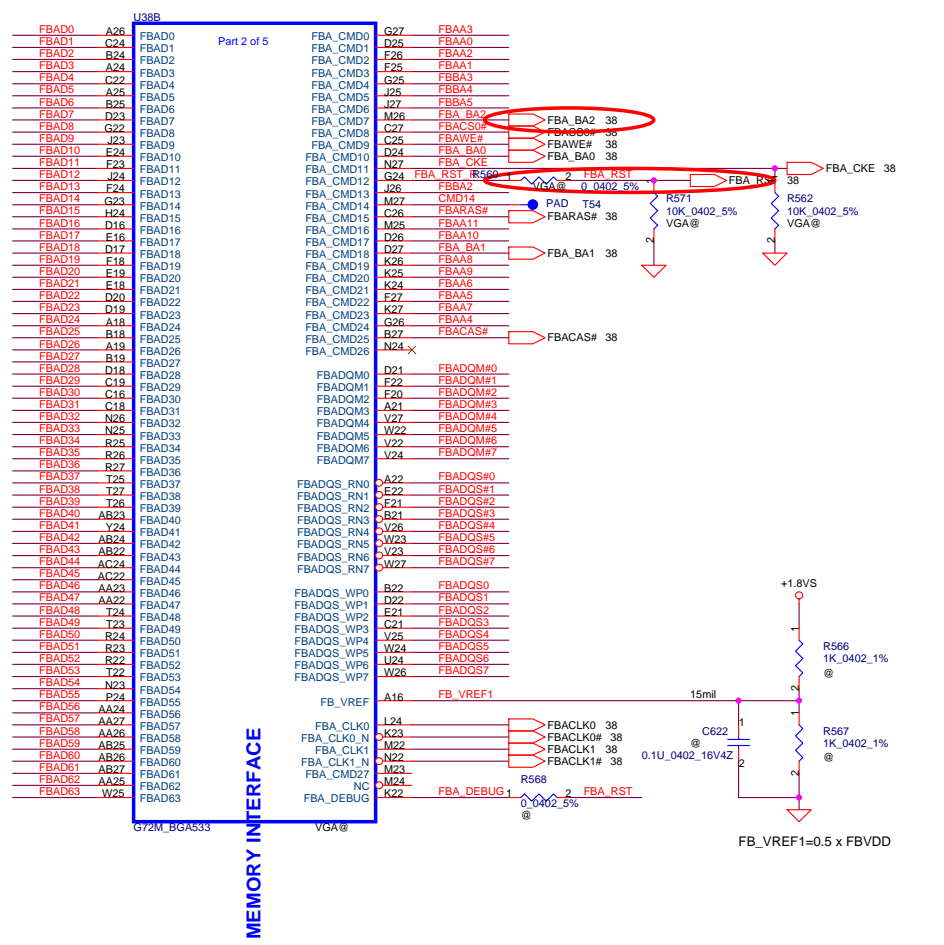
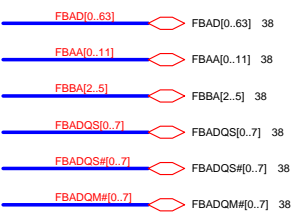
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PEG_NRX_GTX_N0	C582	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_N0	AD5	PEX_TX0_N
PEG_NRX_GTX_P1	C583	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_P1	AE6	PEX_TX1
PEG_NRX_GTX_N1	C584	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_N1	AE7	PEX_TX1_N
PEG_NRX_GTX_P2	C585	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_P2	AD7	PEX_TX2
PEG_NRX_GTX_N2	C586	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_N2	AC7	PEX_TX2_N
PEG_NRX_GTX_P3	C587	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_P3	AE9	PEX_TX3
PEG_NRX_GTX_N3	C588	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_N3	AE10	PEX_TX3_N
PEG_NRX_GTX_P4	C589	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_P4	AD10	PEX_TX4
PEG_NRX_GTX_N4	C590	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_N4	AC10	PEX_TX4_N
PEG_NRX_GTX_P5	C591	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_P5	AE12	PEX_TX5
PEG_NRX_GTX_N5	C592	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_N5	AE13	PEX_TX5_N
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PEG_NRX_GTX_N8	C599	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_N8	AE16	PEX_TX8_N
PEG_NRX_GTX_P9	C600	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_P9	AC18	PEX_TX9
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PEG_NRX_GTX_N15	C613	1	2	VGA@0.1U_0402_16V7K	PEG_NRX_C_GTX_N15	AD24	PEX_TX15_N

16 CLK_PCIE_VGA
 16 CLK_PCIE_VGA#
 7,17,19,22,24,28,29 PLT_RST#

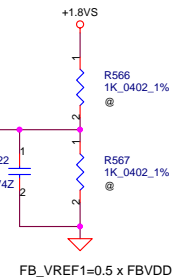


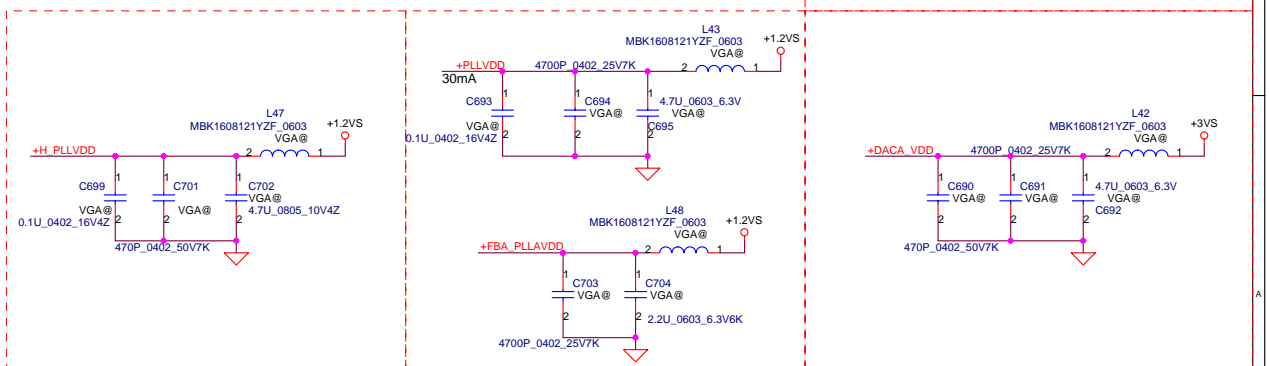
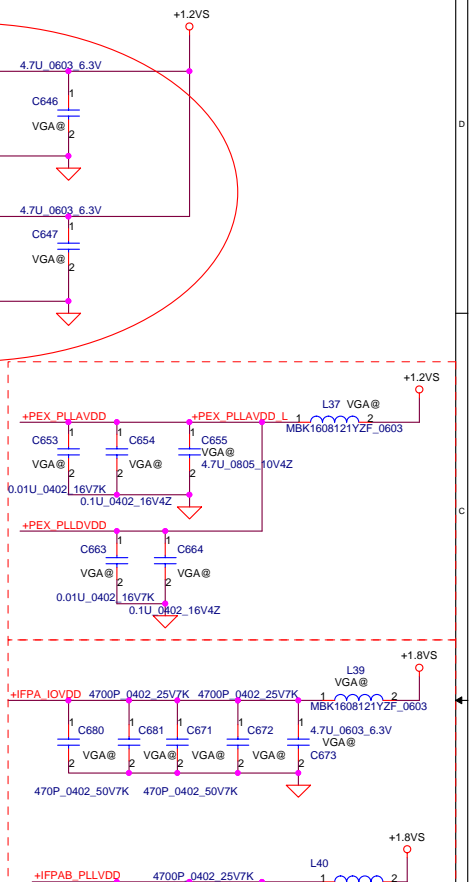
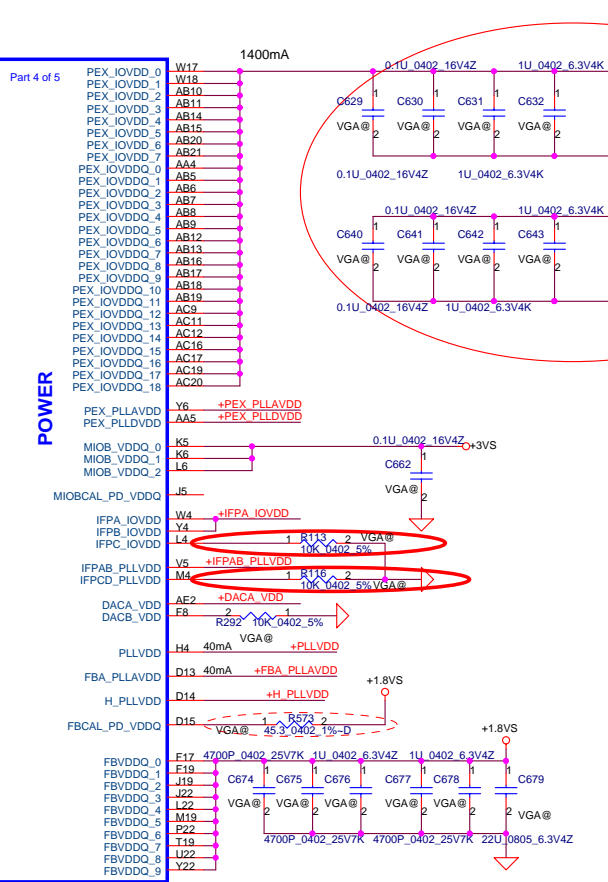
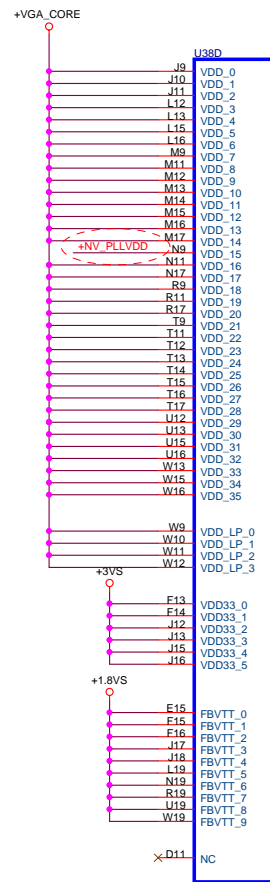
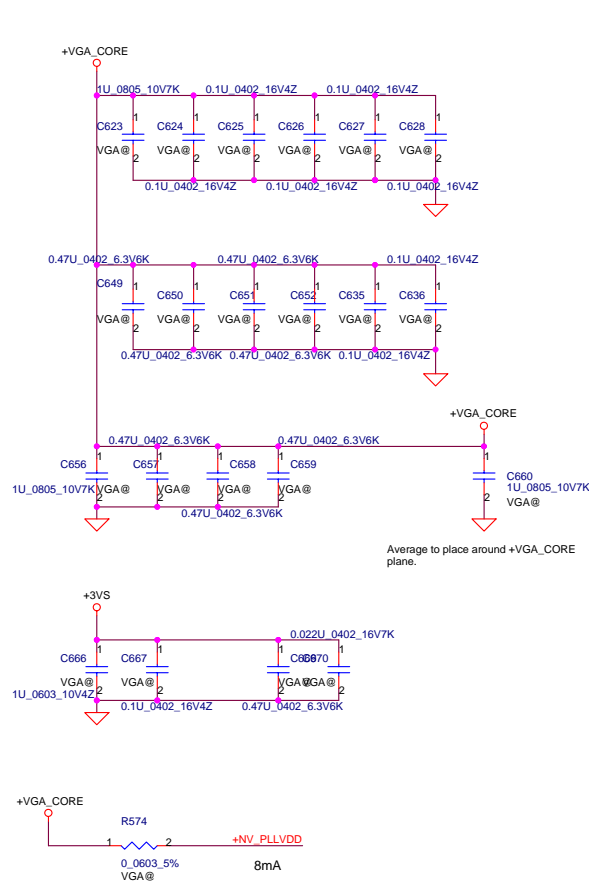
PCI_IOBAR	NB8M
0	Disable
1	Enable(Default)
BAR2_SIZE	NB8M
0	32Mb(Default)
1	16Mb



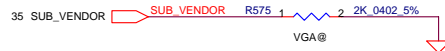
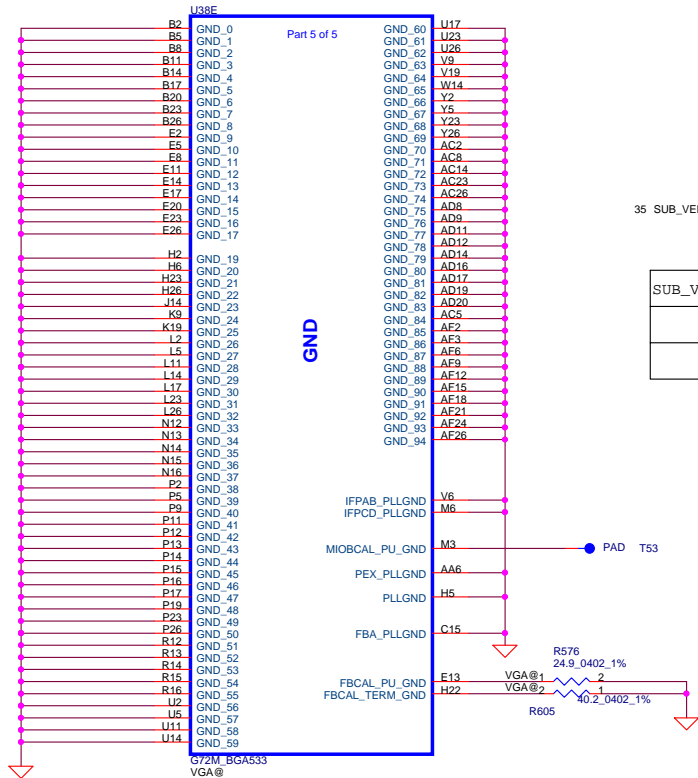


SLOT_CLOCK_CFG	SHARE REFERENCE CLOCK
0	Disable
1	Enable(Default)



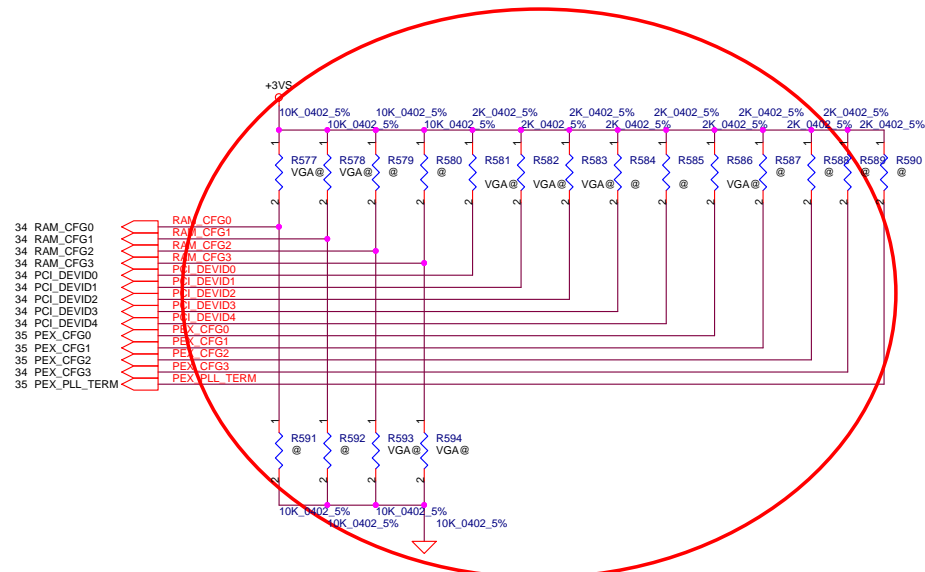


Security Classification				Compal Secret Data		Title	
Issued Date	2006/07/10	Deciphered Date	2007/07/10	NB8M-GS Power			
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				36	0.1	Sheet 36 of 49	



SUB_VENDOR	
0	NO VIDEO BIOS ROM
1	BIOS ROM is present(Default)

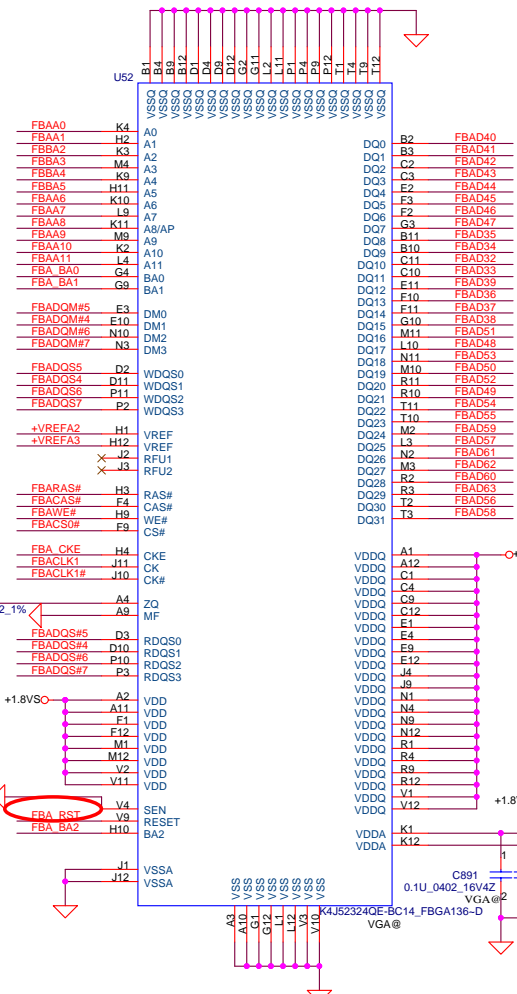
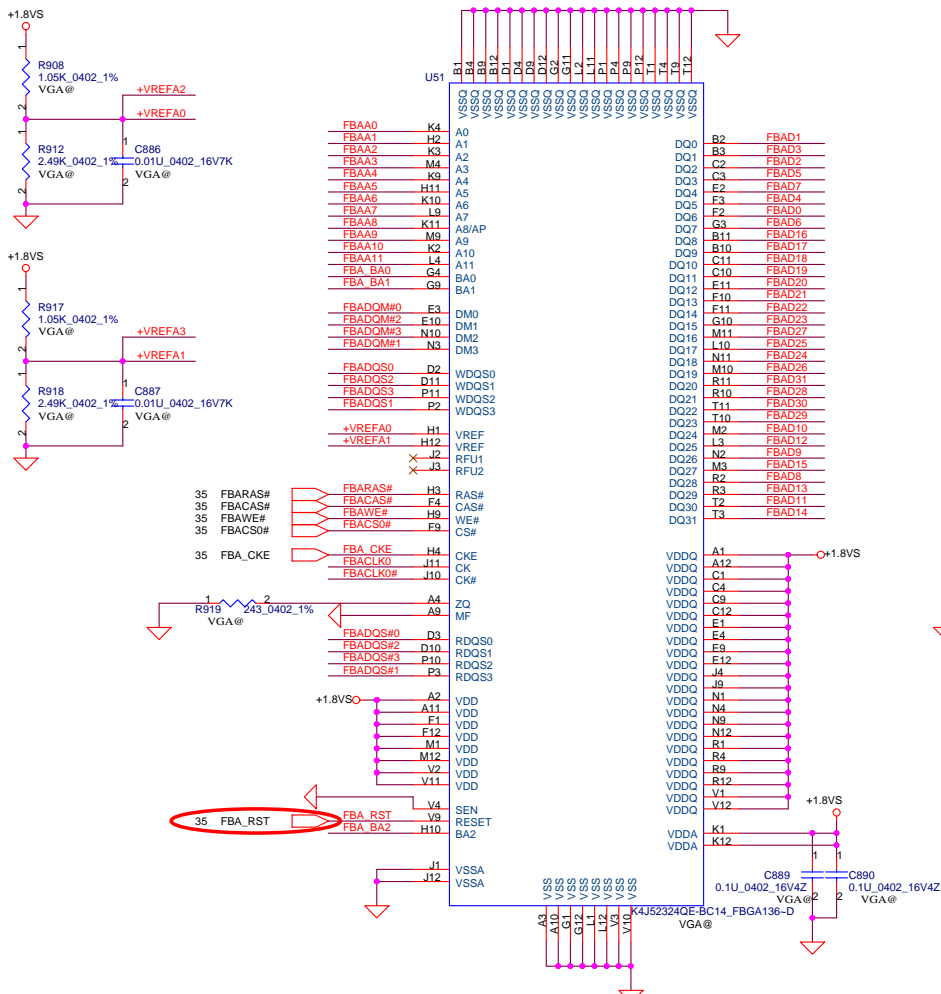
STRAPS	PIN	DESCRIPTION	Value	Value
SUB_VENDOR	MIO_A_D1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0	
PEX_PLL_TERM	MIO_A_D0	PCI-E PLL termination 0---->Enable (Default) 1---->Disable	0	
PEX_CFG[3:0]	MIOAD [9,8,6] MIOBD_HSYNC	Recommended for G8x	0001	
RAM_CFG[3:0]	MIOAD0 MIOAD1 MIOAD8 MIOAD9	0001 ----> qimonda 16Mx32 0010 ----> Hynix 16Mx32 0011 ----> Samsung 16Mx32	0011	
PCI_DEVID[3:0]	VIPD[5:3] MIOA_HSYNC	G73M-xxxx8 G72M-0x01D8 NB8M-GS : 0X0427 NB8M-SE : 0X0428	0111 1000	
		G72MV-0x01D7 TBD/TBD	0111	



Bandwidth	RAM Type	Vendor
FULL R17	32M R11	Samsung R20, R19
HALF R12	16M R16	Hynix R18, R19
		Infineon R18, R21

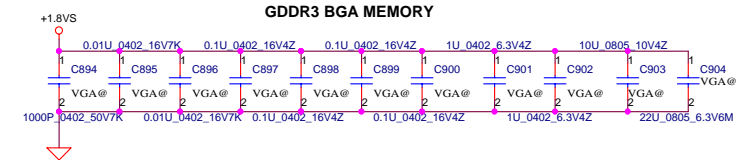
Package		
(10*12.5)	Infineon GDDR2(400): SA0000S800 (HYB18T256161AFL-25)	Infineon GDDR2(350): SA0000T700 (HYB18T256161AF-28)
(11*13)	Samsung GDDR2 (400): SA0000FG10 (K4N56163QF-ZC25)	Samsung GDDR2 (350): SA0000TB00 (K4N56163QF-ZC2A)
(8*13)	Hynix GDDR2 (400): SA0000FF10 (HY5PS561621AFP-25)	Hynix GDDR2 (350): SA0000TJ00 (HY5PS561621AFP-28)

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				Rev 0.1

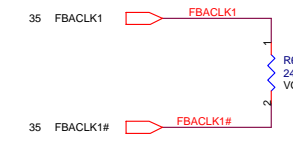
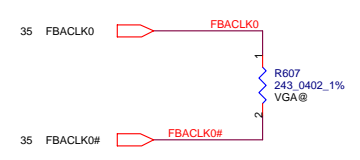
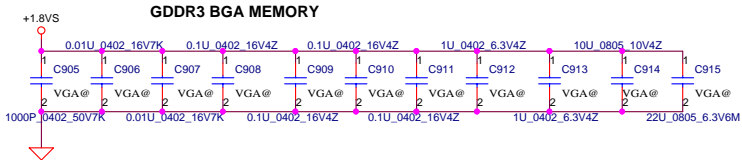


- 35 FBAD[0..63] FBAD[0..63]
- 35 FBADQS#[0..7] FBADQS#[0..7]
- 35 FBADQS[0..7] FBADQS[0..7]
- 35 FBADQM#[0..7] DGMA#[0..7]
- 35 FBAA[0..11] FBAA[0..11]
- 35 FBAA[2..5] FBAA[2..5]
- 35 FBA_BA0 FBA_BA0
- 35 FBA_BA1 FBA_BA1
- 35 FBA_BA2 FBA_BA2

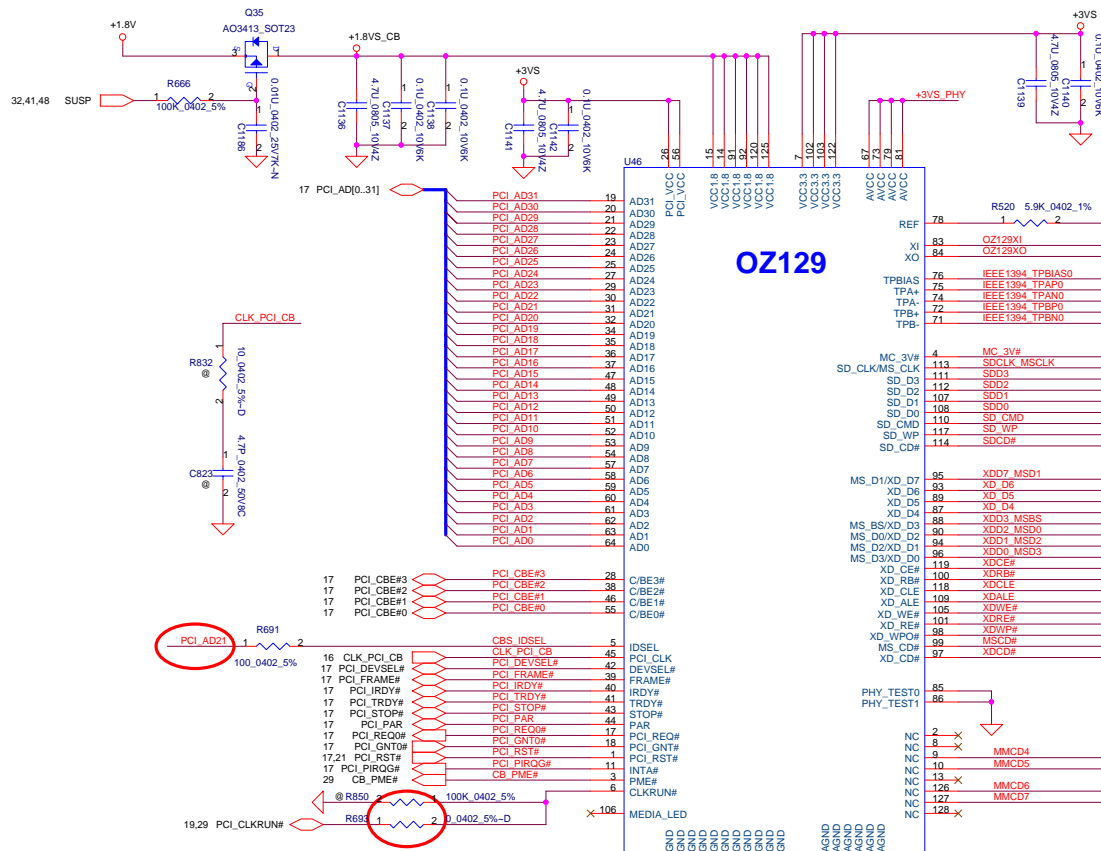
GDDR3 BGA MEMORY



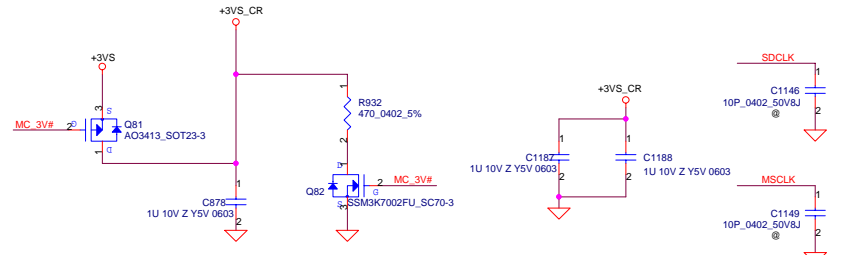
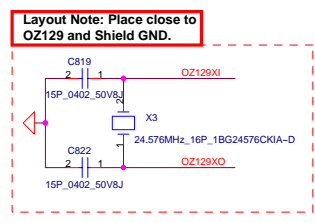
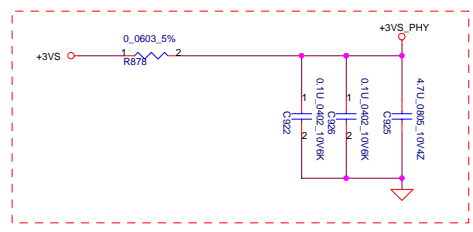
GDDR3 BGA MEMORY



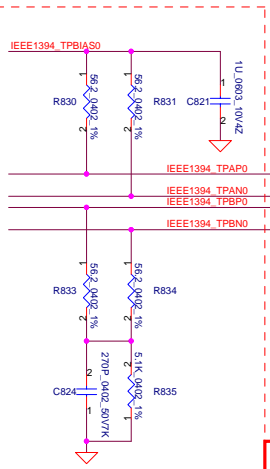
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2007/02/12	Deciphered Date	2008/02/12	VRAM GDDR3 A	
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Document Number			Rev		
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OZ129



LED behave:
 Idle -> low
 Access data -> always high

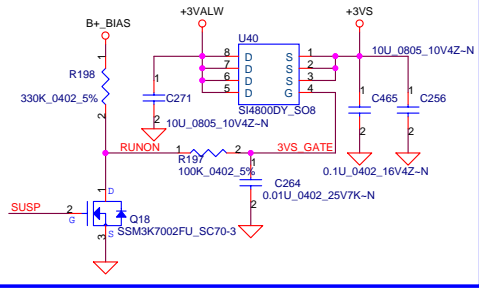


Layout Note: Place close to OZ129 Chipset.

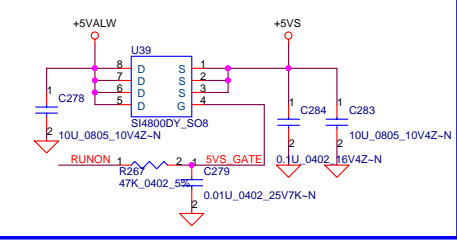
Pin	Signal	Value	Pin	Signal	Value
XDD0_MSD3	R873	2 0.0402 5%-D	XDD0	32	XD-D0
XDD1_MSD2	R874	2 0.0402 5%-D	XDD1	33	XD-D1
XDD2_MSD0	R938	2 0.0402 5%-D	XDD2	10	XD-D2
XDD3_MSBS	R948	2 0.0402 5%-D	XDD3	8	XD-D3
XD_D4	R957	2 0.0402 5%-D	XDD4	7	XD-D4
XD_D5	R944	2 0.0402 5%-D	XDD5	6	XD-D5
XD_D6	R941	2 0.0402 5%-D	XDD6	5	XD-D6
XDD7_MSD1	R951	2 0.0402 5%-D	XDD7	4	XD-D7
XDWE#	R960	2 0.0402 5%-D	XDWE	34	XD-WE
XDWP#	R967	2 0.0402 5%-D	XDWP	33	XD-WP
XDAL	R945	2 0.0402 5%-D	XD_ALE	35	XD-ALE
XDCD#	R955	2 0.0402 5%-D	XDCD	40	XD-CD
XDRB#	R952	2 0.0402 5%-D	XDRB	39	XD-RB
XDR#	R961	2 0.0402 5%-D	XDR	38	XD-RE
XDC#	R956	2 0.0402 5%-D	XDC	37	XD-CE
XDCLE	R946	2 0.0402 5%-D	XD_CLE	36	XD-CLE
MS-DAT0	R958	1 2 0.0402 5%-D	XDD2_MSD0		
MS-DAT1	R943	1 2 0.0402 5%-D	XDD1_MSD2		
MS-DAT2	R942	1 2 0.0402 5%-D	XDD0_MSD3		
MS-DAT3	R954	1 2 0.0402 5%-D	XDD0_MSD3		

Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2007/09/01	Deciphered Date	2008/09/01	OZ129 Card Reader / 1394	
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			Customer	LA-4131P	0.1
			Date:	Thursday, January 10, 2008	Sheet 40 of 40

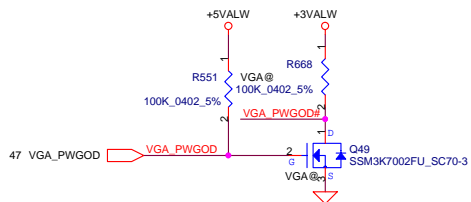
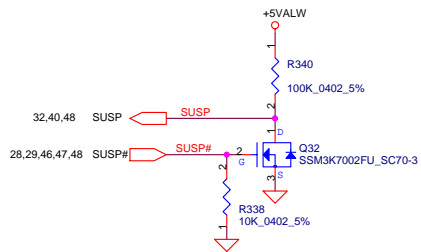
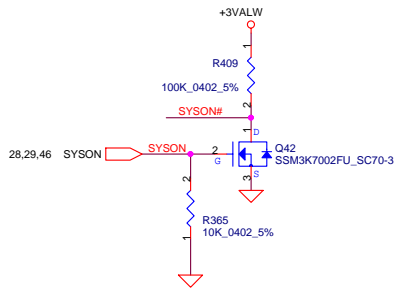
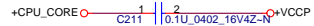
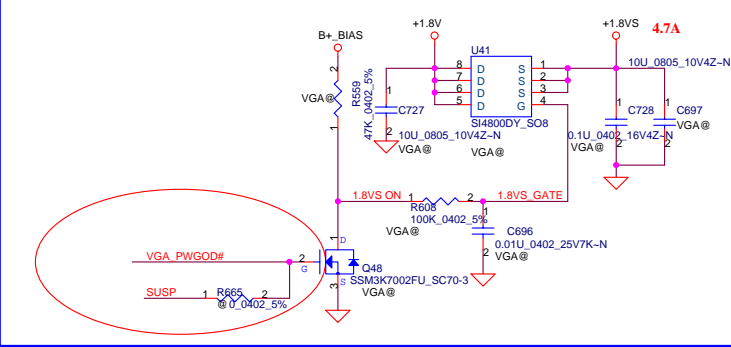
+3VALW to +3VS Transfer



+5VALW to +5VS Transfer

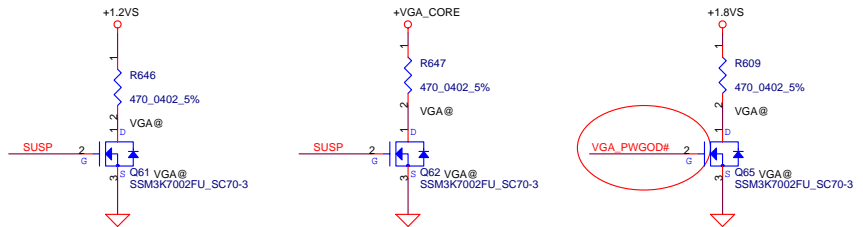


+1.8V to +1.8VS Transfer

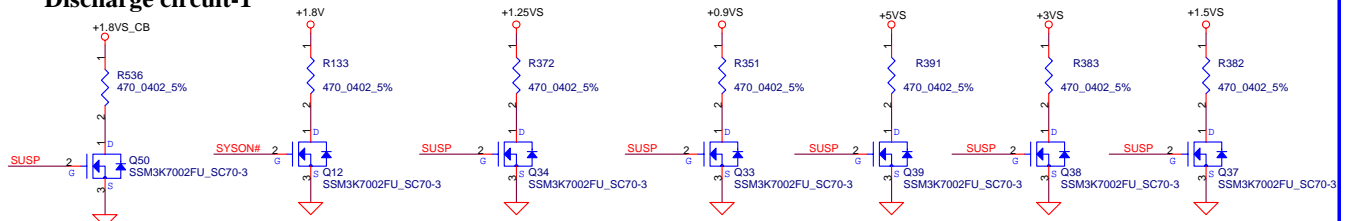


SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

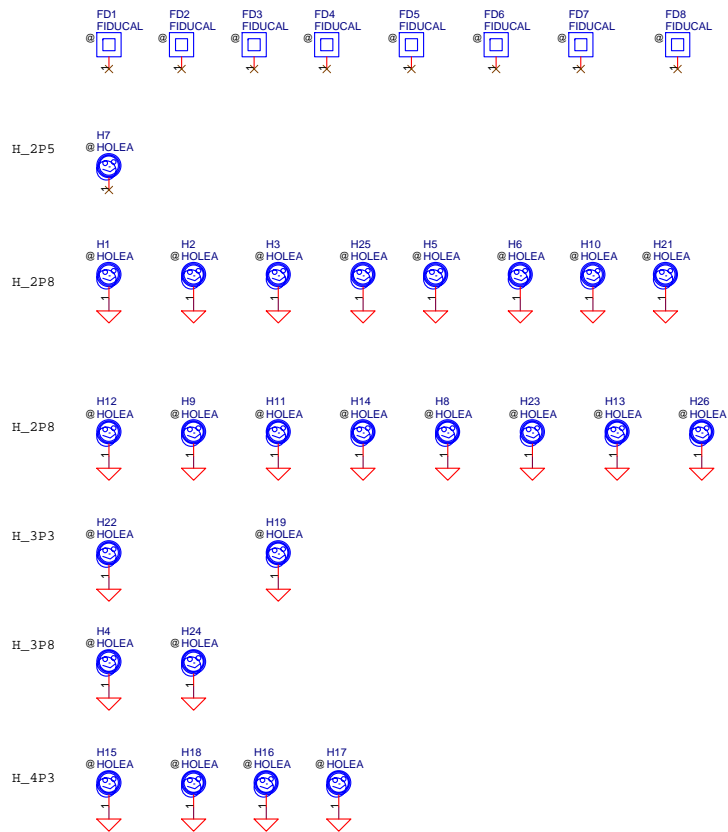
VGA Discharge circuit



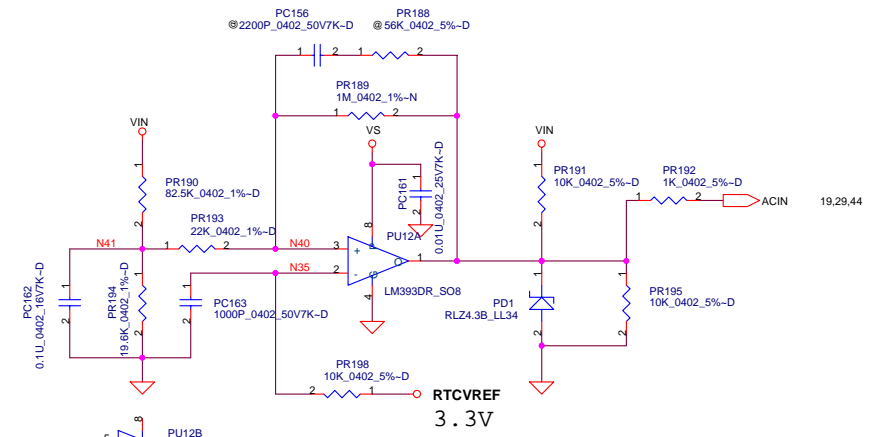
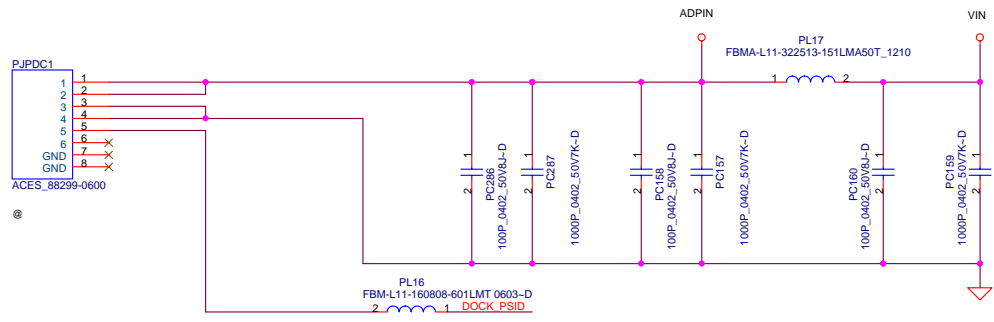
Discharge circuit-1



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Date:	Thursday, January 10, 2008	Sheet	41	of 49

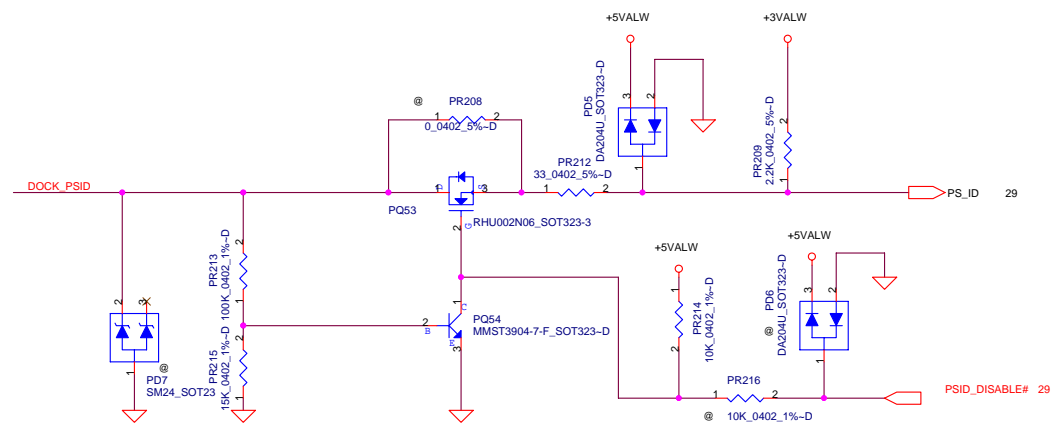
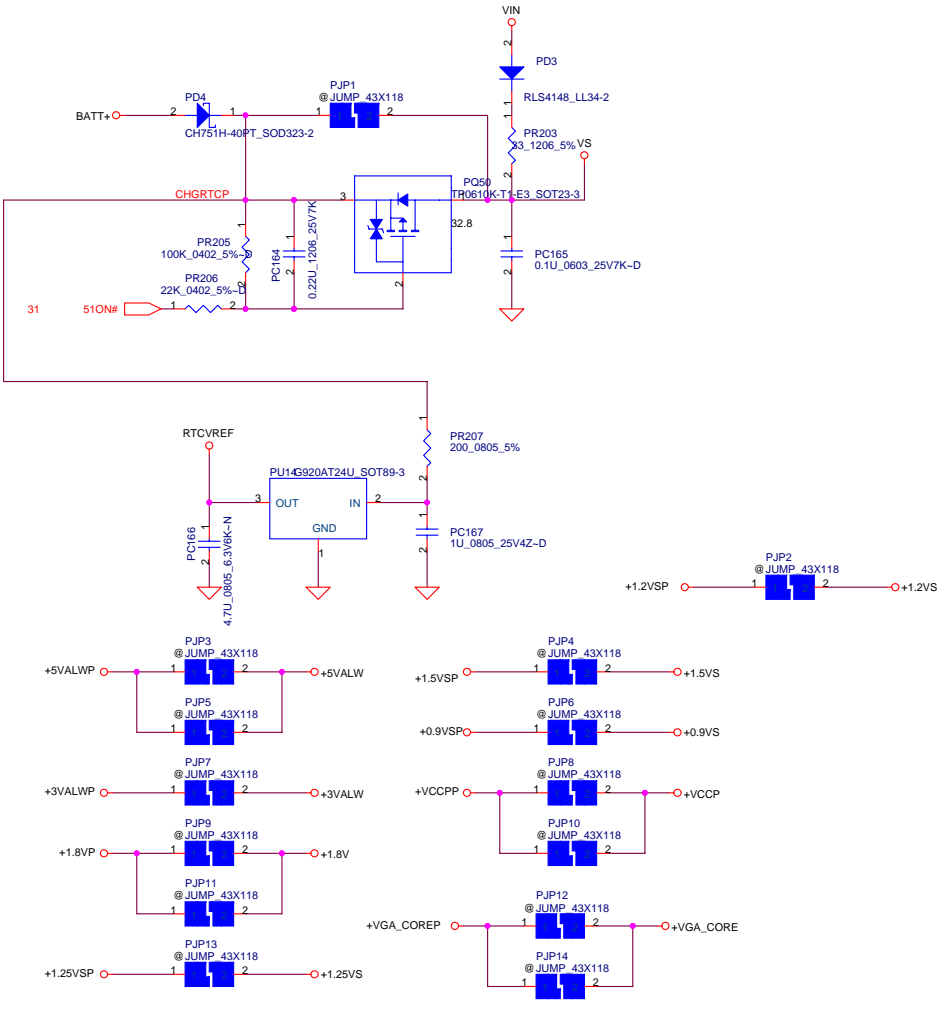


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				Customer	LA-4231P
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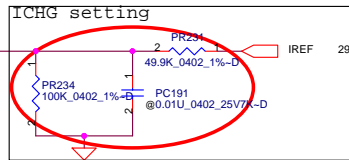
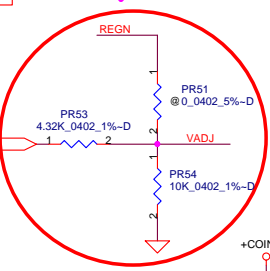
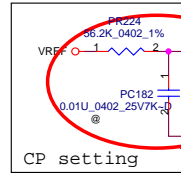
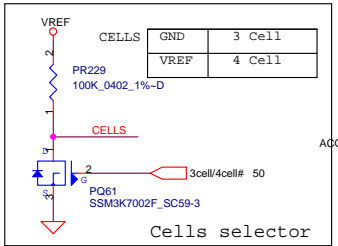


Vin Detector

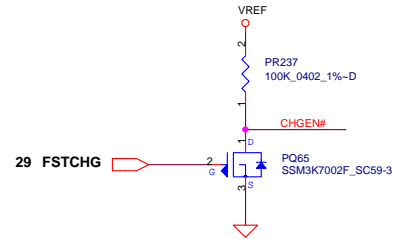
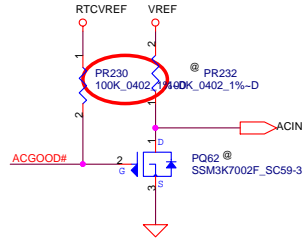
	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813



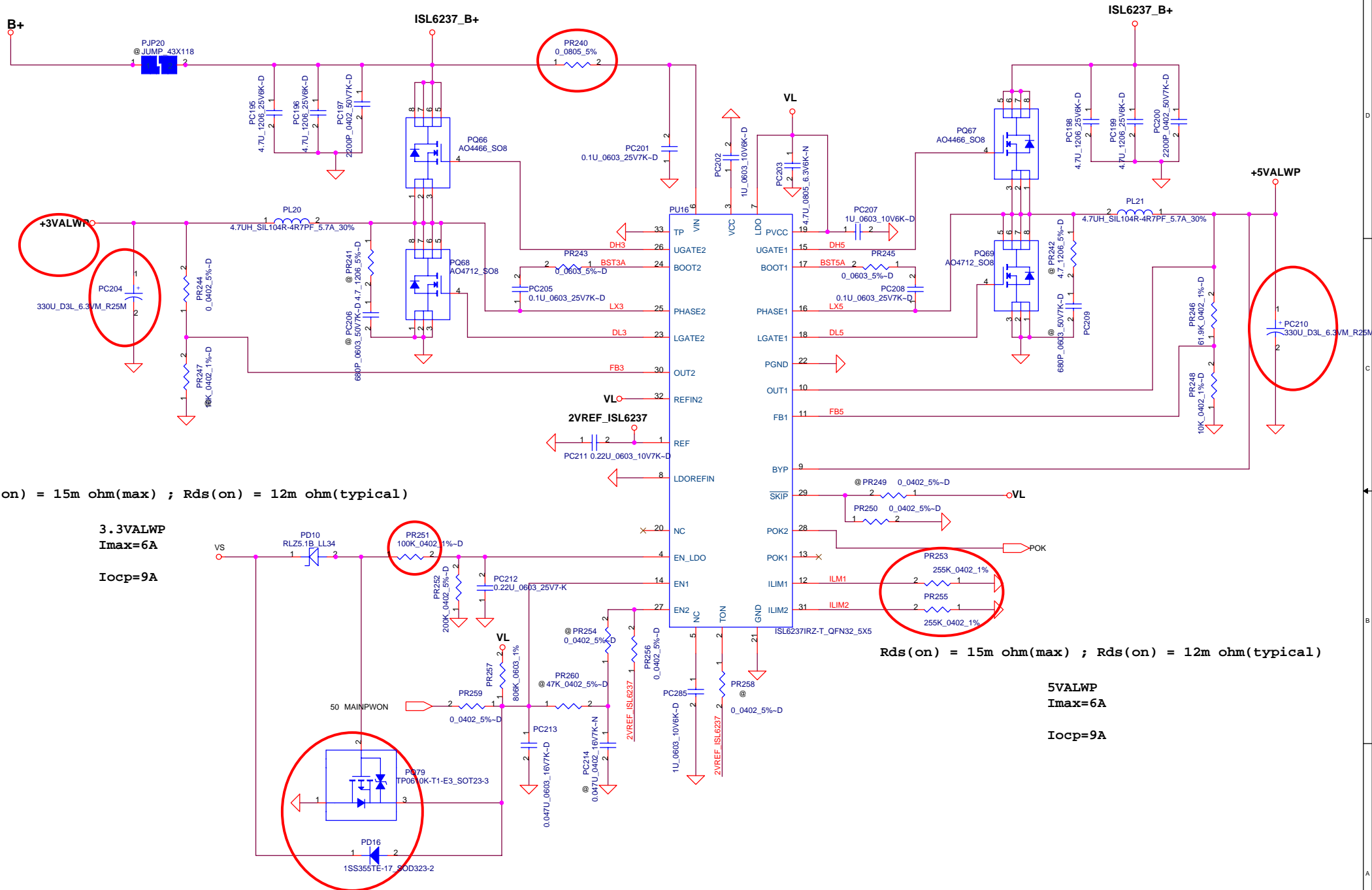
90W adapter
 $I_{charge} = (V_{rsrvt} / V_{vdac}) * (0.1 / PR222) = 3.3A$
 $I_{adapter} = (V_{vacst} / V_{vdac}) * (0.1 / PR217) = 3.65A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz



IREF	Current
2.968V	3A



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Date:	Thursday, January 10, 2008	Sheet	44	of	9	Rev	0.2



Rds(on) = 15m ohm(max) ; Rds(on) = 12m ohm(typical)

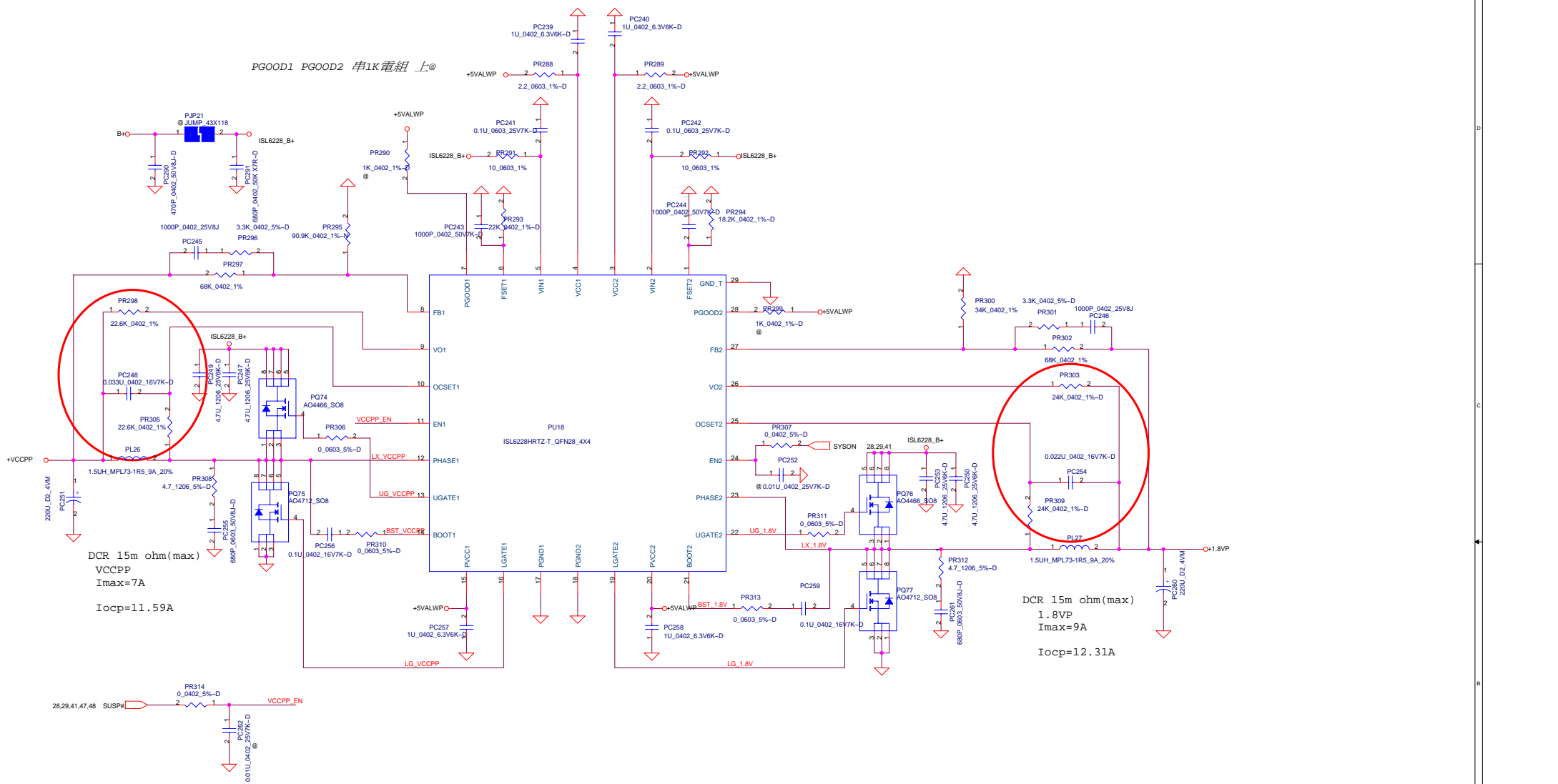
3.3VALWP
 Imax=6A
 Iocp=9A

Rds(on) = 15m ohm(max) ; Rds(on) = 12m ohm(typical)

5VALWP
 Imax=6A
 Iocp=9A

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				Custom	0.2
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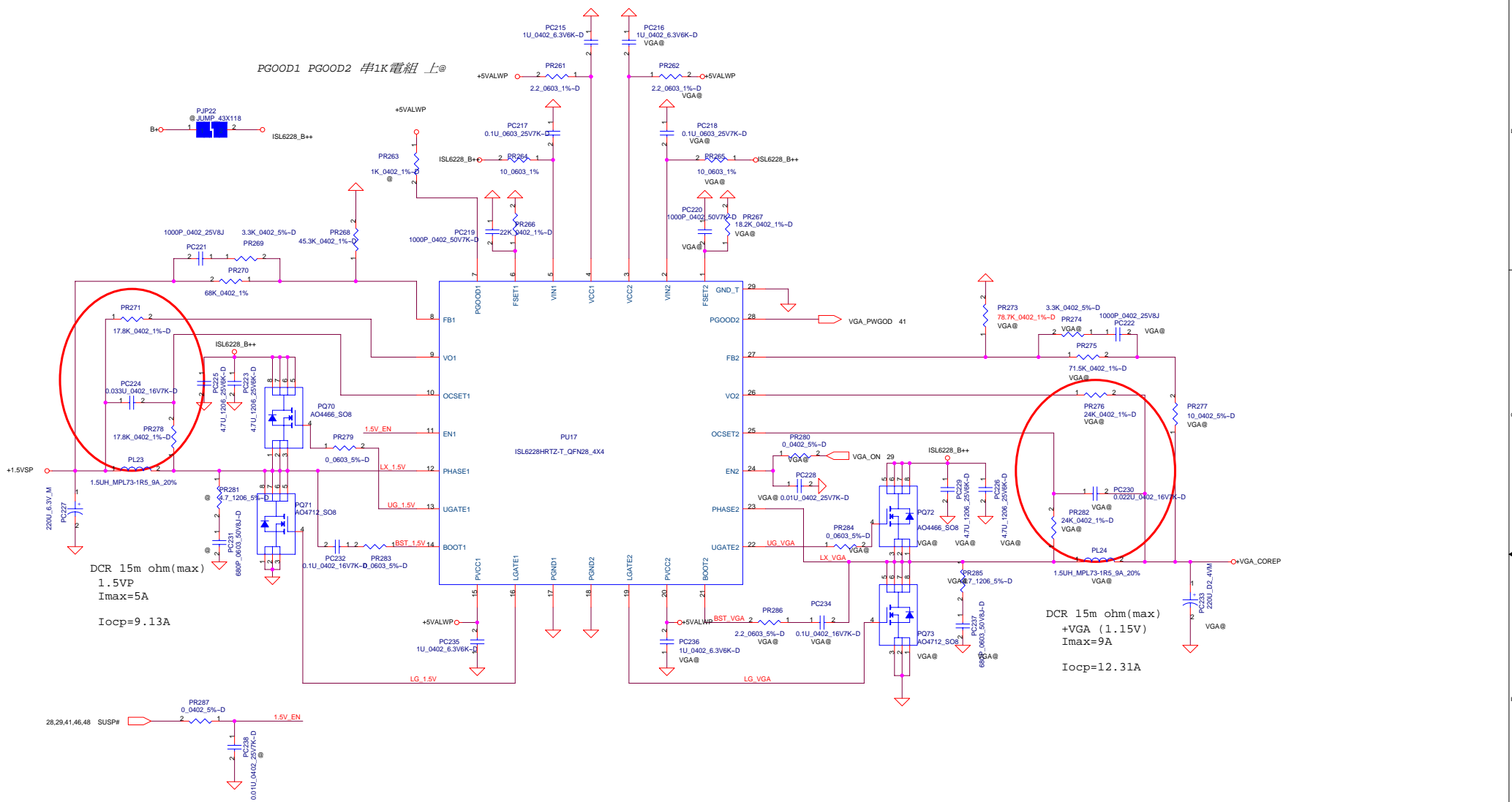


DCR 15m ohm(max)
 VCCPP
 I_{max}=7A
 I_{ocp}=11.59A

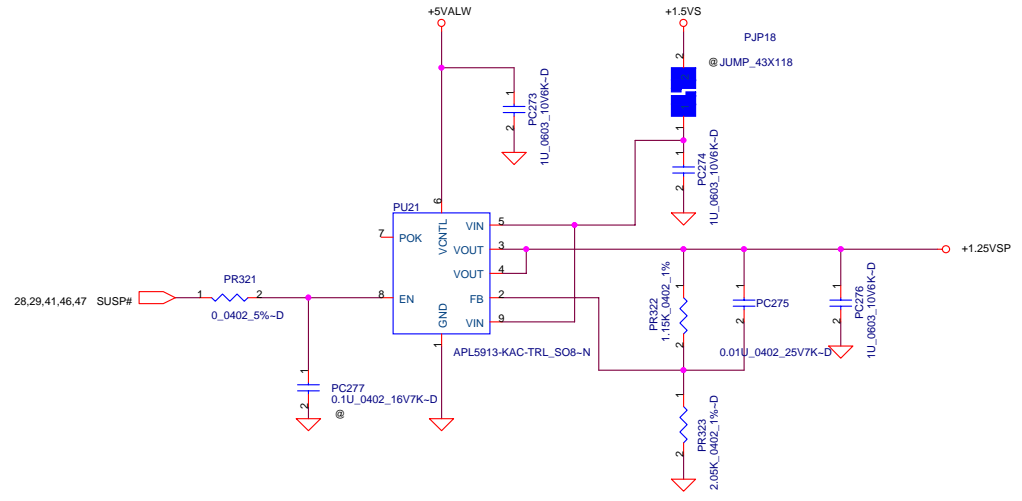
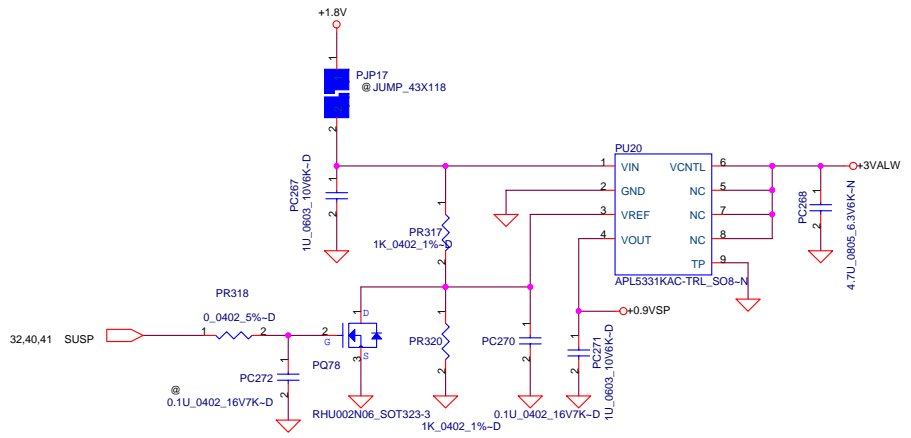
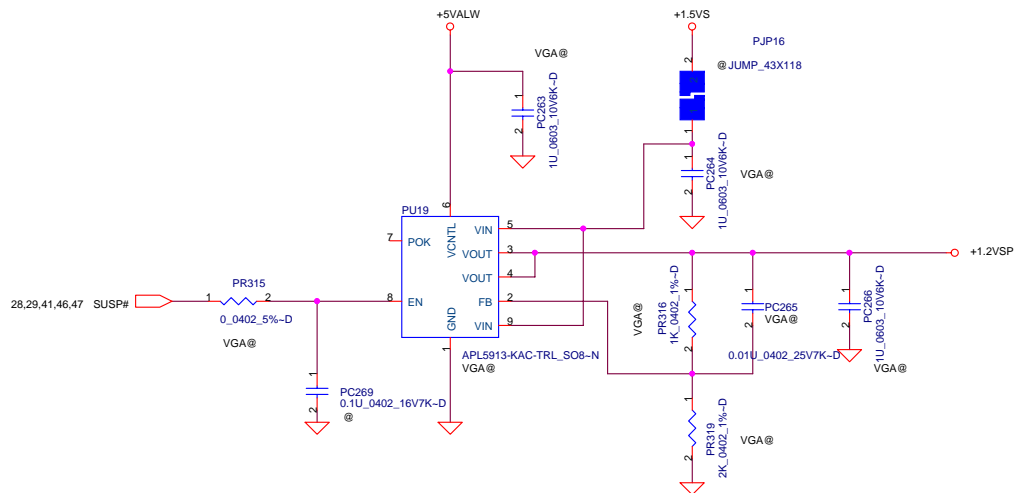
DCR 15m ohm(max)
 1.8VP
 I_{max}=9A
 I_{ocp}=12.31A

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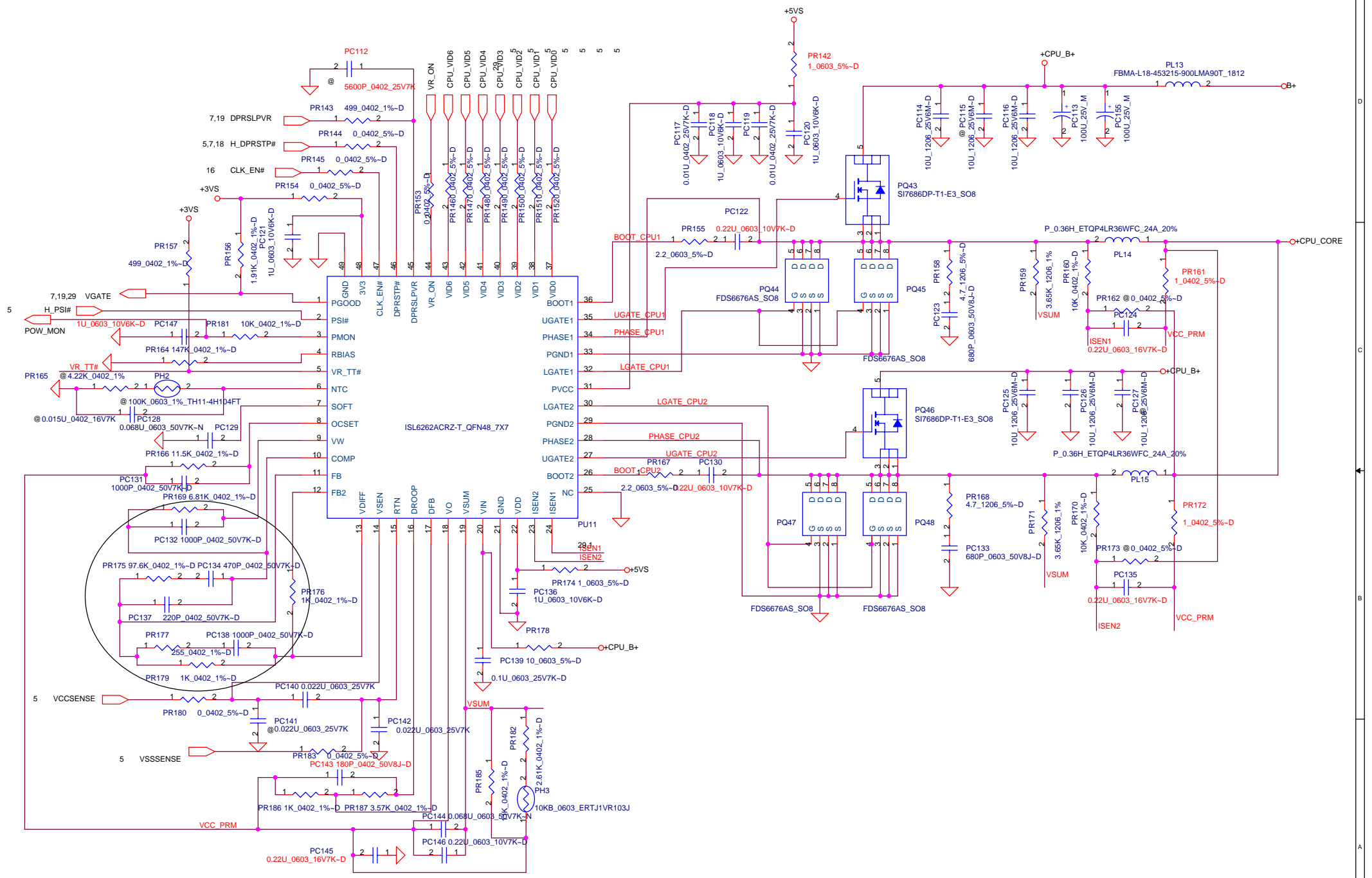
PGOOD1 PGOOD2 串1K電組上@



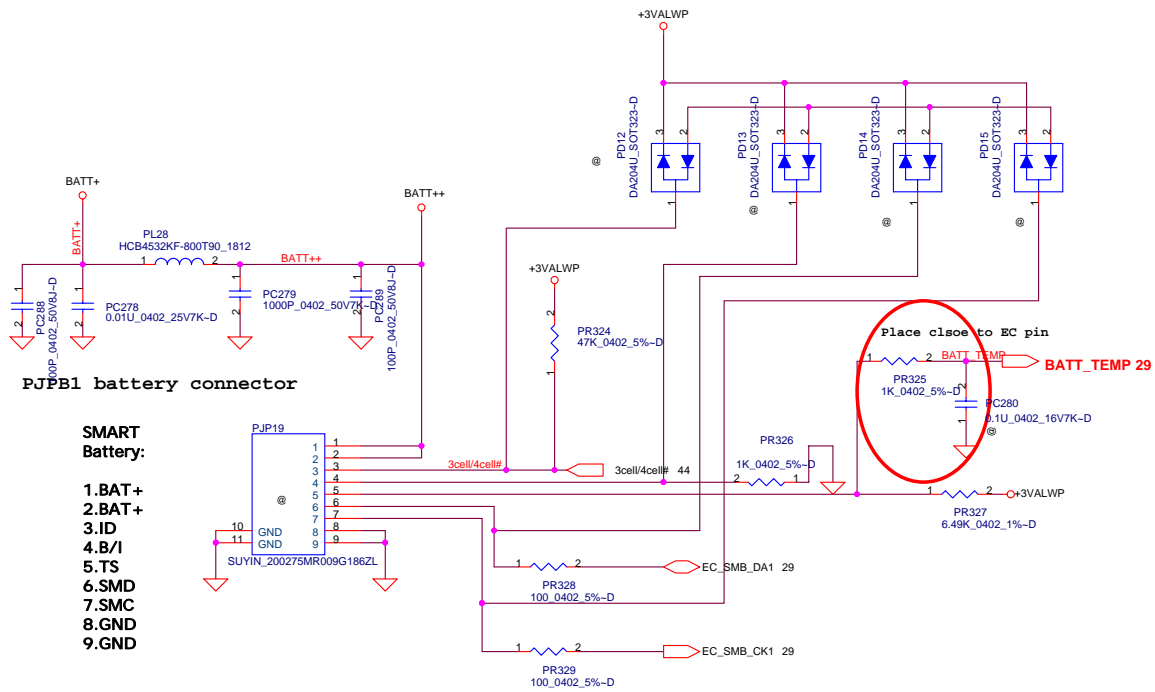
Security Classification	Compal Secret Data		Title	+1.5VP/+VGA
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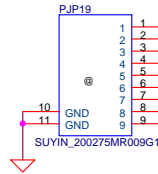
Security Classification		Compal Secret Data		Title +CPU CORE	
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PJPB1 battery connector

SMART Battery:

- 1.BAT+
- 2.BAT+
- 3.ID
- 4.B/I
- 5.TS
- 6.SMD
- 7.SMC
- 8.GND
- 9.GND

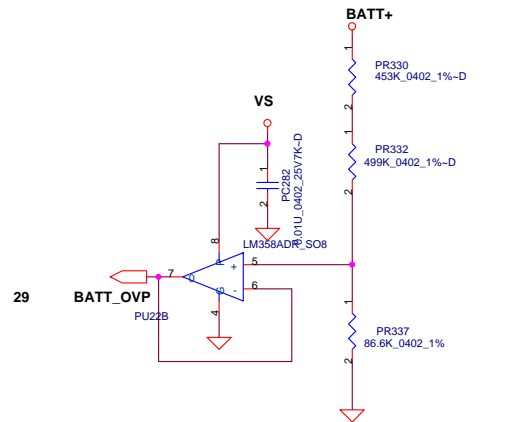


Place close to EC pin
 BATT_TEMP 29

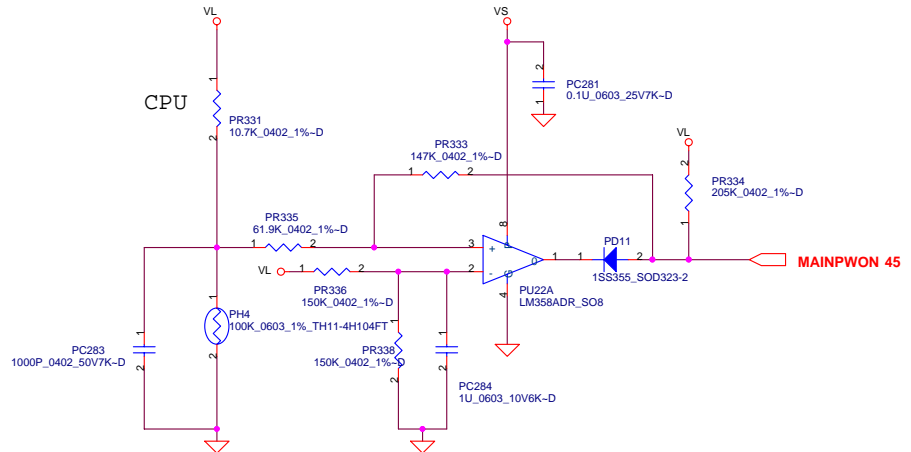
Battery Connect/OTP

CPU

PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 50 +/-3 degree C



LI-3S :13.5V---BATT-OVP=1.5V
 BATT-OVP=0.111*BATT+



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Compal Electronics, Inc.

BATTERY CONN

JAL80

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	board rev update to 0.2	R231 change to 15K & R232 pop	0.2
2	40	P40-02129_Card Reader/1394	07/10/30	compal	CardBus vendor change	CardBus R5C833 change to 02129	0.2
3	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Change pull up resistance	Change EC pin17,18 pull up to 4.7Kohm	0.2
4	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Need pull up	NET MIC_DIAG pull up R to 10Kohm 3VS	0.2
5	13,14	DDR2 SODIMM-I,II Socket	07/10/30	compal	Change Capacitance	Change C84,C189 to SGA00002680 330U	0.2
6	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	EC update rev	EC change to 926C	0.2
7	28	P28-Express card	07/10/30	compal	Express card can't detect	POWER IC(U11) ADD PIN10 CPUSB# PIN9 EXPR_CPUSB#S	0.2
8	32	P32-USB/ BlueTooth/ FP/ Felica	07/10/30	compal	Bluetooth can't detect	BLUETOOTH CONN USB+- change	0.2
9	42	P42-Screws	07/10/30	compal	FIDUCAL no enough	ADD FIDUCAL*4	0.2
10	41	P41-DC/DC Interface	07/10/30	compal	Need pull down	SYSON pull down 10K ohm	0.2
11	41	P41-DC/DC Interface	07/11/12	compal	USB can't detect	SUSP change to 5VALW(Q32)	0.2
12	06	P06-Merom(3/3)-GND/Bypass	07/11/12	compal	Change CPU High Freqeunce Decoupling Capacitance	C195 change to C1150-C1181	0.2
13	41	P41-DC/DC Interface	07/11/13	compal	+1.8VS Discharge error	+1.8VS Discharge circuit Q65 net change to VGA_PWGOD#	0.2
14	41	P41-DC/DC Interface	07/11/16	compal	Delete	Remove SIM card connector	0.2
15	42	P42-Screws	07/11/16	compal	Change Holea size	Change Holea size 2.5 to 2.8, change 3.5 to 3.8	0.2
16	31	P31-PWR_OK/ BTN/ KB / TouchPad	07/11/21	compal	Change Touch PAD/B connector	Touch PAD/B connector change net	0.2
17	15	P15-CRT Conn.& LCD Conn.	07/11/21	compal	Add LCD control pin	Add LCD control pin LCD_CBL_DET# & LCD_TST & LCD_VCC_TEST_EN	0.2
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				LA-423IP	0.1
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	+3VALWP/+5VALWP	07/11/19	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD P079 to turn off 5VALWP wehn shut down the system in the DC-mode	
2	44	Charge	07/12/26	COMPAL	change charge voltage can to adjust	Change PR53 from 15K to 4.3K	
3	49	CPU_CORE	07/12/26	COMPAL	Increase Resistor 0ohm on CPU_CORE high side gate for EMI request	ADD PR163 PR184	
4	45	+3VALWP/+5VALWP	07/12/26	COMPAL	The schematic location is wrong	DEL PL19	
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				LA-3682P	0.1
Date:				Thursday, January 10, 2008	Sheet 52 of 9