Beyonce UMA Schematics Document

uFCPGA Mobile Merom

Intel Crestline-GM + ICH8M

2008-02-21

REV : -2 (DELL:A00)

DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA		
Size: A3	Document Number: COVER PAGE	Rev: -3
Date: Friday, February 22, 2008	Sheet 1 of 46	

Beyonce UMA Block Diagram

Project code:91.4C301.001
PCB P/N :06253
REVISION :-1

Thermal Sensor EMC4001 28 — SMBus

Clock Generator CY28547LFXC 6

Intel Mobile CPU Merom 4M FSB:667/ 800 Mhz 7,8

HOST BUS — FSB 667/800MHz

200-PIN DDR2 SODIMM

CRT 18 — RGB
LCD 19 — LVDS
HDMI 18 — HDMI

Remove in DB5

SIL 1392 17 — SDVO

Crestline-GM
AGTL+ CPU I/F
DDR Memory I/F
EXTERNAL GRAHPICS
9,10,11,12,13,14

DDRII 533/667MHz — UNBUFFERED DDR2 SODIMM Socket 15
DDRII 533/667MHz — UNBUFFERED DDR2 SODIMM Socket 16

Ricoh R5C833 8 in 1 card reader 1394 28
1394 — 1394 CONN 29
7 in1 — 8 in1 CONN 29

SPDIF
AZALIA

DMI x4
C-LINK0 PCI BUS
PCI Express (4)

Power Switch 26
Express Card Slot 54mm 26
PCIE#4

SATA HDD 26 — SATA
ODD Bay 26 — PATA IDE

Intel ICH8-M Enhanced
USB 2.0/1.1 ports (10)
PCI Express ports (6)
High Definition Audio
ATA 66/ 100
SATA (3)
LPC I/F
SPI
ACPI 1.1
PCI/PCI BRIDGE
20,21,22,23,24

USB2.0 (7)
USB#6
USB#7
USB#0
USB#1
USB#8
PCIE#2
PCIE#6
USB#5
USB#4
PCIE#1

Buletooth 2.1 29
USB*1 left side 38
USB*1 Right side 38
Mini-Card WWAN 27
SIM CONN 27
Mini-Card 802.11a/g/n 27
LAN BCM5906 10/100 NIC 25
RJ45 CONN 25
Camera 19

Remove in DB5

LINE OUT / HP
Headphone AMP. MAX4401A 31

Digital MIC 19
MIC IN
Azalia CODEC STAC 9228 30 — AZALIA

LINE OUT / HP
INT. SPKR *2 31
Headphone AMP. MAX9789A 31

BIOS SPI FLASH 16Mb 33 — SPI
SPI
LPC

EC SMSC MEC5025 32
BC
SIO Expander SMSC ECE5021 33
CIR 38

BC
PS/2

KBC SMSC ECE1077 34
Int. KB 34
Touch Pad 34
Biometric 34

Touch Pad Module

LCD 19
Digital MIC 19
Camera 19
LCD Module 23

System DC/DC TPS51120 41	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW +5V_SUS +3.3V_SUS +3.3V_RTC_LDO

System DC/DC TPS51124 42	
+PWR_SRC	+1.05V_VCCP +1.5V_RUN

DDR2 DC/DC TPS51117 43	
+PWR_SRC	+1.8V_SUS

LDO TPS51100 43	
+1.8V_SUS	+0.9V_DDR_VTT V_DDR_MCH_REF

LDO SC339SKTRT 44	
+PWR_SRC	+1.25V_RUN

Battery Charger MAX8731 38	
INPUTS	OUTPUTS
+PWR_SRC	+VCHGR

CPU DC/DC ISL6260C 39,40	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

PCB LAYER

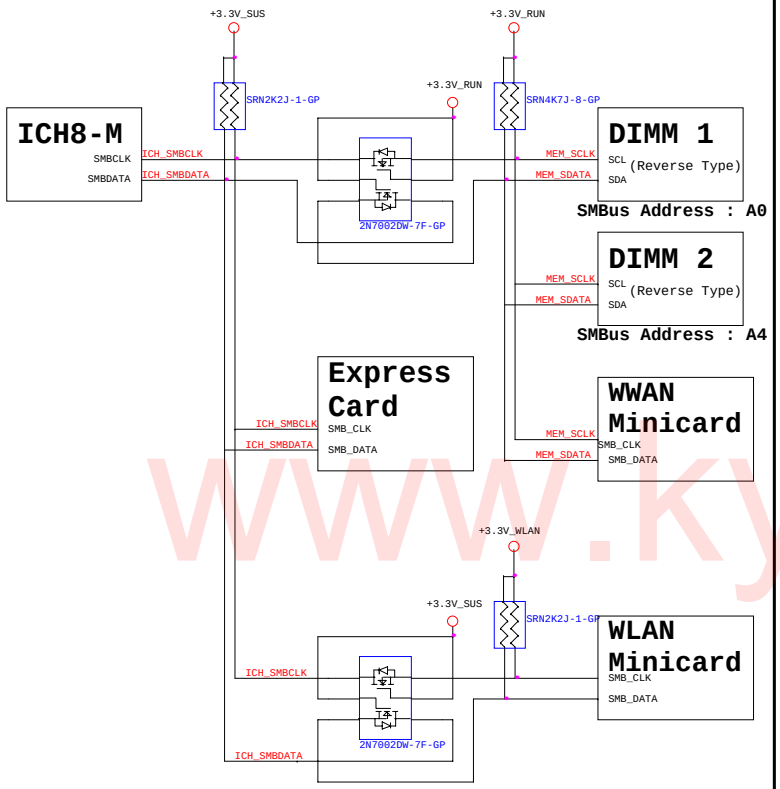
L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:BOT

DB5

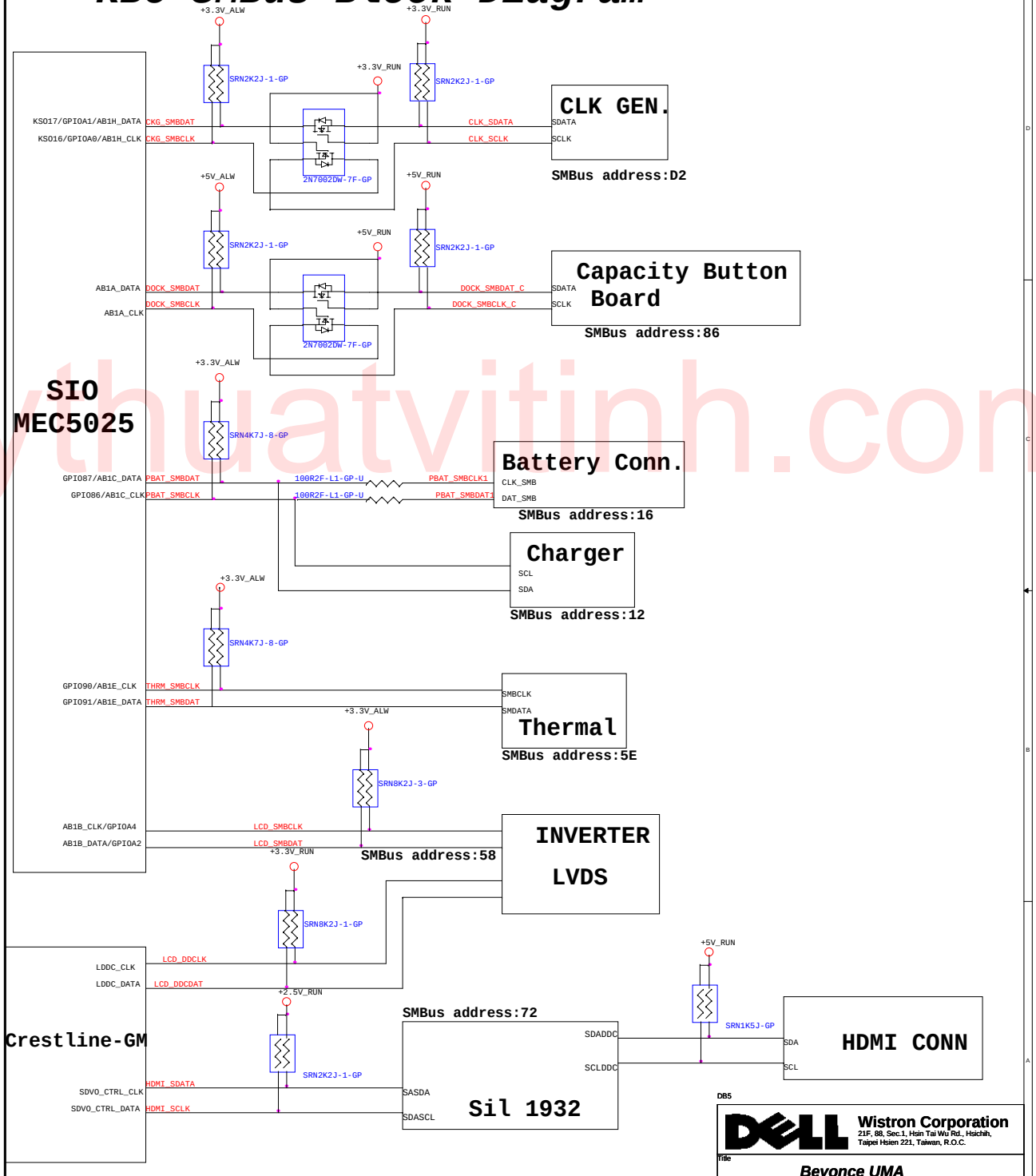
Wistron Corporation
88 Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

Size: C — Title: UMA — Doc: — Rev: -1
Date: 2007.12.04 19:32:15
Sheet 2 of 46

ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA

Size	Document Number	Rev
C	SMBus Block Diagram	-3

Date: Friday, February 22, 2008 Sheet 3 of 46

CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 10

Bit5 S1	Bit4 S0	Spread Spectrum S[1:0]
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

BYTE 15
IO_VOUT[2,1,0]

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL CRESTLINE STRAP PIN

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	10/100 LOM

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

ICH USB TABLE

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD_tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule High=No Reboot

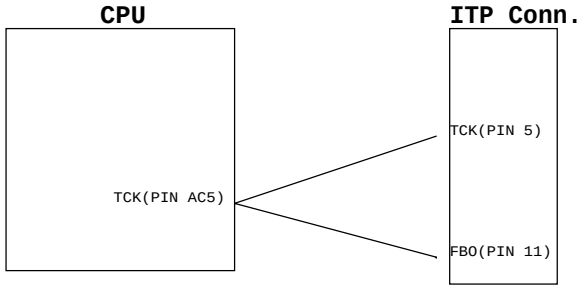
8.2K PULL HIGH

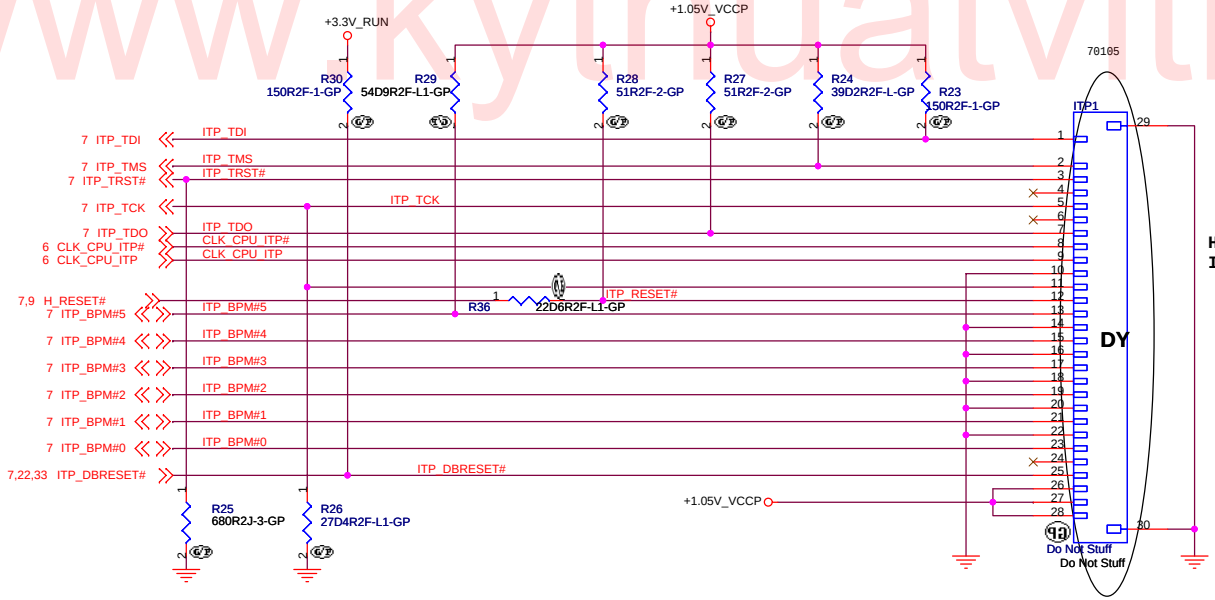
INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA
Size: A3 | Document Number: Table of Content | Rev: -3
Date: Friday, February 22, 2008 | Sheet 4 of 46





H_CPURST# use pull-up Resistor close ITP connector 500 mil (max)

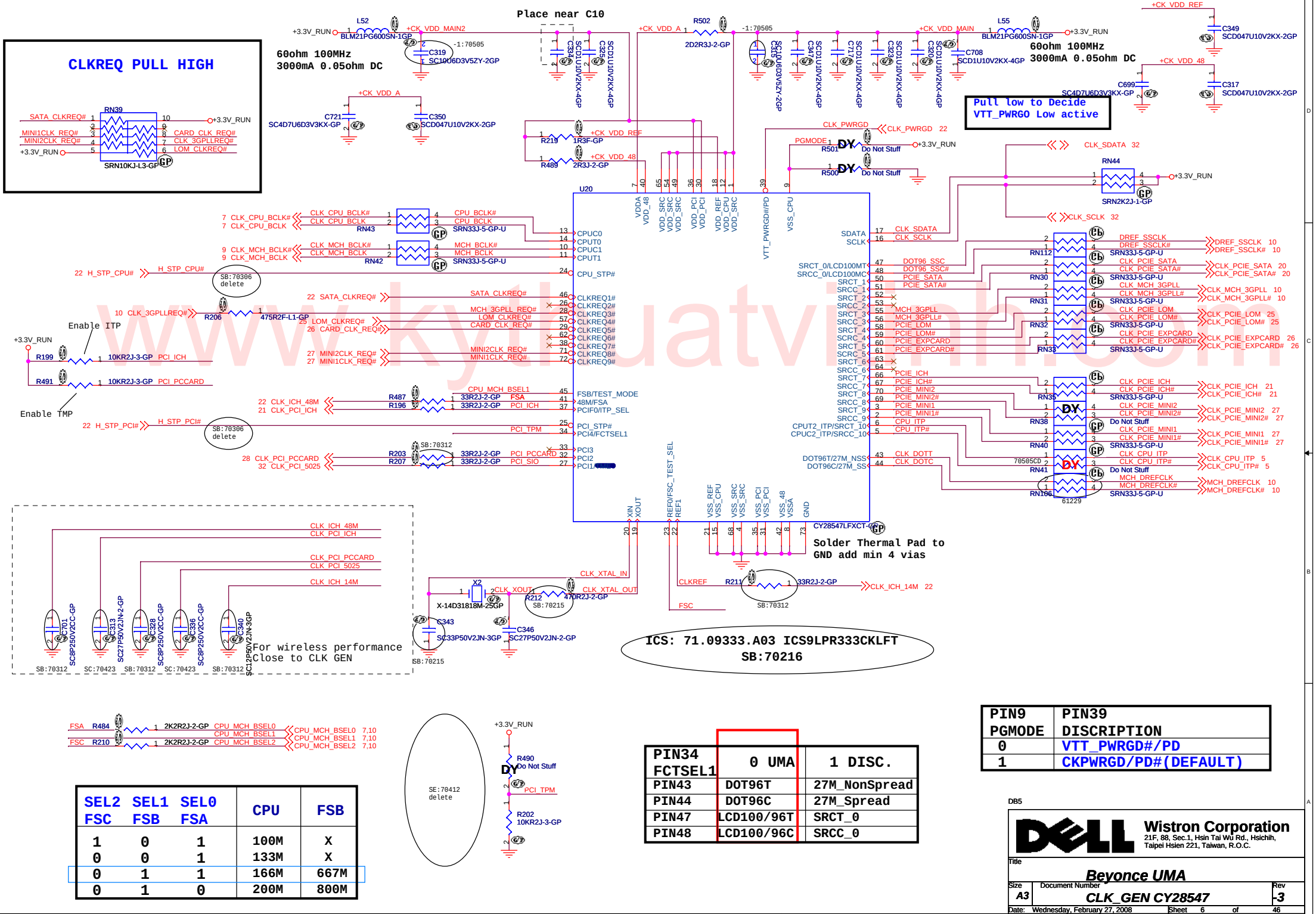
+1.05VRUN use Decoupling Capacitor close ITP connector 100 mil (max)

ITP Debug Conn.

DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Beyonce UMA	
Size: A3	Document Number: ITP Debug	Rev: -3
Date: Wednesday, February 27, 2008	Sheet 5 of 46	



SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

PIN9 PGMODE	PIN39 DISCRIPTION
0	VTT_PWRGD#/PD
1	CKPWRGD/PD#(DEFAULT)

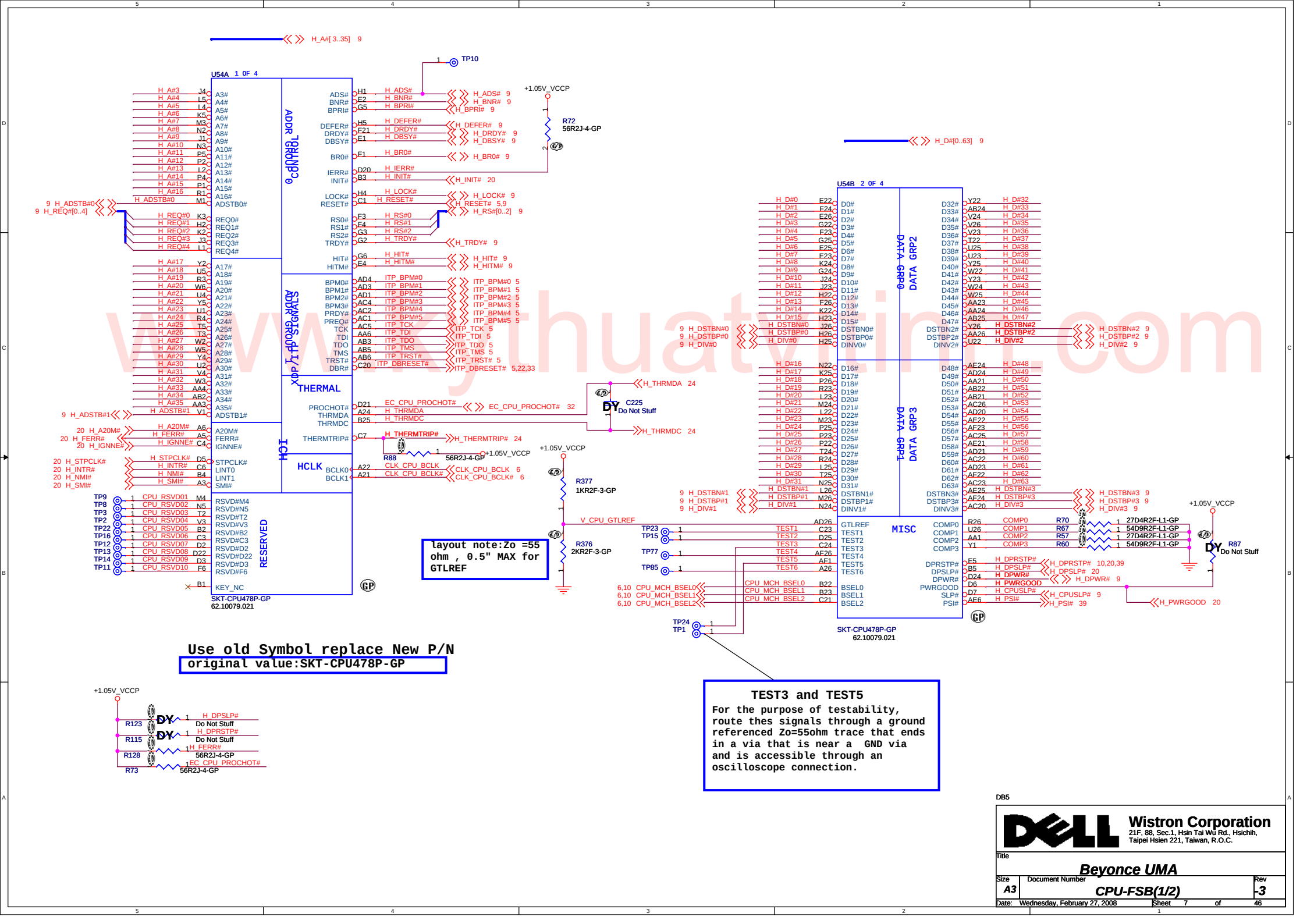
DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA

Size: A3 | Document Number: CLK_GEN CY28547 | Rev: -3

Date: Wednesday, February 27, 2008 | Sheet 6 of 46



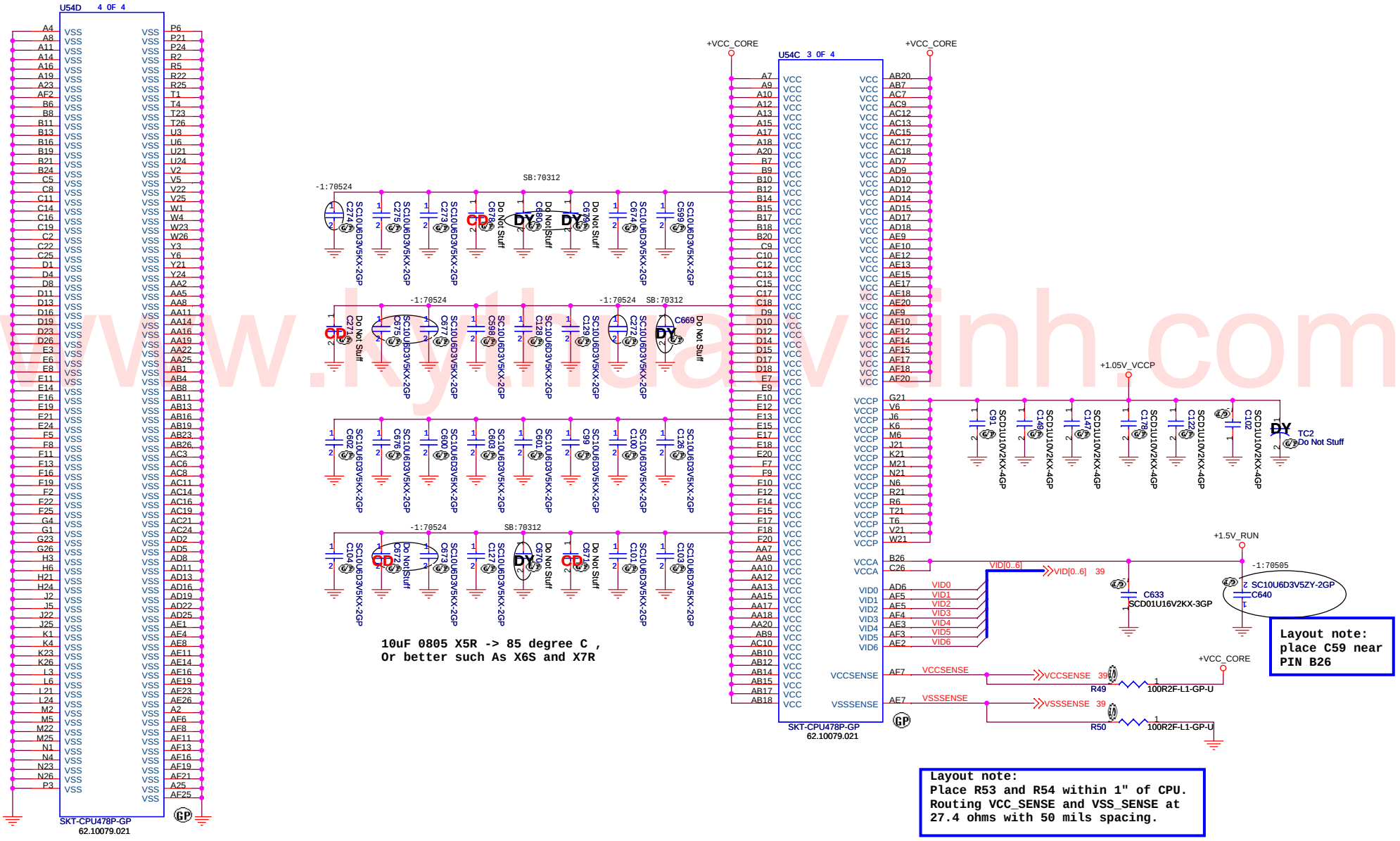
DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA

Size	Document Number	Rev
A3	CPU-FSB(1/2)	-3

Date: Wednesday, February 27, 2008 Sheet 7 of 46



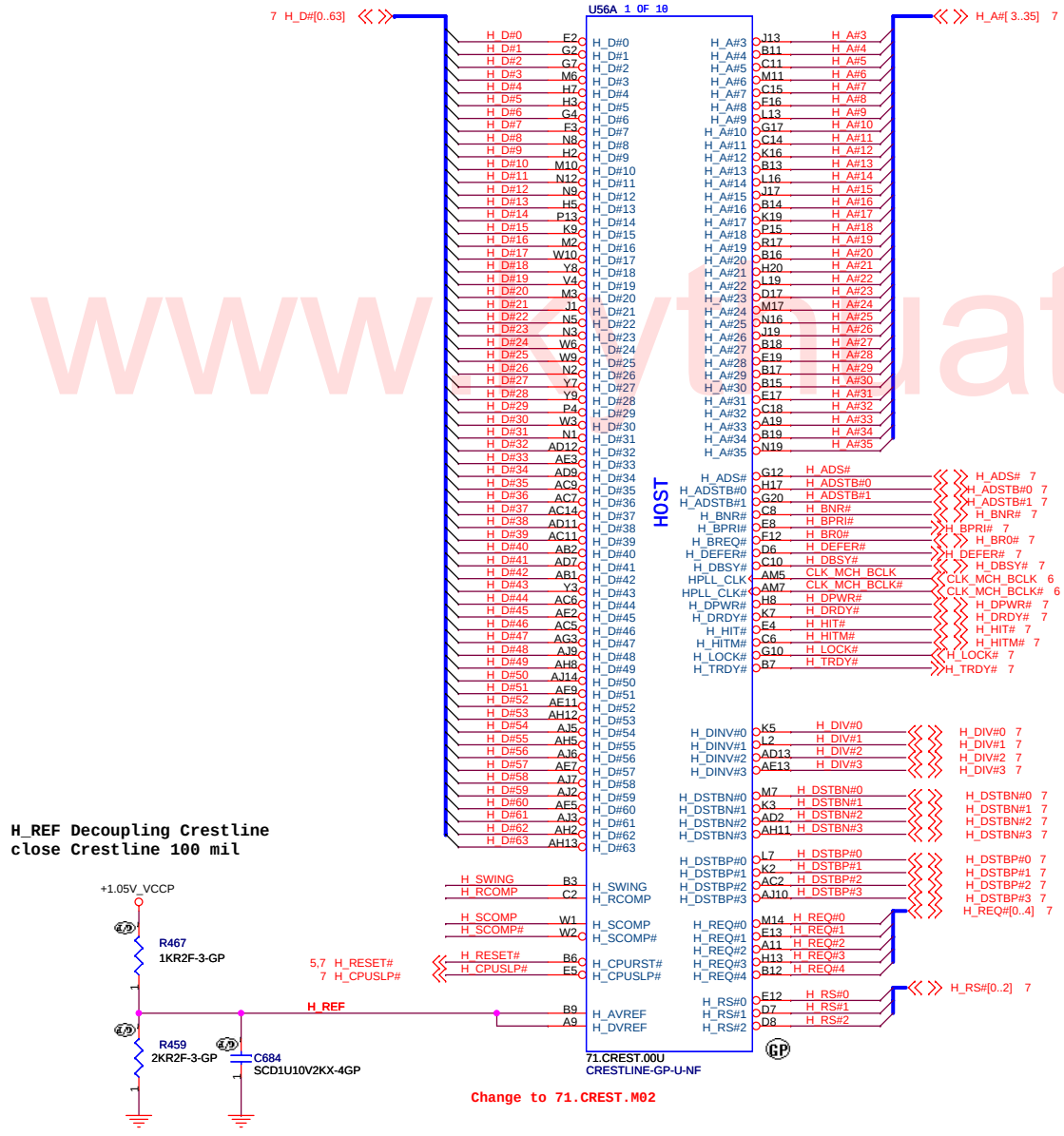
DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA

Size	Document Number	Rev
A3	06.CPU-POWER (2/2)	-3

Date: Wednesday, February 27, 2008 Sheet 8 of 46



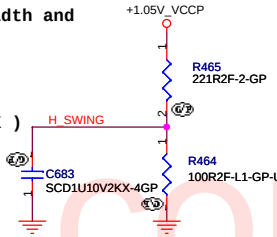
H_REF Decoupling Crestline close Crestline 100 mil

Change to 71.CREST.M02

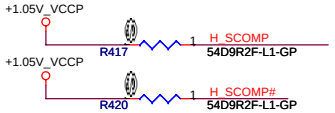
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close Caliistoga 500 mil (MAX)

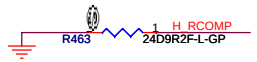
From Schematic Design Checklit v.1201
221 1% pull high 100
1% pull low



H_SCOMP and H_SCOMP# Resistors and Capacitors close Caliistoga 500 mil (MAX)
Zo=55ohms



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA

Size	Document Number	Rev
A3	GMCH-FSB LIBC (1/6)	-3

Date: Wednesday, February 27, 2008 Sheet 9 of 46

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *
	CFG[2..0] FSB Select
LHL	FSB 800
LHH	FSB 667
Other	Reserved

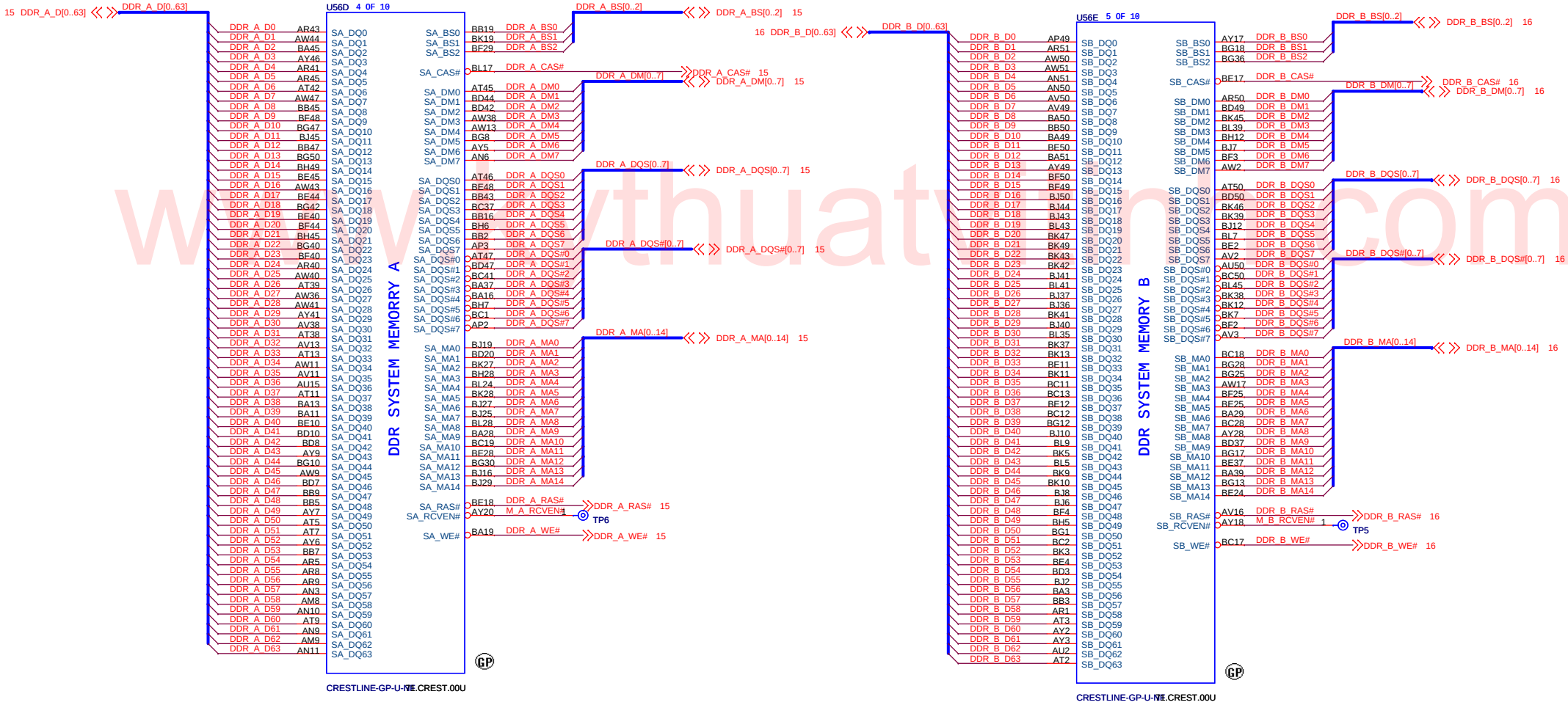
Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.

Layout Note:
MCH_CLVREF ~= 0.350V
Width/Spacing = 12/12

CRESTLINE-GP-U-NF 71.CREST.00U

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA
Size: A3 | Document Number: GMCH-DMI/DDR (2/6) | Rev: -3
Date: Wednesday, February 27, 2008 | Sheet 10 of 46



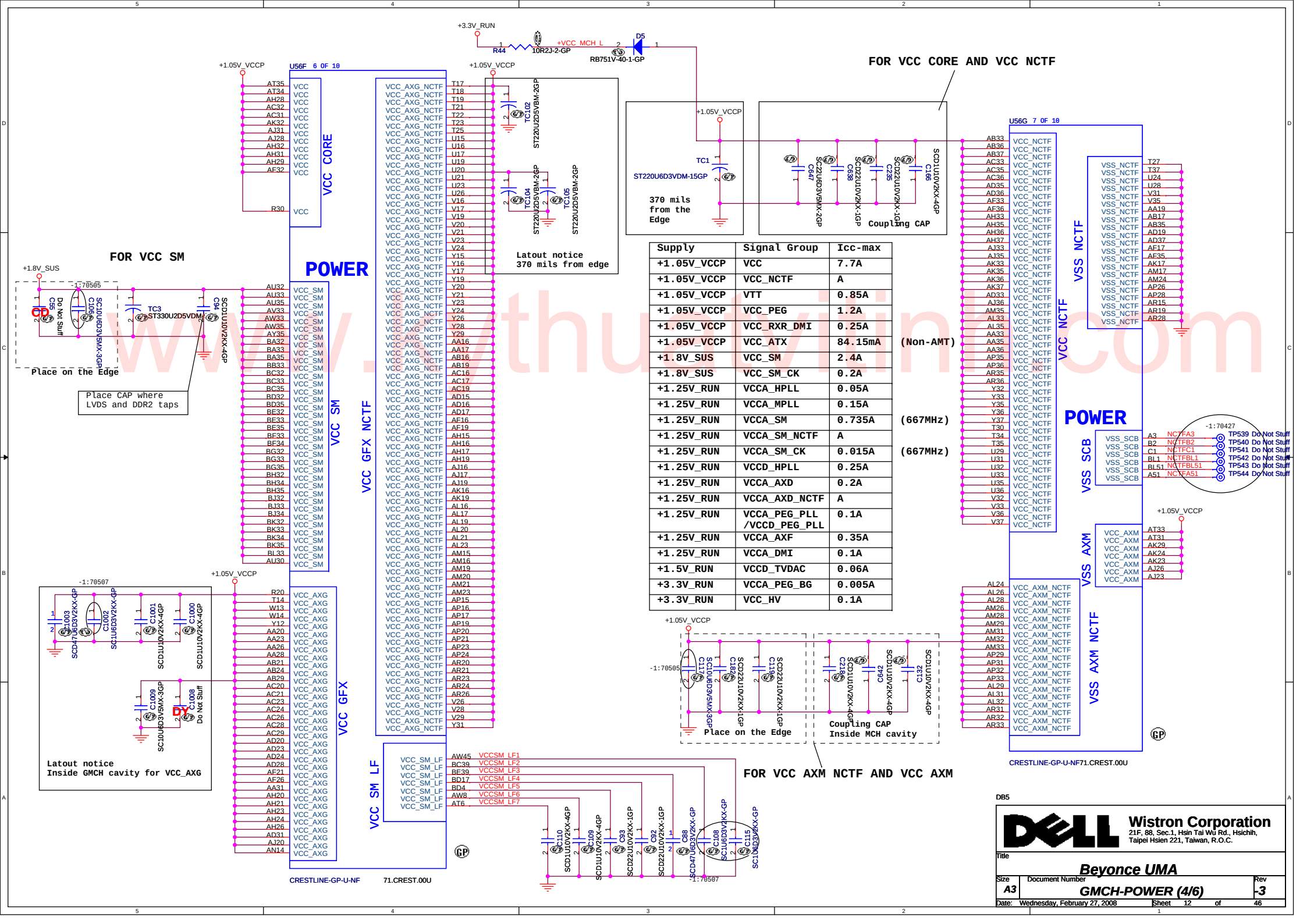
DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA

Size	Document Number	Rev
A3	GMCH-DDR (3/6)	-3

Date: Wednesday, February 27, 2008 Sheet 11 of 46



Supply	Signal Group	Icc-max	
+1.05V_VCCP	VCC	7.7A	
+1.05V_VCCP	VCC_NCTF	A	
+1.05V_VCCP	VTT	0.85A	
+1.05V_VCCP	VCC_PEG	1.2A	
+1.05V_VCCP	VCC_RXR_DMI	0.25A	
+1.05V_VCCP	VCC_ATX	84.15mA	(Non-AMT)
+1.8V_SUS	VCC_SM	2.4A	
+1.8V_SUS	VCC_SM_CK	0.2A	
+1.25V_RUN	VCCA_HPLL	0.05A	
+1.25V_RUN	VCCA_MPLL	0.15A	
+1.25V_RUN	VCCA_SM	0.735A	(667MHz)
+1.25V_RUN	VCCA_SM_NCTF	A	
+1.25V_RUN	VCCA_SM_CK	0.015A	(667MHz)
+1.25V_RUN	VCCD_HPLL	0.25A	
+1.25V_RUN	VCCA_AXD	0.2A	
+1.25V_RUN	VCCA_AXD_NCTF	A	
+1.25V_RUN	VCCA_PEG_PLL /VCCD_PEG_PLL	0.1A	
+1.25V_RUN	VCCA_AXF	0.35A	
+1.25V_RUN	VCCA_DMI	0.1A	
+1.5V_RUN	VCCD_TVDAC	0.06A	
+3.3V_RUN	VCCA_PEG_BG	0.005A	
+3.3V_RUN	VCC_HV	0.1A	

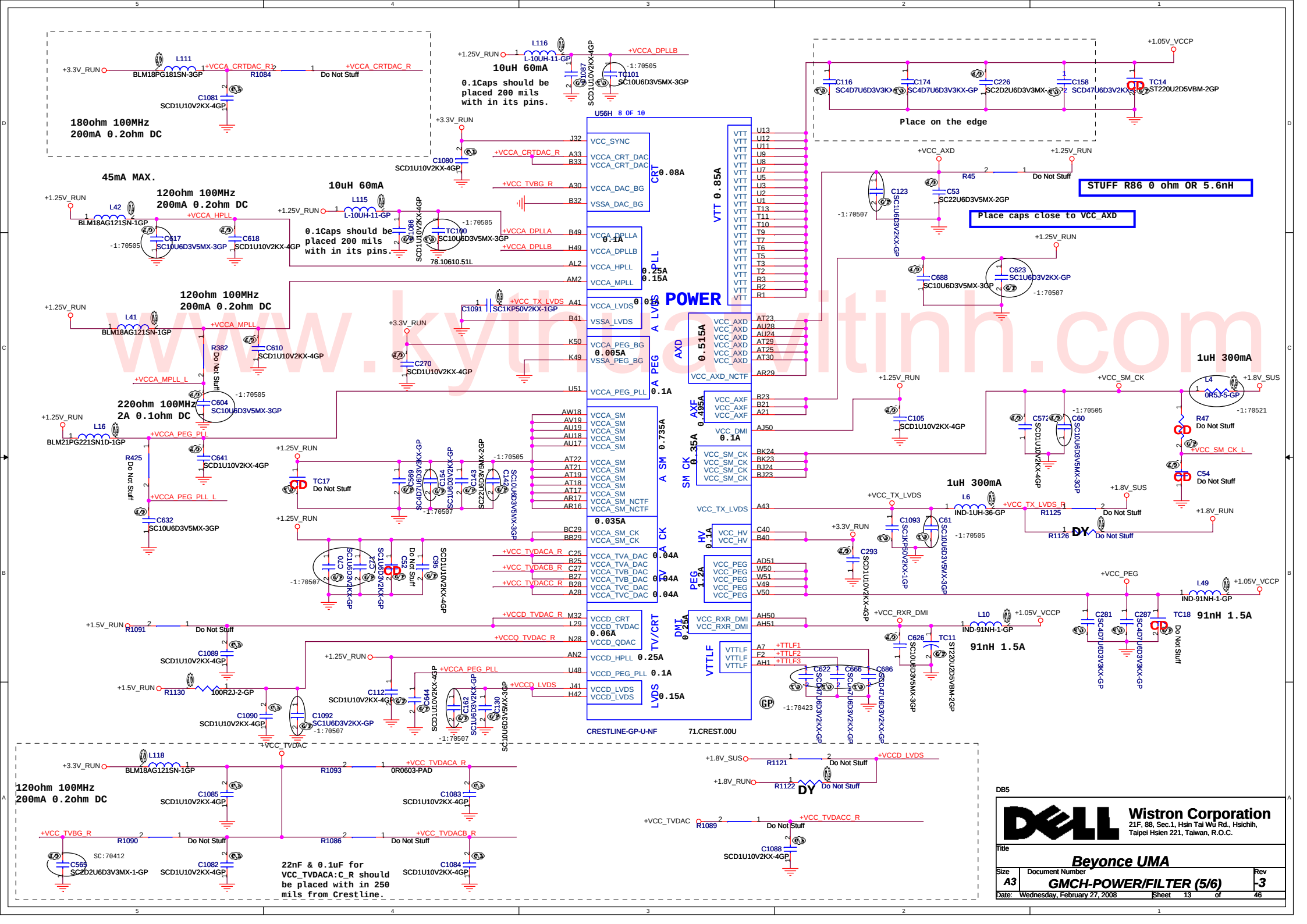
DB5

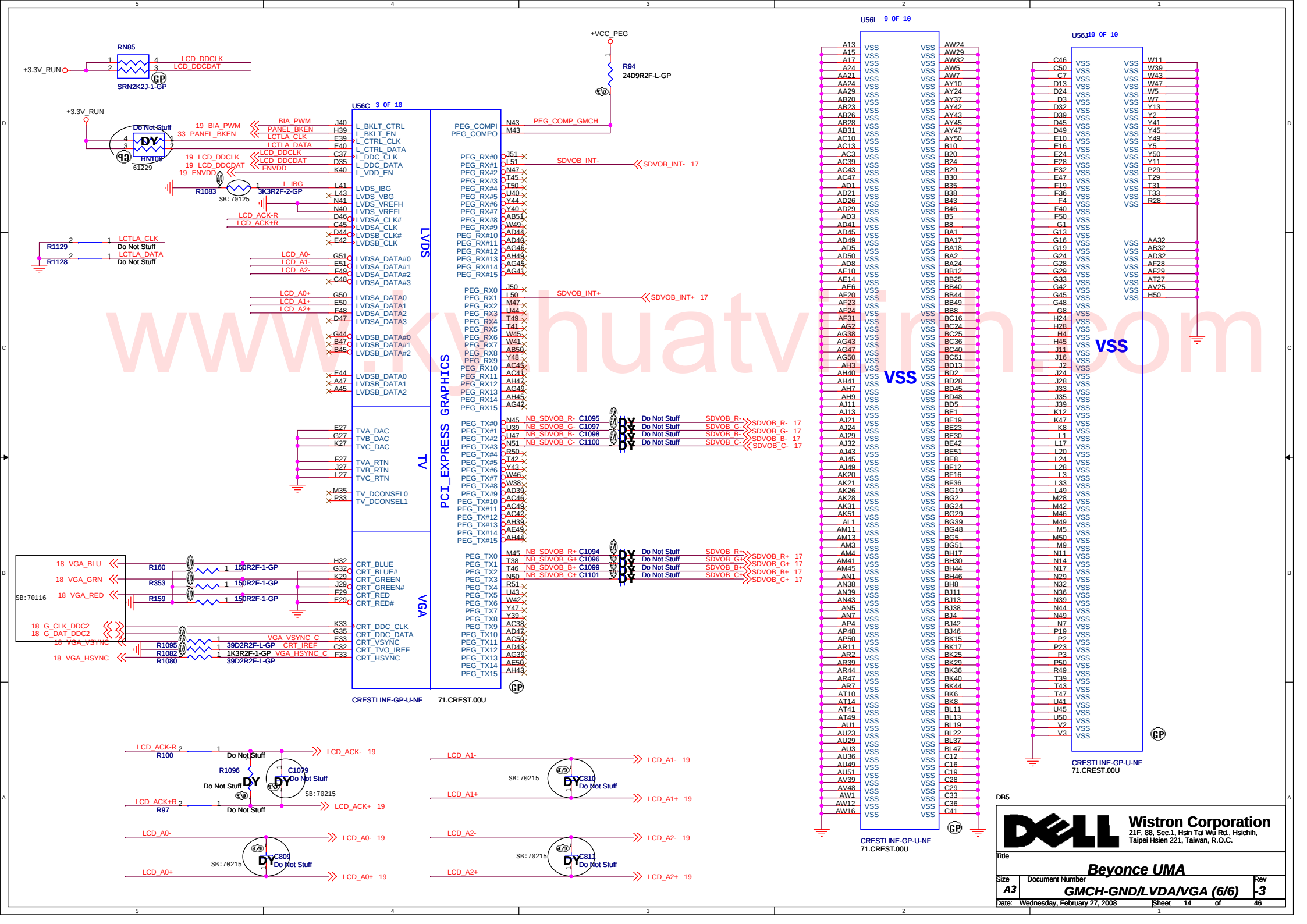
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA

Size: A3 | Document Number: GMCH-POWER (4/6) | Rev: -3

Date: Wednesday, February 27, 2008 | Sheet 12 of 46


POWER
U56H 8 OF 10
CRESTLINE-GP-U-NF
71.CREST.00U
180ohm 100MHz
200mA 0.2ohm DC
45mA MAX.
120ohm 100MHz
200mA 0.2ohm DC
10uH 60mA
0.1Caps should be placed 200 mils with in its pins.
220ohm 100MHz
2A 0.1ohm DC
1uH 300mA
91nH 1.5A
Place on the edge
Place caps close to VCC_AXD
STUFF R86 0 ohm OR 5.6nH
22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Beyonce UMA
GMCH-POWER/FILTER (5/6)
Size A3
Rev -3
Date: Wednesday, February 27, 2008
Sheet 13 of 46


RN85
SRN2K2J-1-GP
+3.3V_RUN
LCD_DDCLK
LCD_DDCDAT
+VCC_PEG
R94
24D9R2F-L-GP
U56C 3 OF 10
L_BKLT_CTRL
L_BKLT_EN
L_CTRL_CLK
L_CTRL_DATA
L_DDC_CLK
L_DDC_DATA
L_VDD_EN
LVDS_IBG
LVDS_VBG
LVDS_VREFH
LVDS_VREFL
LVDSA_CLK#
LVDSA_CLK
LVDSB_CLK#
LVDSB_CLK
LVDSA_DATA#0
LVDSA_DATA#1
LVDSA_DATA#2
LVDSA_DATA#3
LVDSA_DATA0
LVDSA_DATA1
LVDSA_DATA2
LVDSA_DATA3
LVDSB_DATA#0
LVDSB_DATA#1
LVDSB_DATA#2
LVDSB_DATA0
LVDSB_DATA1
LVDSB_DATA2
LVDS
TVA_DAC
TVB_DAC
TVC_DAC
TVA_RTN
TVB_RTN
TVC_RTN
TV_DCONSEL0
TV_DCONSEL1
TV
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_VSYNC
CRT_TVO_IREF
CRT_HSYNC
VGA
PCI_EXPRESS GRAPHICS
PEG_COMPI
PEG_COMPO
PEG_COMP_GMCH
PEG_RX#0
PEG_RX#1
PEG_RX#2
PEG_RX#3
PEG_RX#4
PEG_RX#5
PEG_RX#6
PEG_RX#7
PEG_RX#8
PEG_RX#9
PEG_RX#10
PEG_RX#11
PEG_RX#12
PEG_RX#13
PEG_RX#14
PEG_RX#15
PEG_RX0
PEG_RX1
PEG_RX2
PEG_RX3
PEG_RX4
PEG_RX5
PEG_RX6
PEG_RX7
PEG_RX8
PEG_RX9
PEG_RX10
PEG_RX11
PEG_RX12
PEG_RX13
PEG_RX14
PEG_RX15
PEG_TX#0
PEG_TX#1
PEG_TX#2
PEG_TX#3
PEG_TX#4
PEG_TX#5
PEG_TX#6
PEG_TX#7
PEG_TX#8
PEG_TX#9
PEG_TX#10
PEG_TX#11
PEG_TX#12
PEG_TX#13
PEG_TX#14
PEG_TX#15
PEG_TX0
PEG_TX1
PEG_TX2
PEG_TX3
PEG_TX4
PEG_TX5
PEG_TX6
PEG_TX7
PEG_TX8
PEG_TX9
PEG_TX10
PEG_TX11
PEG_TX12
PEG_TX13
PEG_TX14
PEG_TX15
SDVOB_INT-
SDVOB_INT+
NB_SDVOB_R- C1095
NB_SDVOB_G- C1097
NB_SDVOB_B- C1098
NB_SDVOB_C- C1100
NB_SDVOB_R+ C1094
NB_SDVOB_G+ C1096
NB_SDVOB_B+ C1099
NB_SDVOB_C+ C1101
Do Not Stuff
SDVOB_R-
SDVOB_G-
SDVOB_B-
SDVOB_C-
SDVOB_R+
SDVOB_G+
SDVOB_B+
SDVOB_C+
CRESTLINE-GP-U-NF
71.CREST.00U
U56I 9 OF 10
U56J 10 OF 10
VSS
CRESTLINE-GP-U-NF
71.CREST.00U
18 VGA_BLU
18 VGA_GRN
18 VGA_RED
18 G_CLK_DDC2
18 G_DAT_DDC2
18 VGA_VSYNC
18 VGA_HSYNC
R160
R353
R159
R1095
R1082
R1080
150R2F-1-GP
39D2R2F-L-GP
1K3R2F-1-GP
CRT_IREF
VGA_VSYNC_C
VGA_HSYNC_C
SB:70116
SB:70215
R1083
3K3R2F-2-GP
L_IBG
R1129
R1128
LCTLA_CLK
LCTLA_DATA
R1096
C1079
R100
R97
C809
C810
C811
LCD_ACK-R
LCD_ACK+R
LCD_ACK-
LCD_ACK+
LCD_A0-
LCD_A0+
LCD_A1-
LCD_A1+
LCD_A2-
LCD_A2+
19 BIA_PWM
33 PANEL_BKEN
19 LCD_DDCLK
19 LCD_DDCDAT
19 ENVDD
SDVOB_INT- 17
SDVOB_INT+ 17
SDVOB_R- 17
SDVOB_G- 17
SDVOB_B- 17
SDVOB_C- 17
SDVOB_R+ 17
SDVOB_G+ 17
SDVOB_B+ 17
SDVOB_C+ 17
DB5
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Beyonce UMA
Size A3
Document Number
GMCH-GND/LVDA/VGA (6/6)
Rev -3
Date: Wednesday, February 27, 2008
Sheet 14 of 46

REVERSE TYPE

High 5.2 mm

DM2

DDR2-200P-11-GP-U

62.10017.891

+1.8V_SUS

C503 SCD1U10V2KX-4GP
C30 SCD1U10V2KX-4GP
C29 SCD1U10V2KX-4GP
C20 SCD1U10V2KX-4GP
C499 Do Not Stuff
C502 Do Not Stuff
C506 SC2D2U6D3V3MX-1-GP
C500 SC2D2U6D3V3MX-1-GP
C14 SC2D2U6D3V3MX-1-GP

Please close to the DIMM Slot

071004 modify del TC6

+3.3V_RUN

C505 SCD1U10V2KX-4GP

R1133 Do Not Stuff
R1140 Do Not Stuff

+0.9V_DDR_VTT

C39 SCD1U10V2KX-4GP
C34 SCD1U10V2KX-4GP
C537 Do Not Stuff
C538 SCD1U10V2KX-4GP
C40 SCD1U10V2KX-4GP
C35 SCD1U10V2KX-4GP
C536 SCD1U10V2KX-4GP
C539 SCD1U10V2KX-4GP
C33 Do Not Stuff

Please use One Capacitor close to every Two pull-up Resistors

V_DDR_MCH_REF

C25 SC2D2U6D3V3MX-1-GP
C23 SCD1U10V2KX-4GP

R21 56R2J-4-GP

RN16 SRN56J-4-GP
RN18 SRN56J-4-GP
RN62 SRN56J-4-GP
RN61 SRN56J-4-GP
RN20 SRN56J-4-GP
RN63 SRN56J-4-GP

RN60 SRN56J-4-GP
RN21 SRN56J-4-GP
RN19 SRN56J-4-GP
RN58 SRN56J-4-GP
RN59 SRN56J-4-GP
RN17 SRN56J-4-GP
RN64 SRN56J-4-GP

M_CKE[1:0] and M_CS[1:0]# pull-up Resistors close DIMM Slot 1300 mil (MAX)

Others pull-up Resistors close DIMM Slot 750 mil (MAX)

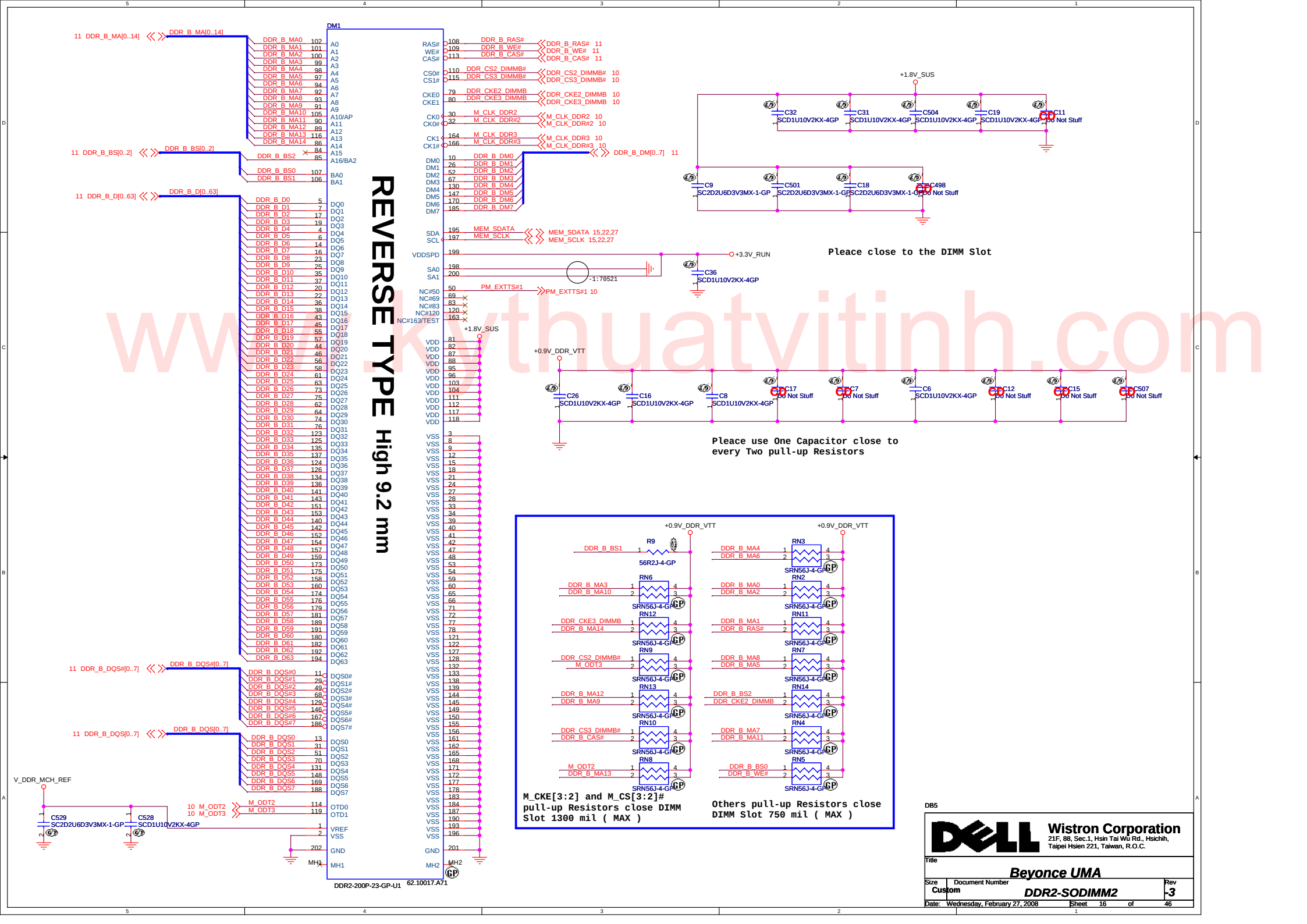
DB5

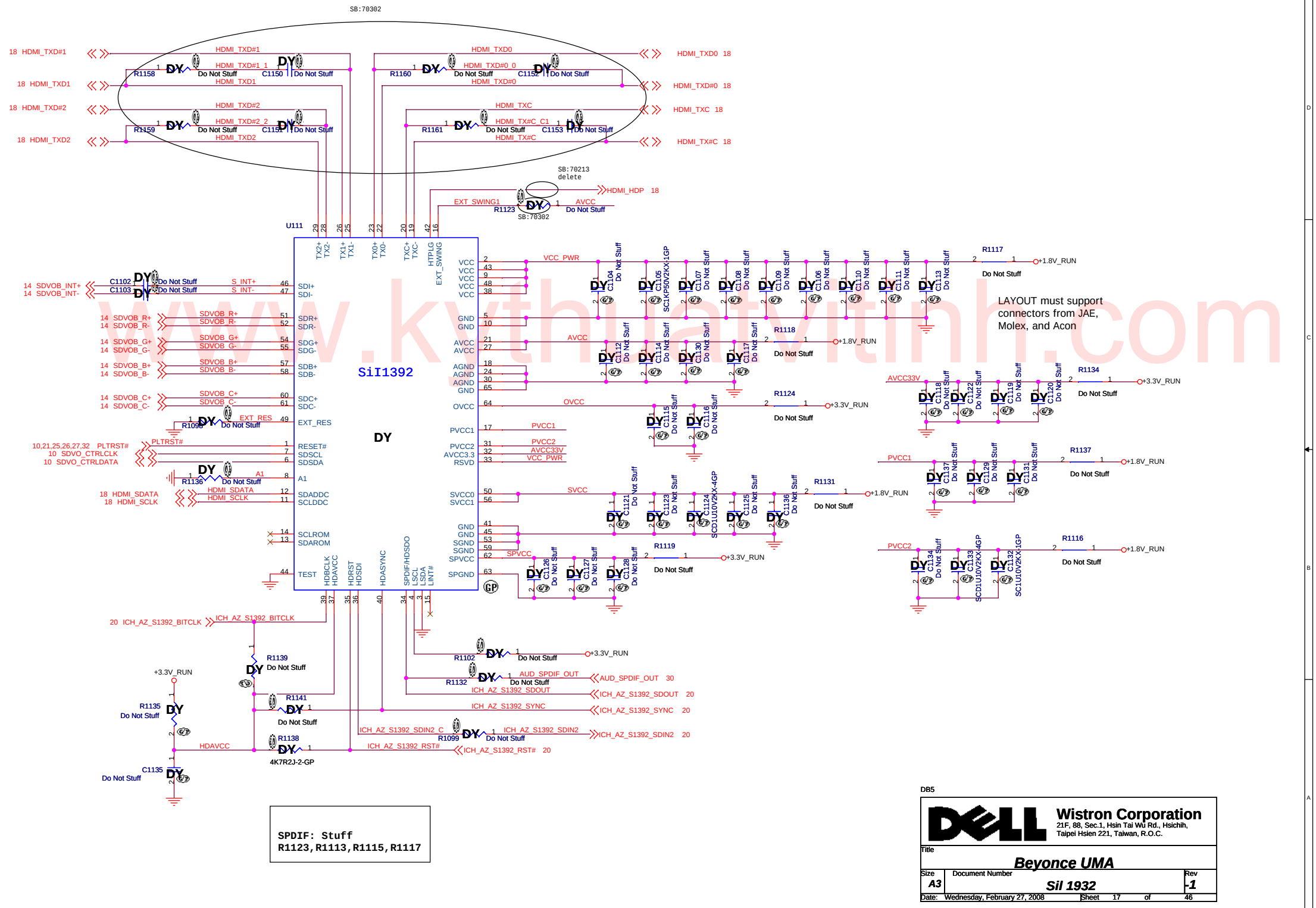
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

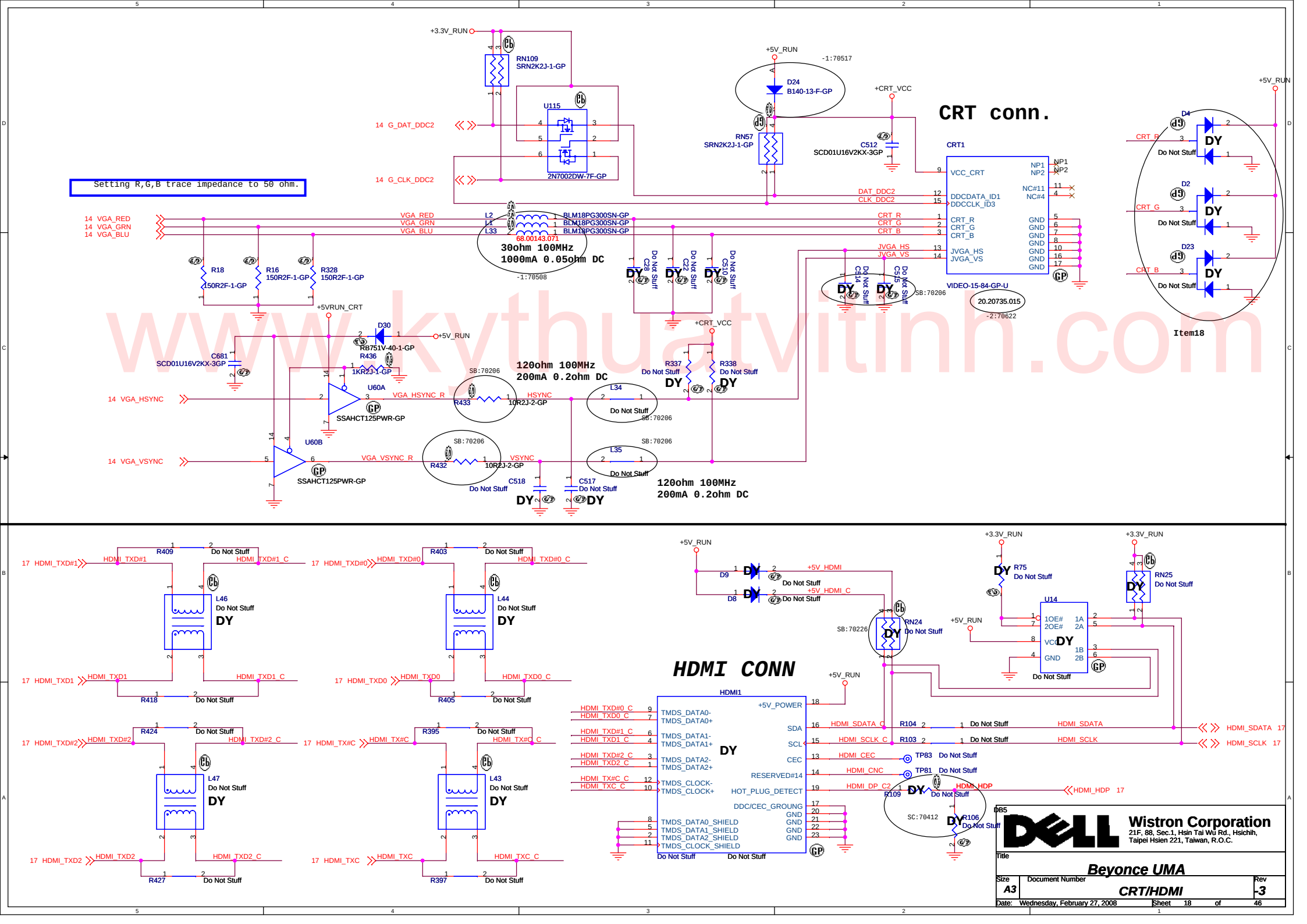
Title: Beyonce UMA

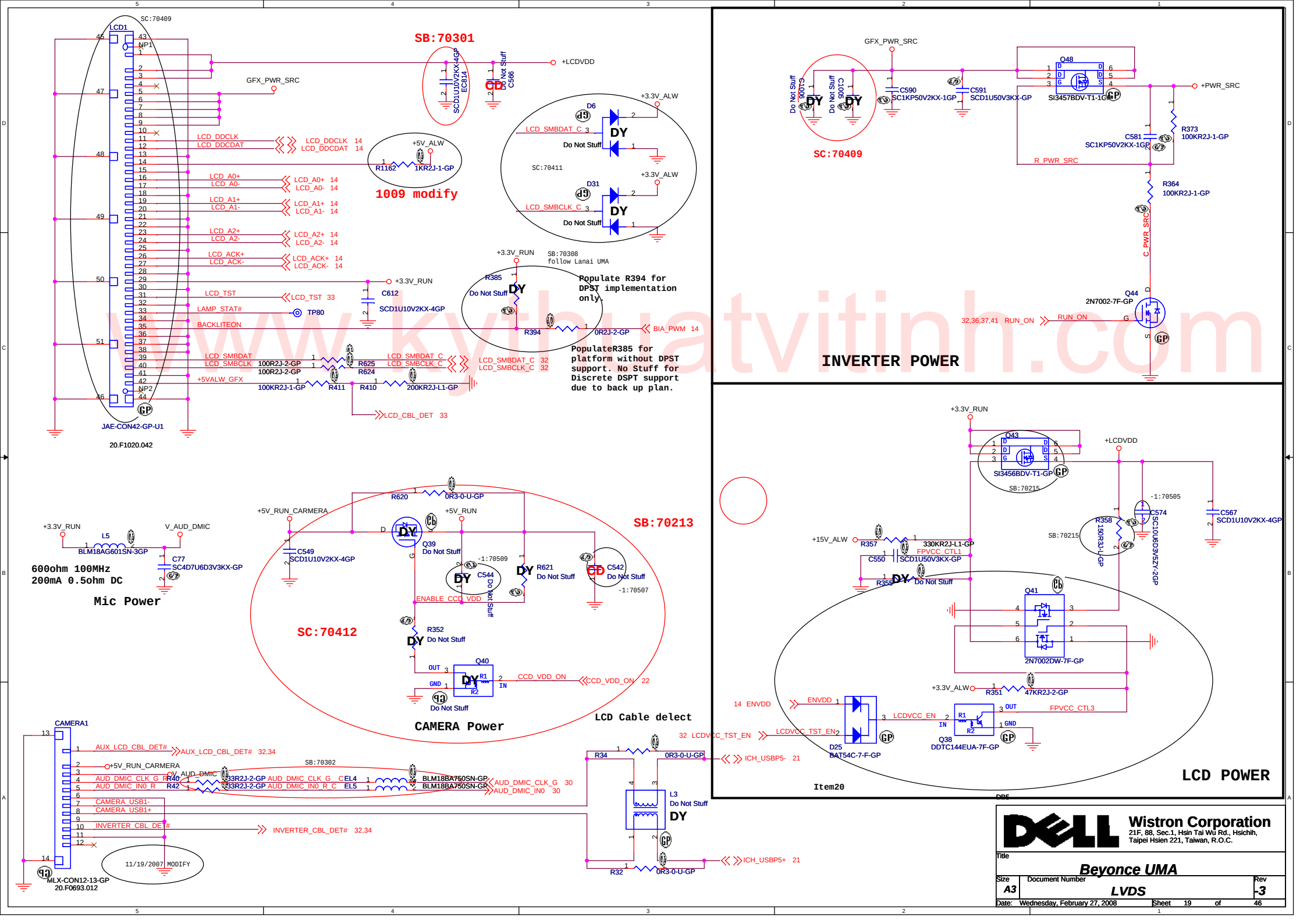
Size: A3 | Document Number: DDR2-SODIMM1 | Rev: -3

Date: Wednesday, February 27, 2008 | Sheet 15 of 46






CRT conn.
HDMI CONN
Setting R,G,B trace impedance to 50 ohm.
30ohm 100MHz
1000mA 0.05ohm DC
120ohm 100MHz
200mA 0.2ohm DC
120ohm 100MHz
200mA 0.2ohm DC
Item18
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Beyonce UMA
CRT/HDMI
-3
Wednesday, February 27, 2008
18
46


LCD1
JAE-CON42-GP-U1
20.F1020.042
SB:70301
SC:70409
SC:70411
1009 modify
Do Not Stuff
DY
Populate R394 for DPST implementation only.
PopulateR385 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.
SB:70308
follow Lanai UMA
INVERTER POWER
SI3457BDV-T1-1GP
2N7002-7F-GP
SB:70213
SC:70412
CAMERA Power
Mic Power
600ohm 100MHz
200mA 0.5ohm DC
LCD Cable delect
CAMERA1
MLX-CON12-13-GP
20.F0693.012
11/19/2007 MODIFY
SB:70302
LCD POWER
Item20
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Beyonce UMA
LVDS
Size A3
Rev -3
Date: Wednesday, February 27, 2008
Sheet 19 of 46

We would like to change X5 to 82.10026.021 and X3 to 82.30001.691.

RTC circuitry

ICH8-Strap PIN

integrated VccSus1_05,VccSus1_5,VccCL1_5	
ICH_INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
ICH_LAN100_SLP	High=Enable Low=Disable

This circuit is only needed if the platform has the SNIFFER

Distance between the ICH8-M and cap on the "P" signal should be identical distance between the ICH8-M and cap on the "N" signal for same pair.

SM_SATASB Place within 500 mil of ICH8-M

GLAN_COMP place within 500 mil of ICH8M

Change to 71.0ICH8.M08

ICH8-Strap PIN

XOR Chain Entrance Strap		
ICH_RSVD	ACZ_DOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

SC:70412T

IC SB ICH8M QM74 MM#882553 B0

ICH8-M-1-GP-U-NF 71.0ICH8.A0U

DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA

Size: A3 | Document Number: ICH8M-RTC/IDE/LPC/DHI (1/4) | Rev: -3

Date: Wednesday, February 27, 2008 | Sheet 20 of 46

ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R168)	low = A16 swap override enable high = default	

PCI_GNT#0 R582 1 1KR2J-1-GP
ICH_SPI_CS1# R R292 DY 1 Do Not Stuff
PCI_GNT#3 R581 DY 1 Do Not Stuff

PCI I/F PULL HIGH

RP4 SRN8K2J-2-GP-U
PCI_SERR# 1 10 +3.3V_RUN
PCI_TRDY# 2 9 PCI_STOP#
PCI_IRDY# 3 8 PCI_DEVSEL#
PCI_PLOCK# 4 7 PCI_FRAME#
+3.3V_RUN 5 6 PCI_REQ#1

RP5 SRN8K2J-2-GP-U
PCI_PIRQB# 1 10 +3.3V_RUN
PCI_REQ#0 2 9 SB_WPAN_PCIE_RST#
PCI_PIRQC# 3 8 PCI_PIRQA#
USB_IDE# 4 7 PCI_PIRQD#
+3.3V_RUN 5 6 PCI_PERR#
22 USB_IDE#

BIOS should not enable the internal GPIO pull up

+3.3V_RUN RN52 SRN10KJ-5-GP
2 SB_WLAN_PCIE_RST#
1 SB_NB_PCIE_RST#

R295 1 20KR3J-1-GP SB_WWAN_PCIE_RST#
RN53 SRN100KJ-6-GP
2 SB_NB_PCIE_RST#
1 SB_WLAN_PCIE_RST#
R296 1 20KR3J-1-GP SB_LOM_PCIE_RST#

R611 15R2J-GP -1:70505 ICH_SPI_CS0#
+3.3V_ALW U80
33 SPI_CS0# R612 DY 1 SPI_CS0# R 4 Do Not Stuff
VCC B 1
Y DY A 2
GND 3
Do Not Stuff
R597 -1:70505 32 SIO_SPI_CS#

PCIE Interface Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	LAN

PCI Interface Routing

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

Add Buffers as need for Loading and Fanout concerns

28 PCI_AD[0..31] PCI_AD[0..31]
U29C 3 OF 6
PCI
AD0 D20 PCI_AD0
AD1 E19 PCI_AD1
AD2 D19 PCI_AD2
AD3 A20 PCI_AD3
AD4 D17 PCI_AD4
AD5 A21 PCI_AD5
AD6 A19 PCI_AD6
AD7 C19 PCI_AD7
AD8 A18 PCI_AD8
AD9 B16 PCI_AD9
AD10 A12 PCI_AD10
AD11 E16 PCI_AD11
AD12 A14 PCI_AD12
AD13 G16 PCI_AD13
AD14 A15 PCI_AD14
AD15 B6 PCI_AD15
AD16 C11 PCI_AD16
AD17 A9 PCI_AD17
AD18 D11 PCI_AD18
AD19 B12 PCI_AD19
AD20 C12 PCI_AD20
AD21 D10 PCI_AD21
AD22 C7 PCI_AD22
AD23 F13 PCI_AD23
AD24 E11 PCI_AD24
AD25 E13 PCI_AD25
AD26 E12 PCI_AD26
AD27 D8 PCI_AD27
AD28 A6 PCI_AD28
AD29 E8 PCI_AD29
AD30 D6 PCI_AD30
AD31 A3 PCI_AD31

REQ0# A4 PCI_REQ#0
GNT0# D7 PCI_GNT#0
REQ1#/GPIO50 E18 PCI_REQ#1 — PCI_REQ#1 28
GNT1#/GPIO51 C18 PCI_GNT#1 — PCI_GNT#1 28
REQ2#/GPIO52 B19 SB_WWAN_PCIE_RST# — SB_WWAN_PCIE_RST# 27
GNT2#/GPIO53 F18 PCI_GNT#2 1 TP114
GNT3#/GPIO55 C10 PCI_GNT#3
REQ3#/GPIO54 A11 SB_LOM_PCIE_RST# — SB_LOM_PCIE_RST# 25
PCI_C_BE#[0..3] — PCI_C_BE#[0..3] 28
C/BE0# C17 PCI_C_BE#0
C/BE1# E15 PCI_C_BE#1
C/BE2# E16 PCI_C_BE#2
C/BE3# E17 PCI_C_BE#3
IRDY# C8 PCI_IRDY# — PCI_IRDY# 28
PAR D9 PCI_PAR — PCI_PAR 28
PCIRST# G6 PCI_RST# G
DEVSEL# D16 PCI_DEVSEL# — PCI_DEVSEL# 28
PERR# A7 PCI_PERR# — PCI_PERR# 28
FRAME# A17 PCI_FRAME# — PCI_FRAME# 28
PLOCK# B7 PCI_PLOCK# 1 TP124
SERR# F10 PCI_SERR# — PCI_SERR# 28
STOP# C16 PCI_STOP# — PCI_STOP# 28
TRDY# C9 PCI_TRDY# — PCI_TRDY# 28
PLTRST# AG24 PCI_PLTRST#
PCICLK B10 CLK_PCI_ICH — CLK_PCI_ICH 6
PME# G7 ICH_PME# — ICH_PME# 33

R281 33R2J-2-GP 1 PCI_RST# 28

+3.3V_SUS
16mA
U28
C404 CP 1 Do Not Stuff
1 A VCC 5
2 B
3 GND Y 4 PLT_RST# S
SNLVC1G08DCKRG4-GP
R260 33R2J-2-GP 1 PLTRST# 10,17,25,26,27,32
R261 DY 1 Do Not Stuff

Interrupt I/F

SB:70302
PIRQA# F9 PCI_PIRQA#
PIRQB# B5 PCI_PIRQB#
PIRQC# C5 PCI_PIRQC#
PIRQD# A10 PCI_PIRQD#
28 PCI_PIRQC#
28 PCI_PIRQD#
PIRQE#/GPIO2 F8 SB_WPAN_PCIE_RST# — SB_WPAN_PCIE_RST# 27
PIRQF#/GPIO3 G11 SB_WLAN_PCIE_RST# — SB_WLAN_PCIE_RST# 27
PIRQG#/GPIO4 F12 SB_NB_PCIE_RST# — SB_NB_PCIE_RST# 10
PIRQH#/GPIO5 B3 PCIE_MCARD2_DET# — PCIE_MCARD2_DET# 27
GP
ICH8-M-1-GP-U-NF 71.0ICH8.A0U
IC SB ICH8M QM74 MM#882553 B0

CLK_ICH_14M EMI Mode Place close to ICH8-M

CLK_PCI_ICH
R294 Do Not Stuff DY
CLK_ICHPCI
C462 Do Not Stuff DY
EMI

MiniCard WWAN

27 PCIE_RX1- PCIE_RX1-
27 PCIE_RX1+ PCIE_RX1+
27 PCIE_TX1- C409 DY Do Not Stuff PCIE_TXN1_C N29
27 PCIE_TX1+ C407 DY Do Not Stuff PCIE_TXP1_C N28

MiniCard WLAN

27 PCIE_RX2- PCIE_RX2-
27 PCIE_RX2+ PCIE_RX2+
27 PCIE_TX2- C416 1 SCD1U10V2KX-4GP PCIE_TXN2_C L29
27 PCIE_TX2+ C414 1 SCD1U10V2KX-4GP PCIE_TXP2_C L28

Express Card

26 PCIE_RX4- PCIE_RX4-
26 PCIE_RX4+ PCIE_RX4+
26 PCIE_TX4- C429 1 SCD1U10V2KX-4GP PCIE_TXN3_C G29
26 PCIE_TX4+ C425 1 SCD1U10V2KX-4GP PCIE_TXP3_C G28

LAN

25 PCIE_RX6- PCIE_RX6-
25 PCIE_RX6+ PCIE_RX6+
25 PCIE_TX6- C433 1 SCD1U10V2KX-4GP PCIE_TXN4_C C29
25 PCIE_TX6+ C432 1 SCD1U10V2KX-4GP PCIE_TXP4_C C28

32 ICH_EC_SPI_CLK R291 15R2J-GP ICH_EC_SPI_CLK_R
ICH_SPI_CS# ICH_SPI_CS1# R
32 ICH_EC_SPI_DO R290 15R2J-GP ICH_EC_SPI_DO_R
32 ICH_EC_SPI_DIN ICH_EC_SPI_DIN

38 USB_OC0# USB_OC0#
38 USB_OC1# USB_OC1#
USB_OC2# USB_OC3# USB_OC4# USB_OC5# USB_OC6# USB_OC7# USB_OC8# USB_OC9#

U29B 2 OF 6

PCI-Express
PERN1 P27
PERP1 P26
PETN1 N29
PETP1 N28
PERN2 M27
PERP2 M26
PETN2 L29
PETP2 L28
PERN3 K27
PERP3 K26
PETN3 J29
PETP3 J28
PERN4 H27
PERP4 H26
PETN4 G29
PETP4 G28
PERN5 F27
PERP5 F26
PETN5 E29
PETP5 E28
PERN6/GLAN_RXN D27
PERP6/GLAN_RXP D26
PETN6/GLAN_TXN C29
PETP6/GLAN_TXP C28

SPI
SPI_CLK C23
SPI_CS0# B23
SPI_CS1# E22
SPI_MOSI D23
SPI_MISO F21

USB
OC0# AJ19
OC1#/GPIO40 AG16
OC2#/GPIO41 AG15
OC3#/GPIO42 AE15
OC4#/GPIO43 AF15
OC5#/GPIO29 AG17
OC6#/GPIO30 AD12
OC7#/GPIO31 AJ18
OC8# AD14
OC9# AH18

Direct Media Interface
DMI0RXN V27 DMI_MTX_IRX_N0 — DMI_MTX_IRX_N0 10
DMI0RXP V26 DMI_MTX_IRX_P0 — DMI_MTX_IRX_P0 10
DMI0TXN U29 DMI_MRX_ITX_N0 — DMI_MRX_ITX_N0 10
DMI0TXP U28 DMI_MRX_ITX_P0 — DMI_MRX_ITX_P0 10
DMI1RXN Y27 DMI_MTX_IRX_N1 — DMI_MTX_IRX_N1 10
DMI1RXP Y26 DMI_MTX_IRX_P1 — DMI_MTX_IRX_P1 10
DMI1TXN W29 DMI_MRX_ITX_N1 — DMI_MRX_ITX_N1 10
DMI1TXP W28 DMI_MRX_ITX_P1 — DMI_MRX_ITX_P1 10
DMI2RXN AB26 DMI_MTX_IRX_N2 — DMI_MTX_IRX_N2 10
DMI2RXP AB25 DMI_MTX_IRX_P2 — DMI_MTX_IRX_P2 10
DMI2TXN AA29 DMI_MRX_ITX_N2 — DMI_MRX_ITX_N2 10
DMI2TXP AA28 DMI_MRX_ITX_P2 — DMI_MRX_ITX_P2 10
DMI3RXN AD27 DMI_MTX_IRX_N3 — DMI_MTX_IRX_N3 10
DMI3RXP AD26 DMI_MTX_IRX_P3 — DMI_MTX_IRX_P3 10
DMI3TXN AC29 DMI_MRX_ITX_N3 — DMI_MRX_ITX_N3 10
DMI3TXP AC28 DMI_MRX_ITX_P3 — DMI_MRX_ITX_P3 10
DMI_CLKN T26 CLK_PCIE_ICH# — CLK_PCIE_ICH# 6
DMI_CLKP T25 CLK_PCIE_ICH — CLK_PCIE_ICH 6
DMI_ZCOMP
DMI_IRCOMP
Y23 DMI_COMP — R246 24D9R2F-L-GP — +1.5V_PCIE_ICH
Y24

USBP0N G3 ICH_USBP0- — ICH_USBP0- 38
USBP0P G2 ICH_USBP0+ — ICH_USBP0+ 38
USBP1N H5 ICH_USBP1- — ICH_USBP1- 38
USBP1P H4 ICH_USBP1+ — ICH_USBP1+ 38
USBP2N H2
USBP2P H1
USBP3N J3
USBP3P J2
USBP4N K5 ICH_USBP4- — ICH_USBP4- 34
USBP4P K4 ICH_USBP4+ — ICH_USBP4+ 34
USBP5N K2 ICH_USBP5- — ICH_USBP5- 19
USBP5P K1 ICH_USBP5+ — ICH_USBP5+ 19
USBP6N L3 ICH_USBP6- — ICH_USBP6- 26
USBP6P L2 ICH_USBP6+ — ICH_USBP6+ 26
USBP7N M5 ICH_USBP7- — ICH_USBP7- 29
USBP7P M4 ICH_USBP7+ — ICH_USBP7+ 29
USBP8N M2
USBP8P M1
USBP9N N3 ICH_USBP9- — ICH_USBP9- 27
USBP9P N2 ICH_USBP9+ — ICH_USBP9+ 27
USBRBIAS F2 USBRBIAS — R272 22D6R2F-L1-GP
USBRBIAS# F3
GP
ICH8-M-1-GP-U-NF 71.0ICH8.A0U
IC SB ICH8M QM74 MM#882553 B0

DMI_COMP R158 place within 500 mil of ICH8M

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	MINI Card WLAN
USB9	

DB5

Layout Note:
Place R235, R237 and R234 within 500 mils from ICH.

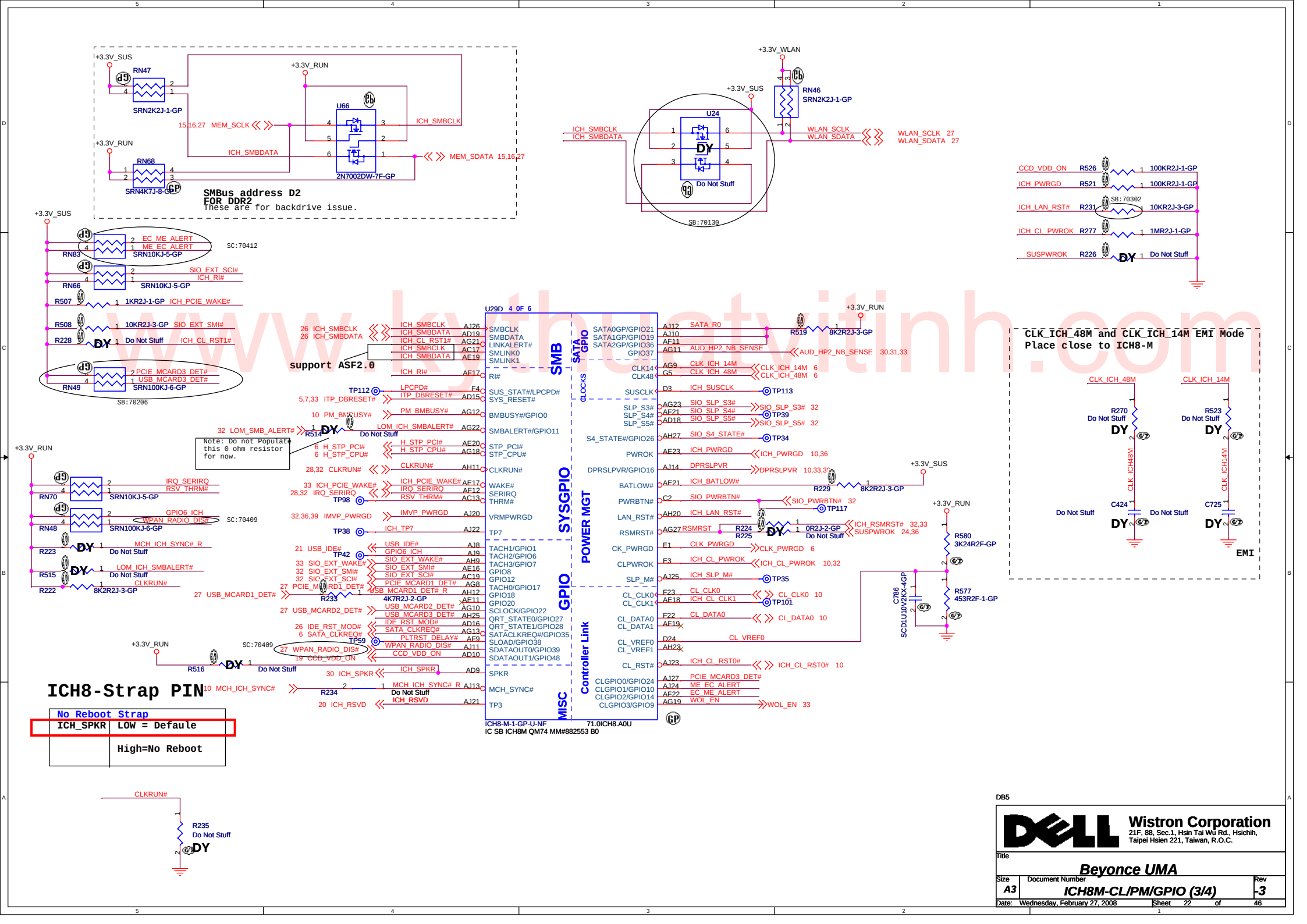
USBRBIAS close to ICH8M 500 mils and Trace impedance should be 60 ohm +/- 15%

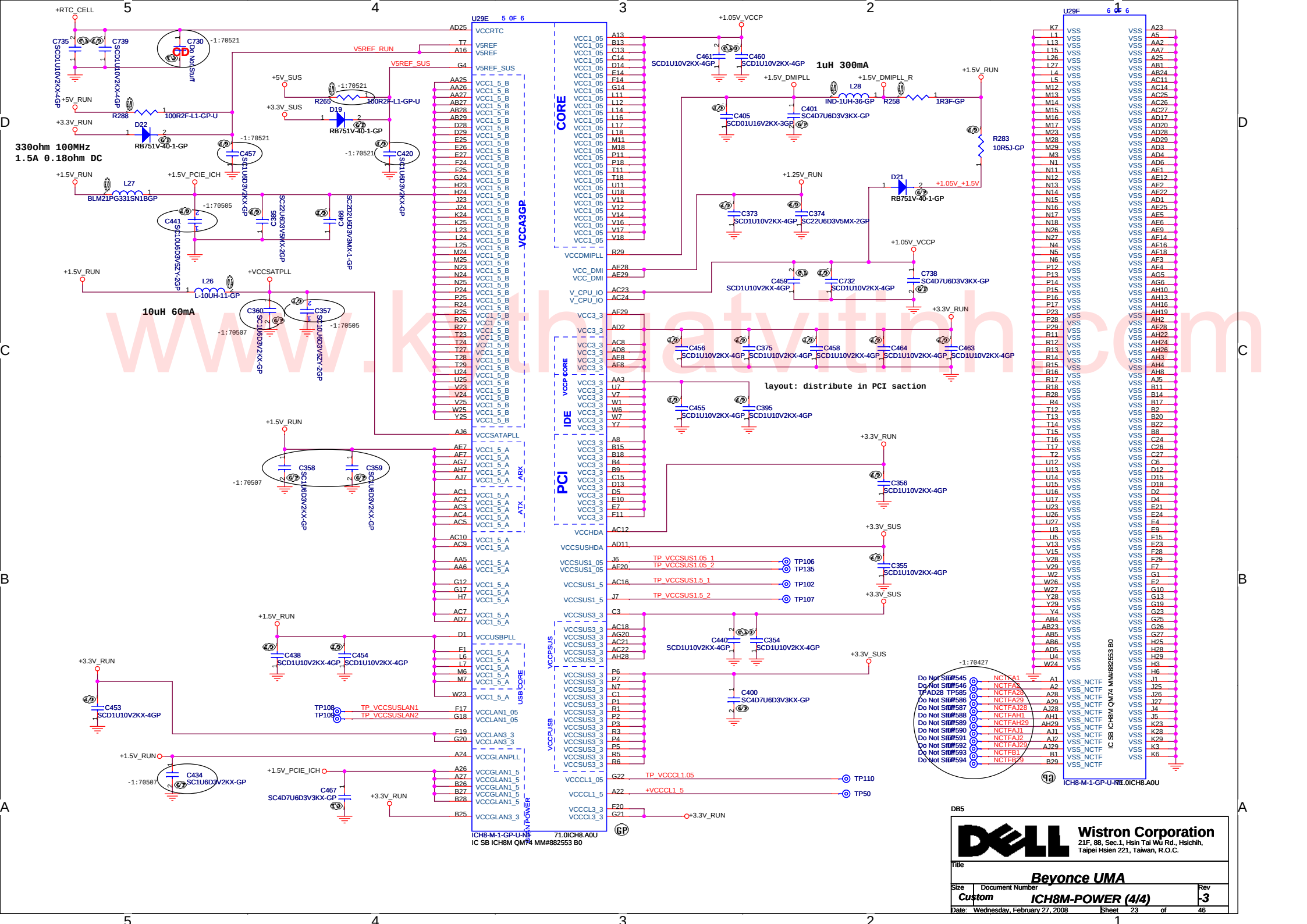
+3.3V_SUS
RN67 SRN10KJ-5-GP
USB_OC5# 4 1
USB_OC4# 2

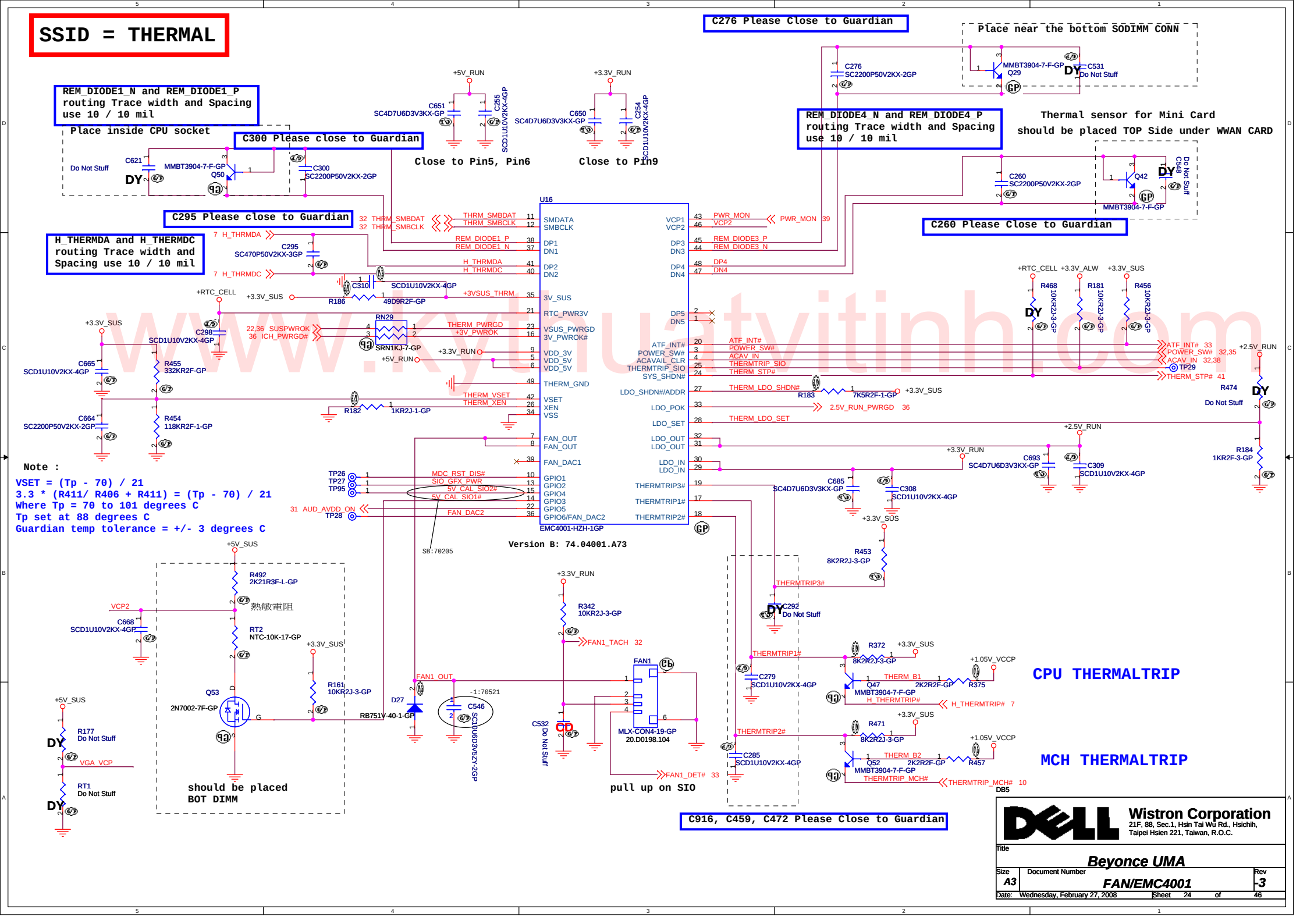
RP1 SRN10KJ-L3-GP
USB_OC6# 1 10 USB_OC1#
USB_OC9# 2 9 USB_OC2#
USB_OC7# 3 8 USB_OC3#
USB_OC0# 4 7 USB_OC8#
+3.3V_SUS 5 6

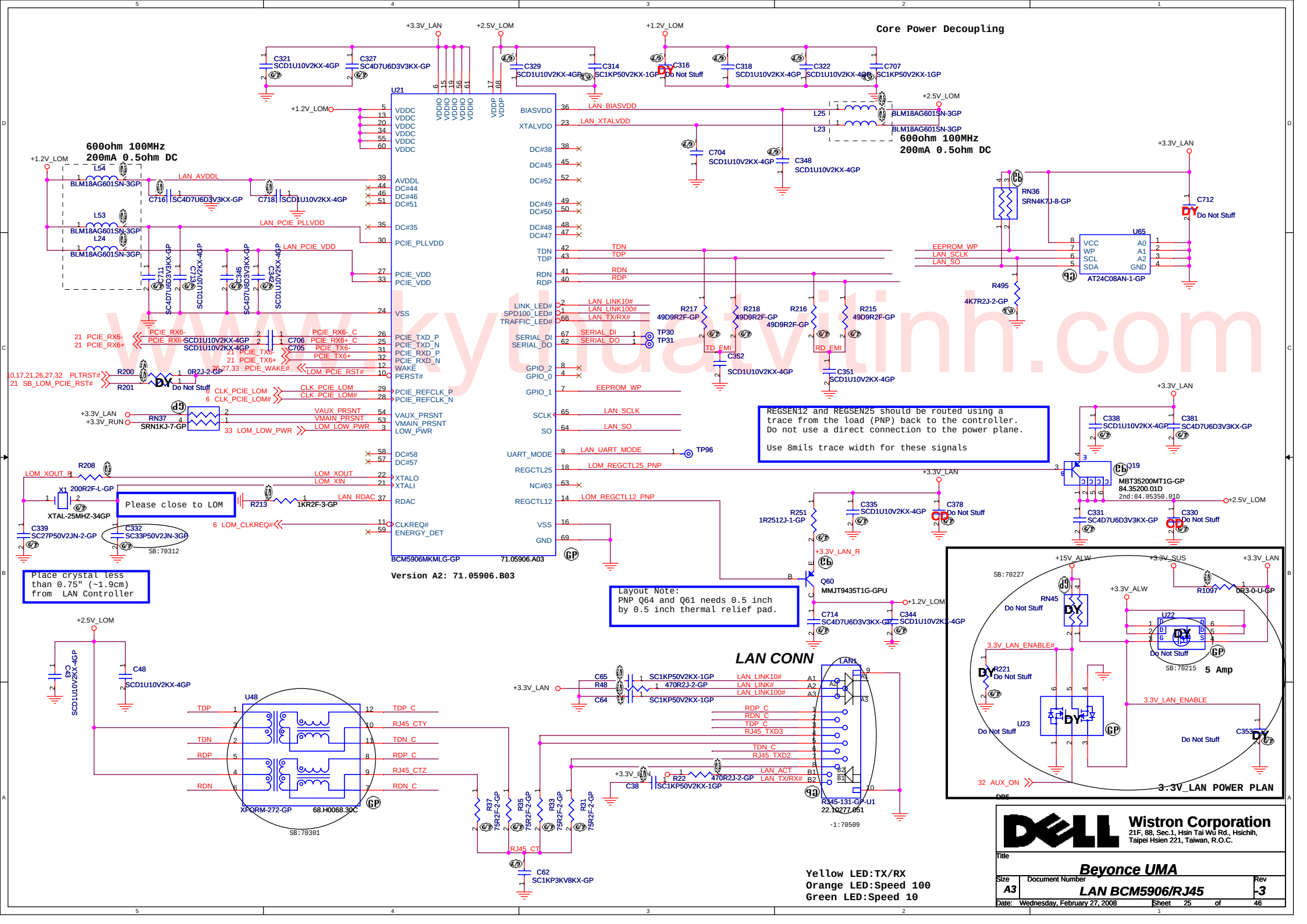
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA
Size: A3 | Document Number: ICH8M-PCIE/USB/SPI/DMI (2/4) | Rev: -3
Date: Wednesday, February 27, 2008 | Sheet 21 of 46


SMBus address D2
FOR DDR2
These are for backdrive issue.
support ASF2.0
Note: Do not Populate this 0 ohm resistor for now.
CLK_ICH_48M and CLK_ICH_14M EMI Mode
Place close to ICH8-M
EMI
ICH8-Strap PIN
No Reboot Strap
ICH_SPKR LOW = Defaule
High=No Reboot
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
ICH8-M-1-GP-U-NF
71.0ICH8.A0U
IC SB ICH8M QM74 MM#882553 B0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Beyonce UMA
ICH8M-CL/PM/GPIO (3/4)
Size A3
Rev -3
Date: Wednesday, February 27, 2008
Sheet 22 of 46

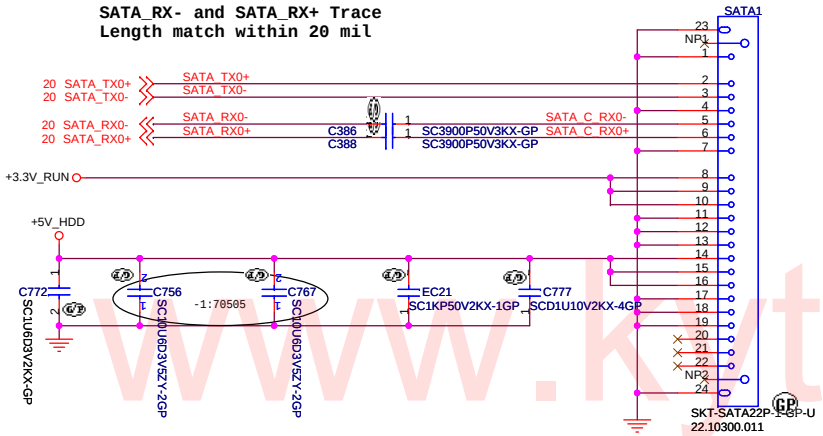

330ohm 100MHz
1.5A 0.18ohm DC
10uH 60mA
1uH 300mA
layout: distribute in PCI saction
U29E 5 OF 6
U29F 6 OF 6
CORE
VCCA3GP
VCCP CORE
IDE
PCI
ATX
USB CORE
VCCPSUS
VCCPUSB
RTC POWER
ICH8-M-1-GP-U-NS 71.0ICH8.A0U
IC SB ICH8M QM74 MM#882553 B0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Beyonce UMA
Custom
ICH8M-POWER (4/4)
-3
Wednesday, February 27, 2008
Sheet 23 of 46


SSID = THERMAL
C276 Please Close to Guardian
Place near the bottom SODIMM CONN
REM_DIODE1_N and REM_DIODE1_P routing Trace width and Spacing use 10 / 10 mil
Place inside CPU socket
C300 Please close to Guardian
Close to Pin5, Pin6
Close to Pin9
REM_DIODE4_N and REM_DIODE4_P routing Trace width and Spacing use 10 / 10 mil
Thermal sensor for Mini Card should be placed TOP Side under WWAN CARD
C295 Please close to Guardian
C260 Please Close to Guardian
H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil
U16
EMC4001-HZH-1GP
Version B: 74.04001.A73
Note :
VSET = (Tp - 70) / 21
3.3 * (R411/ R406 + R411) = (Tp - 70) / 21
Where Tp = 70 to 101 degrees C
Tp set at 88 degrees C
Guardian temp tolerance = +/- 3 degrees C
should be placed BOT DIMM
pull up on SIO
CPU THERMALTRIP
MCH THERMALTRIP
C916, C459, C472 Please Close to Guardian
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Beyonce UMA
FAN/EMC4001
Size A3
Rev -3
Date: Wednesday, February 27, 2008
Sheet 24 of 46

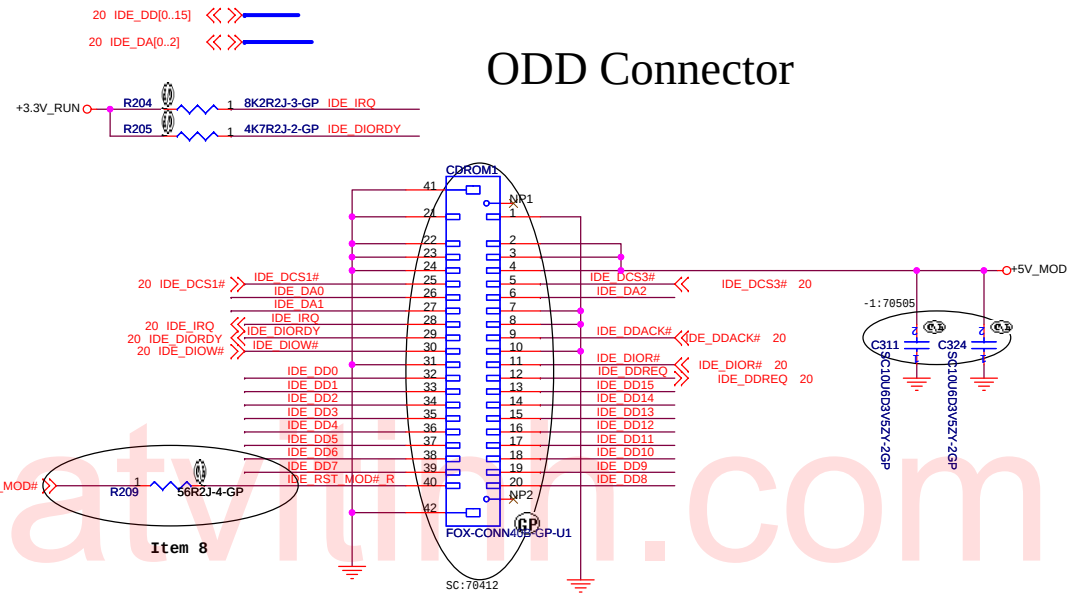

Core Power Decoupling
600ohm 100MHz
200mA 0.5ohm DC
600ohm 100MHz
200mA 0.5ohm DC
U21
BCM5906MKMLG-GP
71.05906.A03
Version A2: 71.05906.B03
REGSEN12 and REGSEN25 should be routed using a trace from the load (PNP) back to the controller. Do not use a direct connection to the power plane.
Use 8mils trace width for these signals
Please close to LOM
Place crystal less than 0.75" (~1.9cm) from LAN Controller
Layout Note: PNP Q64 and Q61 needs 0.5 inch by 0.5 inch thermal relief pad.
LAN CONN
U48
XFORM-272-GP
68.H0068.30C
RJ45-131-GP-U1
22.10277.051
Yellow LED:TX/RX
Orange LED:Speed 100
Green LED:Speed 10
3.3V_LAN POWER PLAN
5 Amp
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Beyonce UMA
LAN BCM5906/RJ45
Size A3
Rev -3
Date: Wednesday, February 27, 2008
Sheet 25 of 46

SSID = IDE & SATA

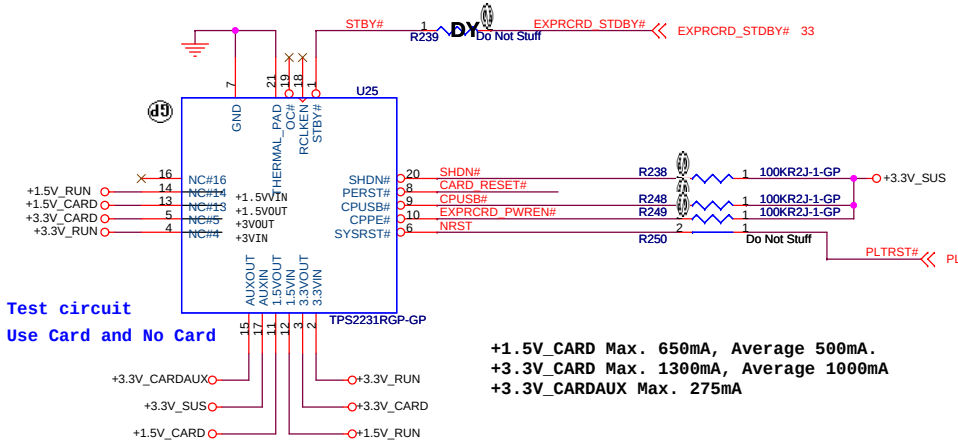
SATA HDD Connector

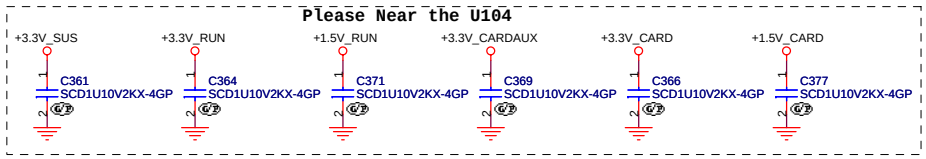


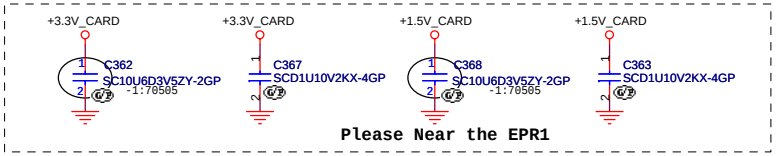
ODD Connector

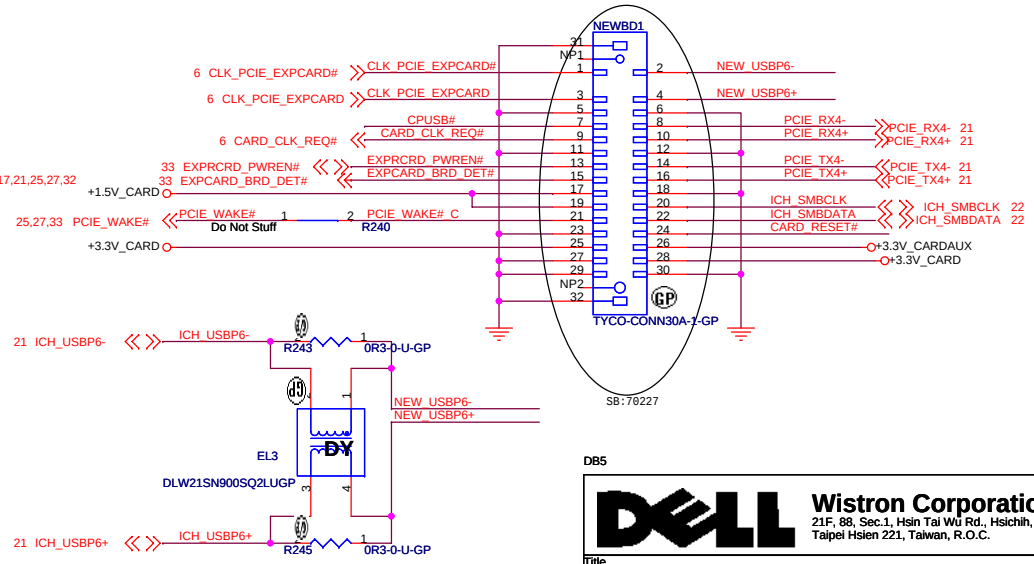


Express Card









DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Beyonce UMA	
Size A3	Document Number HDD/ODD/TO EXPRESS BD CONN	Rev -3
Date: Wednesday, February 27, 2008	Sheet 26 of 46	

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

DEBUG PINS

MiniCard WLAN connector

MiniCard WWAN connector

Prevent backdrive when WoW is enabled.

C587 Please Near the MINICARD1/Pin24

This circuit is only needed if the platform has the SNIFFER

C337 Please Near the MINICARD2/Pin24

Layout note: Place caps EC10-EC14 close Mini Card connector.

Layout note: Place caps EC87,EC88 close SIM Card connector.

For Debug card used only.

Close WLAN1

SB:070301

SC:70409

SC:70330 need close to SIM CN pin

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

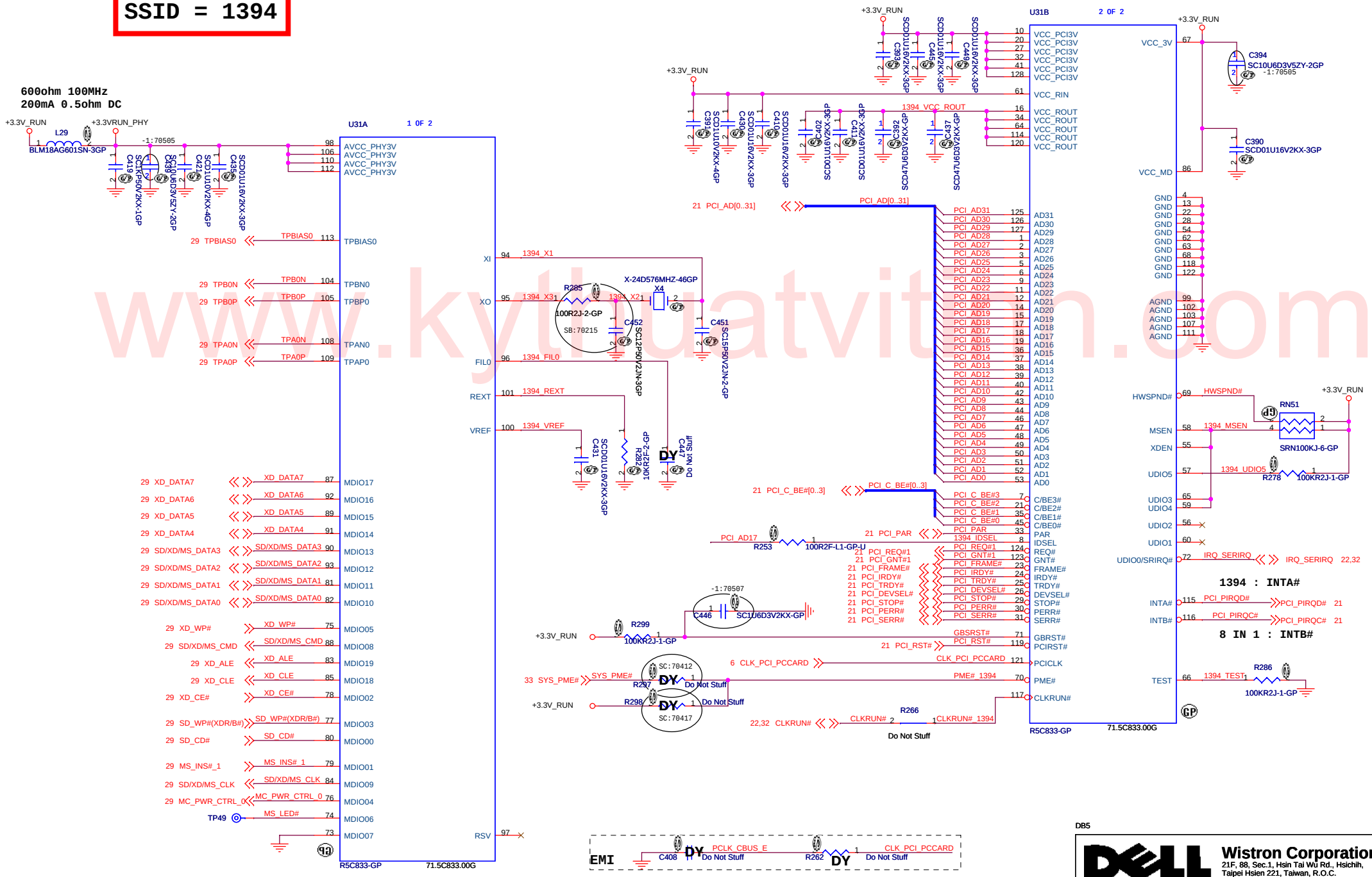
Title: Beyonce UMA

Size: A3 | Document Number: MINICARD/WLAN/WWAN | Rev: -1

Date: Wednesday, February 27, 2008 | Sheet 27 of 46

SSID = 1394

600ohm 100MHz
200mA 0.5ohm DC



DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

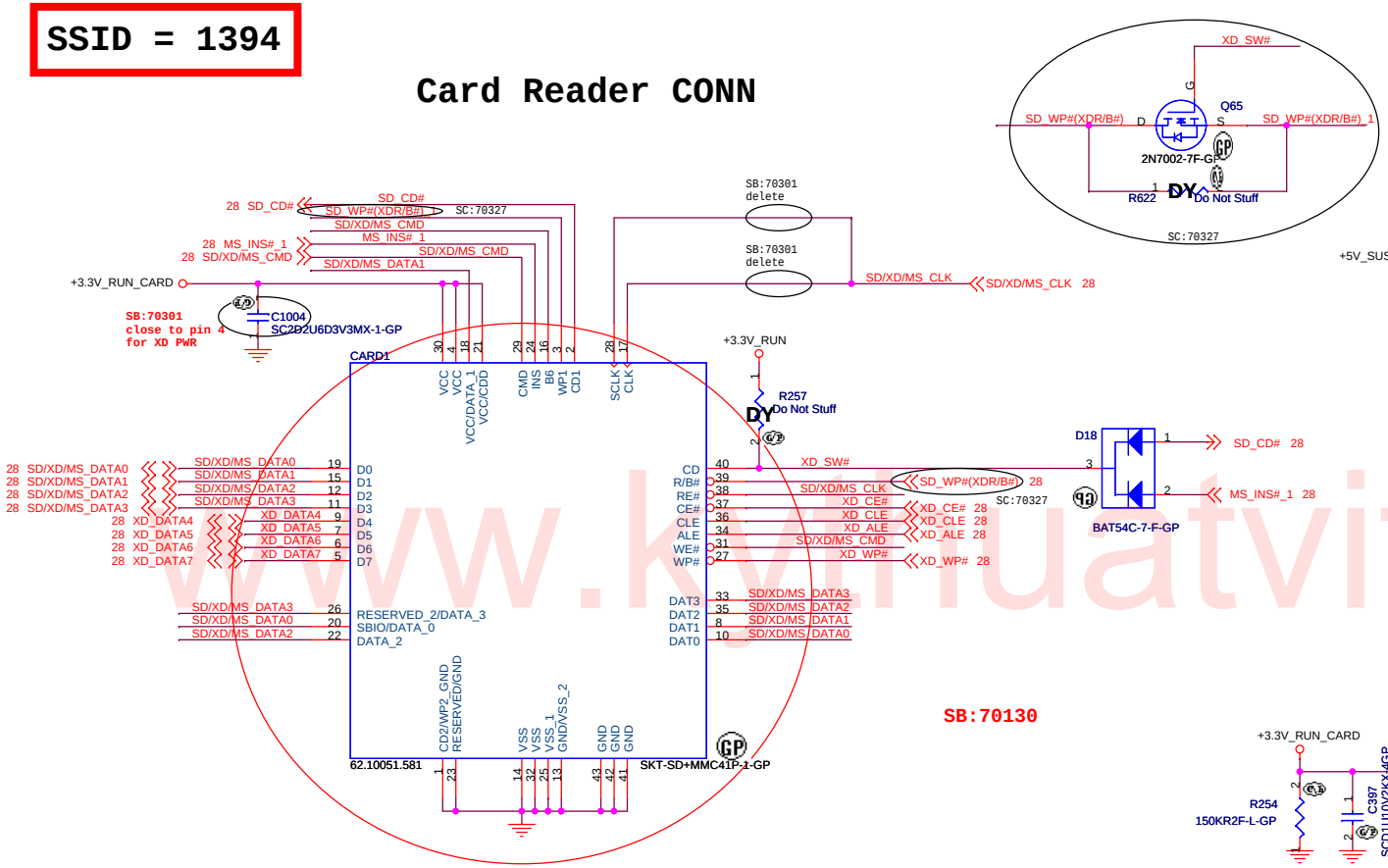
Title: Beyonce UMA

Size	Document Number	Rev
A3	1394 R5C833	-3

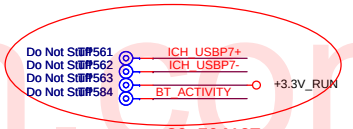
Date: Wednesday, February 27, 2008 Sheet 28 of 46

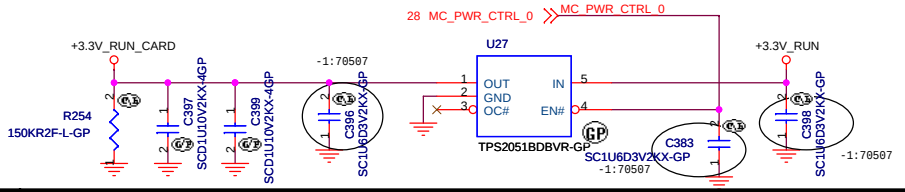
SSID = 1394

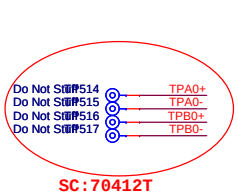
Card Reader CONN



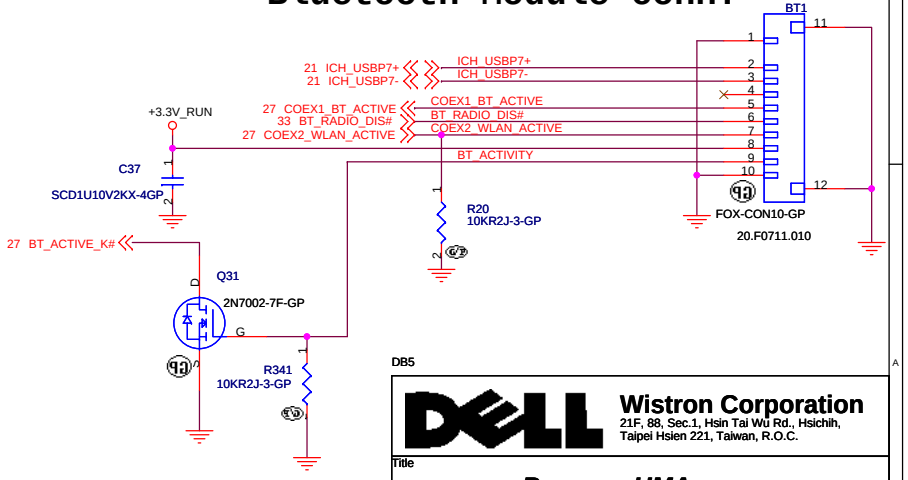
SNIFFER BOARD CONN







Bluetooth Module conn.



DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Beyonce UMA***

Size	Document Number	Rev
A3	8in1 /1394/SNIFFER BD CON/BT	-3

Date: Wednesday, February 27, 2008 Sheet 29 of 46

60ohm 100MHz
3000mA 0.05ohm DC

+3.3V_RUN
L60
BLM21PG600SN1GP
-1:70521
+3V_RUN_DVDD_CORE
C783 SCD1U10V2KX-4GP
C450 SCD1U10V2KX-4GP
C791 SC1U6D3V2KX-GP
-1:70507
R284 100KR2J-1-GP
+3V_RUN_DVDD_CORE3
C448 SC1KP50V2KX-1GP

U76
DVDD_CORE
DVDD_CORE
DVDD
BIT_CLK
SDATA_IN
SDATA_OUT
SYNC
RESET#
AVDD1
AVDD2
SENSE_A
SENSE_B
PORT_A_L
PORT_A_R
VREFOUT_A
PORT_B_L
PORT_B_R
VREFOUT_B
PORT_C_L
PORT_C_R
VREFOUT_C
PORT_D_L
PORT_D_R
VREFOUT_D
PORTE_L
PORTE_R
VREFOUT_E
PORTF_L
PORTF_R
VREFOUT_F
PORTG_L
PORTG_R
PORTH_L
PORTH_R
CD_L
CD_GND
CD_R
VOLUME UP/DMIC_0/GPIO1
VOLUME DN/DMIC_1/GPIO2
SPDIF_IN/GPIO0/DMIC_CLK
SPDIF_OUT
PC_BEEP
CAP2
VREFFILT
AVSS1
AVSS2
DVSS1
DVSS2
STAC9228X5TAEA2-GP
71.09228.00G

20 ICH_AZ_CODEC_BITCLK
20 ICH_AZ_CODEC_SDIN0
20 ICH_AZ_CODEC_SDOUT
20 ICH_AZ_CODEC_SYNC
20 ICH_AZ_CODEC_RST#
R583 33R2J-2-GP
SB_AZ_CODEC_SDIN0_R

+3.3V_RUN
U36
VCC OE# A GND Y
DY
Do Not Stuff
19 AUD_DMIC_CLK_G
AUD_DMIC_CLK_G
R306 0R2J-2-GP
AUD_DMIC_CLK

19 AUD_DMIC_IN0
31 AUD_EAPD#
AUD_DMIC_IN0
AUD_EAPD#
+3.3V_RUN
R584 4K7R2J-2-GP
AUD_DMIC_CLK
AUD_SPDIF_OUT
17 AUD_SPDIF_OUT

+VDDA
C770 SCD1U10V2KX-4GP
C436 SC1U6D3V2KX-GP
-1:70507

AUD_SENSE_A
AUD_SENSE_B
AUD_HP1_OUT_L
AUD_HP1_OUT_R
AUD_HP1_OUT_L 31
AUD_HP1_OUT_R 31
TO Audio OP
AUD_LINE_OUT_L
AUD_LINE_OUT_R
AUD_LINE_OUT_L 31
AUD_LINE_OUT_R 31
TO Audio OP
AUD_EXT_MIC_L
AUD_EXT_MIC_R
AUD_VREFOUT_B
AUD_HP2_OUT_L 31
AUD_HP2_OUT_R 31

PORT C : LEAVE NC
IF NO INTERNAL MICS.

Port A---> HP1
Port E---> ext Mic
Port D---> Speaker
Port F---> HP2

+VDDA
R569 5K1R2F-2-GP
R573 39K2R2F-L-GP
C778 SC1KP50V2KX-1GP
HP1_NB_SENSE
Q64 2N7002-7F-GP
AUD_HP1_NB_SENSE 31,33
+VDDA
R300 5K1R2F-2-GP
R316 39K2R2F-L-GP
SB:70106
R313 Do Not Stuff
DY
C758 SC1KP50V2KX-1GP
MIC_SWITCH
AUD_HP2_NB_SENSE 22,31,33
Q24 2N7002DW-7F-GP
HP2_NB_SENSE
AUD_MIC_SWITCH

Change R352 to 2.67K
1% for AD1984

If SENSE_A total length
> 6" change C to 0.1uF

C760 SC10U6D3V5ZY-2GP
C761 SC10U6D3V5ZY-2GP
-1:70505

PC BEEP
AUD_PC_BEEP
AUD_CAP2
AUD_VREFFLT
C780 SCD1U10V2KX-4GP
AUD_BEEP
R302 20KR2J-L2-GP
AUD_SYS_BEEP
R587 10KR2J-3-GP
SB:70302

+VDDA
U33
74AHC1G86GW-GP
VCC B A GND Y
From SB
ICH_SPKR 22
BEEP 32
From EC

XOR gate

Azalia I/F EMI

ICH_AZ_CODEC_SDOUT
R578 Do Not Stuff
DY
ICH_AZ_CODEC_SDOUT1
C787 Do Not Stuff
DY

Azalia I/F EMI

ICH_AZ_CODEC_BITCLK
R579 Do Not Stuff
DY
ICH_AZ_CODEC_BITCLK1
C788 Do Not Stuff
DY

MIC IN

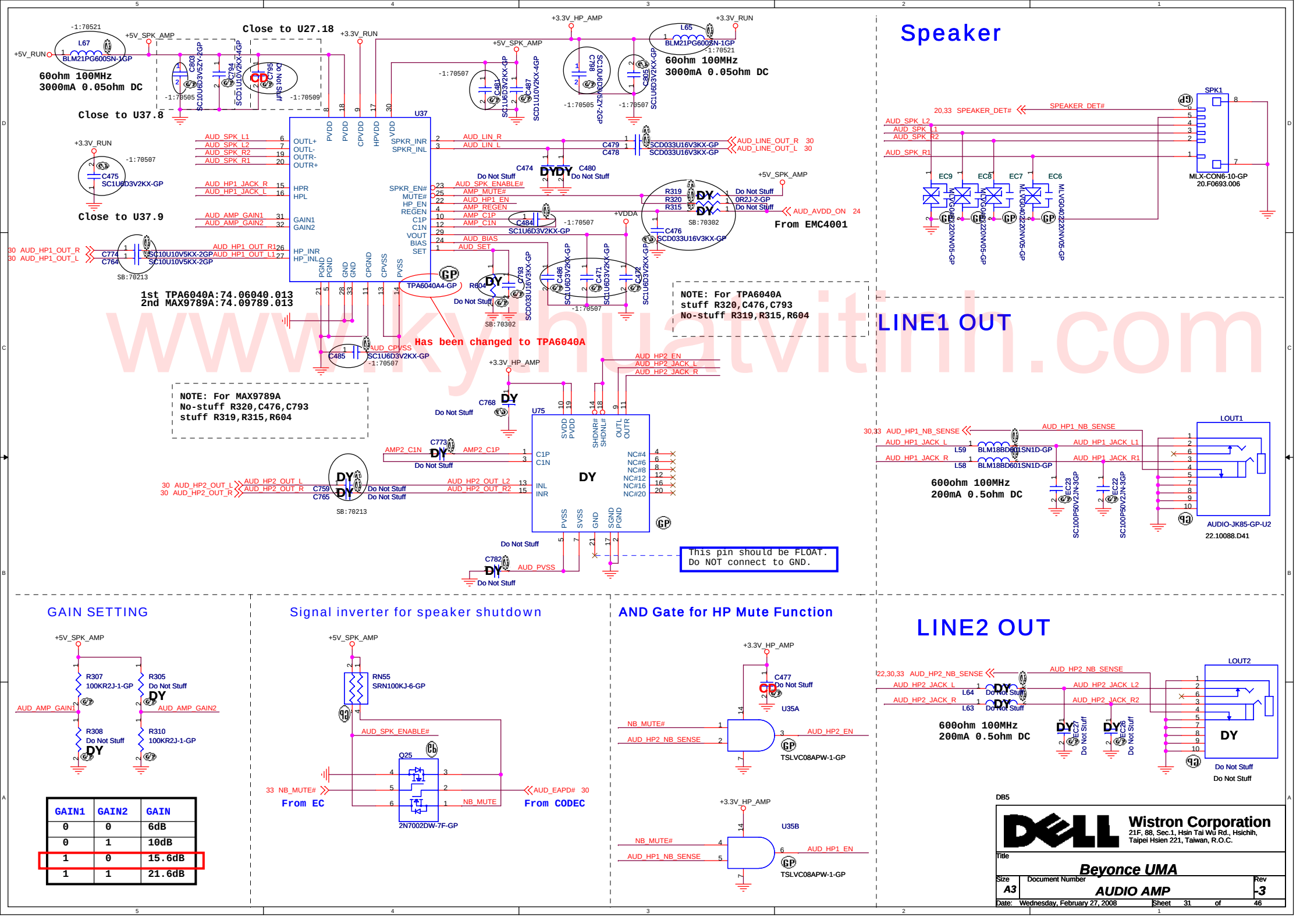
AUD_VREFOUT_B
R576 4K7R2J-2-GP
R599 4K7R2J-2-GP
-1:70521
C790 SC10U6D3V5ZY-2GP
AUD_EXT_MIC_L
AUD_EXT_MIC_R
C785 SC1U6D3V3KX-1GP
C789 SC1U6D3V3KX-1GP
-1:70505
MIC_IN_L_2
MIC_IN_R_2
R586
R594
MIC_IN_L_3
MIC_IN_R_3
Do Not Stuff
BLM18BD601SN1D-GP
L62
L61
BLM18BD601SN1D-GP
MIC_IN_L_C
MIC_IN_R_C
+3.3V_RUN
R602 100KR2J-1-GP
AUD_MIC_SWITCH
MIC1
EC25 SC100P50V2JN-3GP
EC24 SC100P50V2JN-3GP
AUDIO-JK85-GP-U2
22.10088.D41

600ohm 100MHz
200mA 0.5ohm DC

DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA
Size: A3
Document Number: CODEC STAC9228
Rev: -3
Date: Wednesday, February 27, 2008
Sheet 30 of 46



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

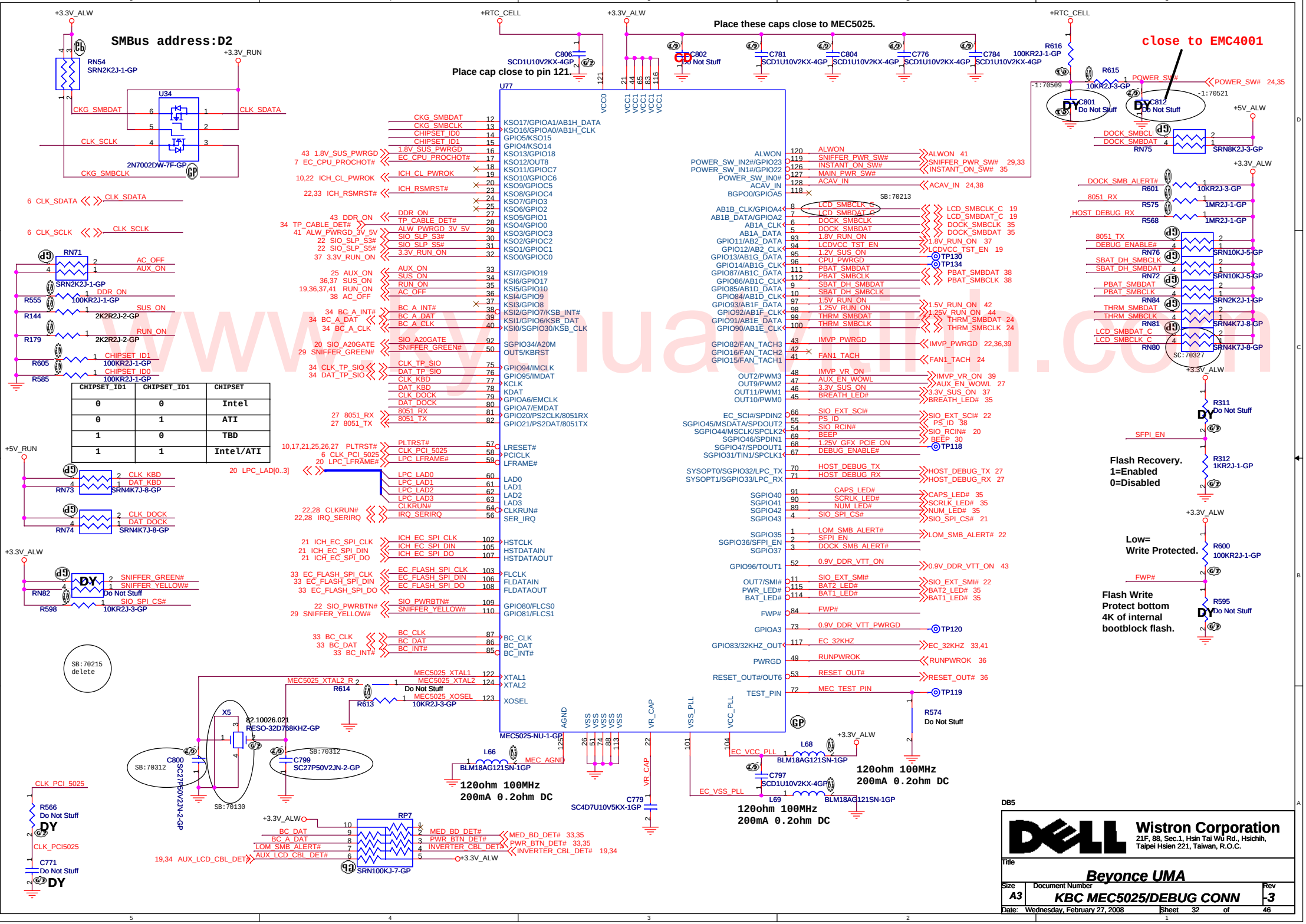
DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

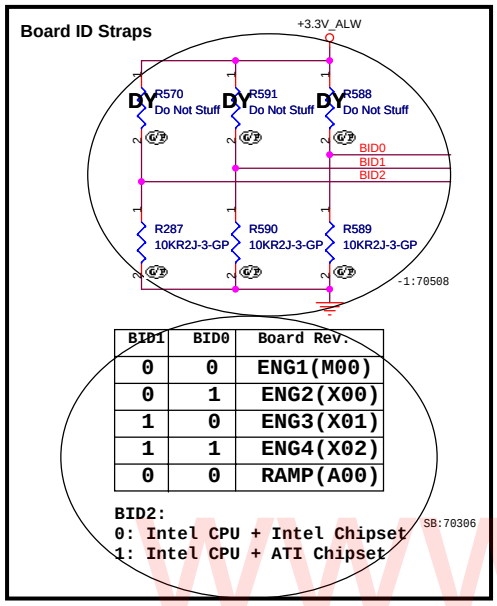
Title: **Beyonce UMA**

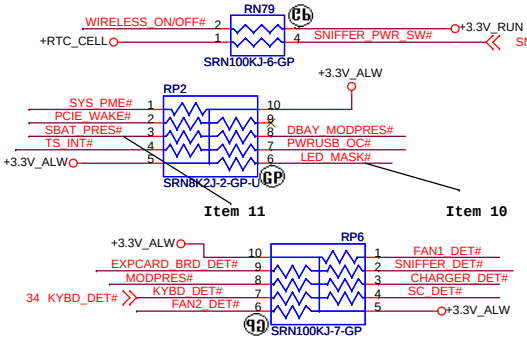
Size: A3 | Document Number: **AUDIO AMP** | Rev: -3

Date: Wednesday, February 27, 2008 | Sheet 31 of 46

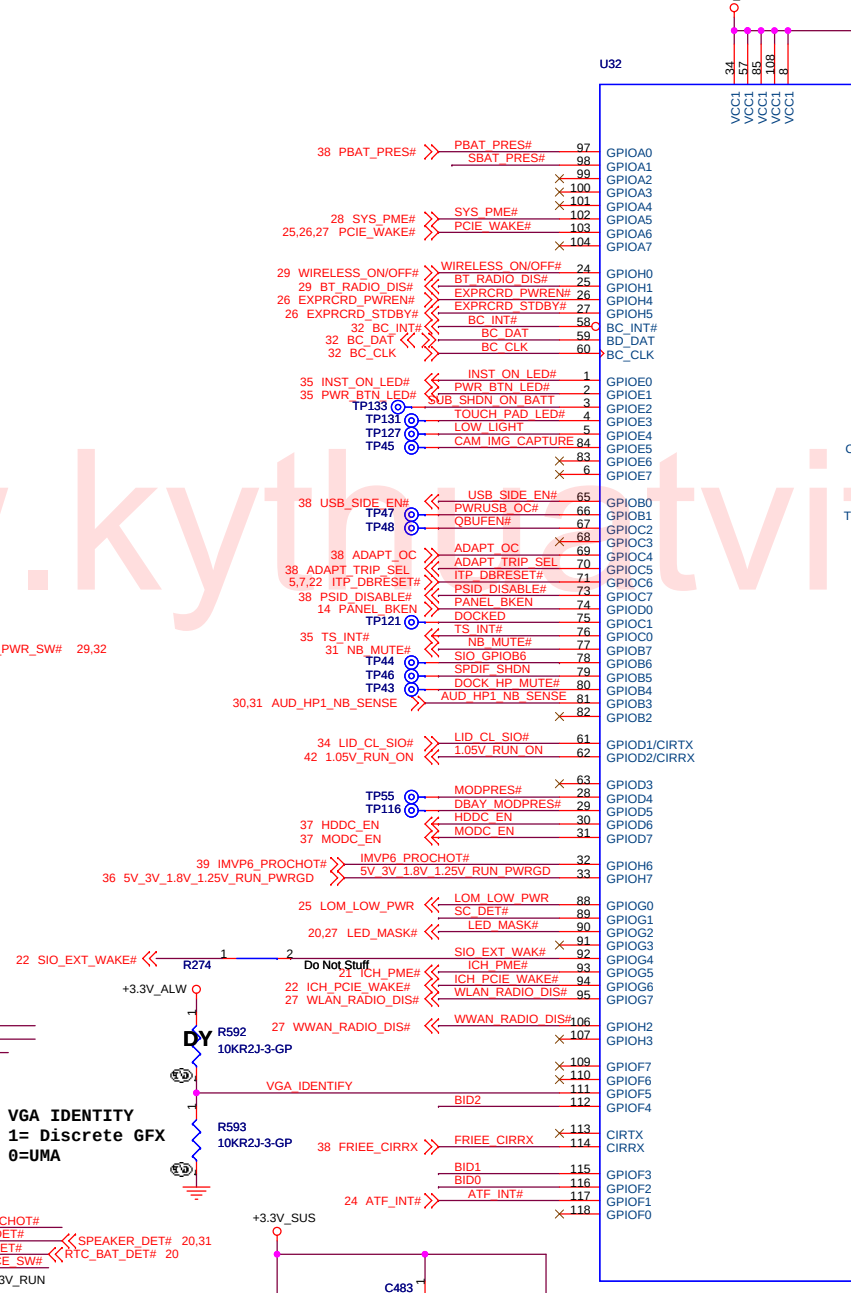


CHIPSET_ID1	CHIPSET_ID1	CHIPSET
0	0	Intel
0	1	ATI
1	0	TBD
1	1	Intel/ATI



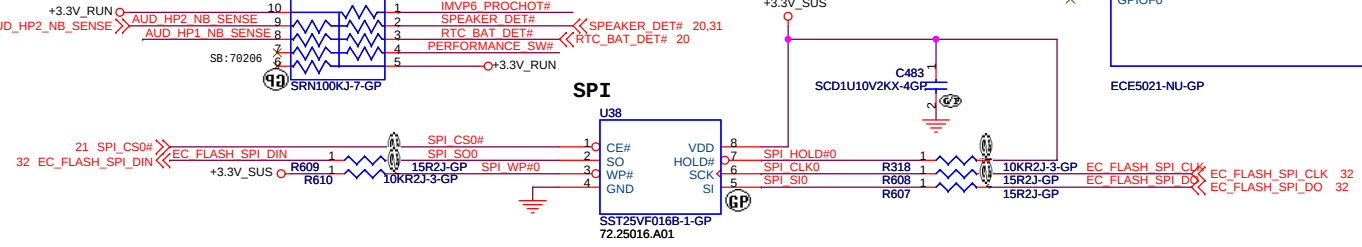


VGA IDENTITY
1= Discrete GFX
0=UMA



MEDID BD ID
0= CYPRESS
1=Synaptics

SPI



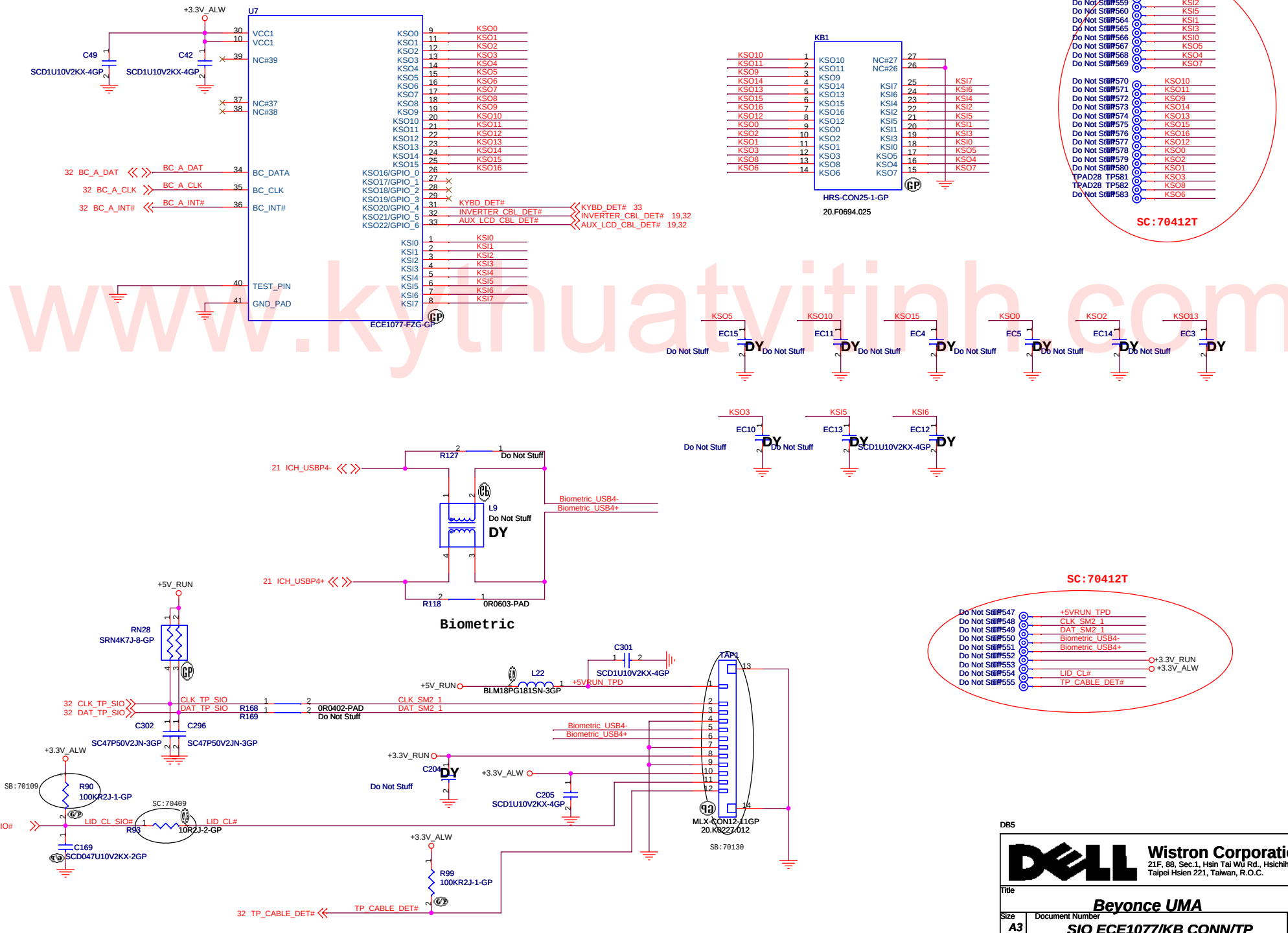
DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

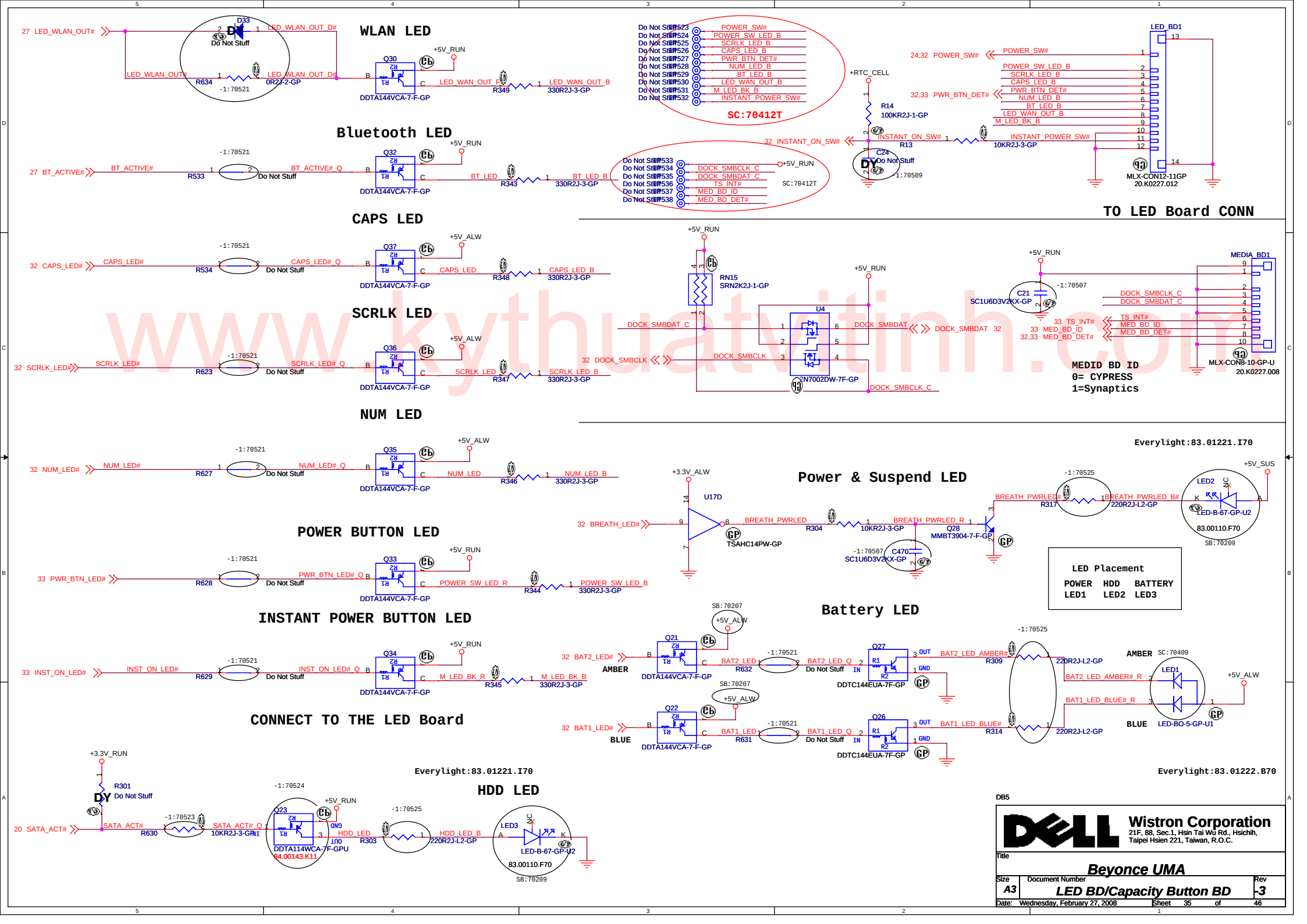
Title: Beyonce UMA

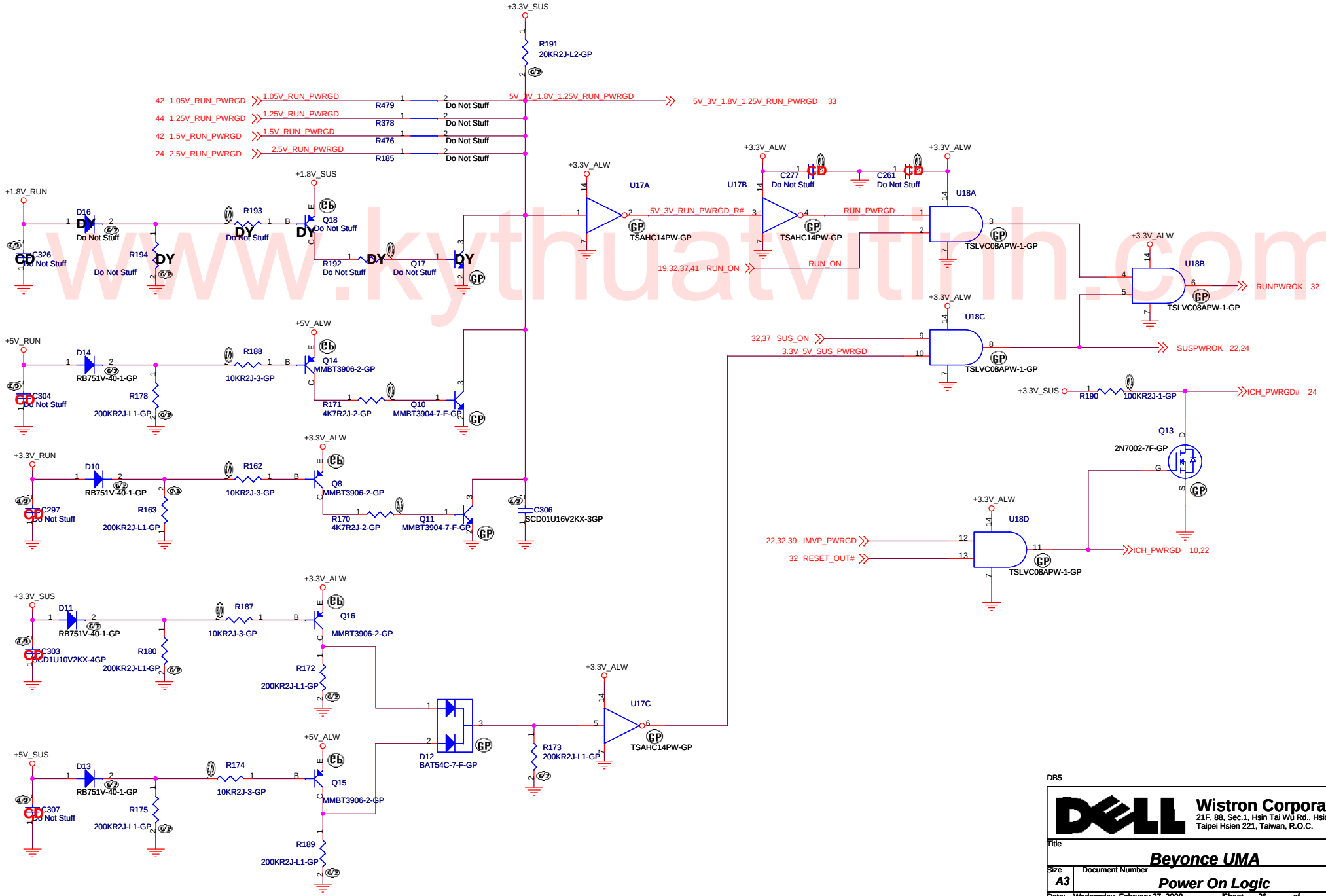
Size	Document Number	Rev
A3	SIO ECE5011/SPI ROM	-3

Date: Wednesday, February 27, 2008 Sheet 33 of 46



DB5		
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Beyonce UMA	
Size: A3	Document Number: SIO ECE1077/KB CONN/TP	Rev: -3
Date: Wednesday, February 27, 2008	Sheet 34 of 46	

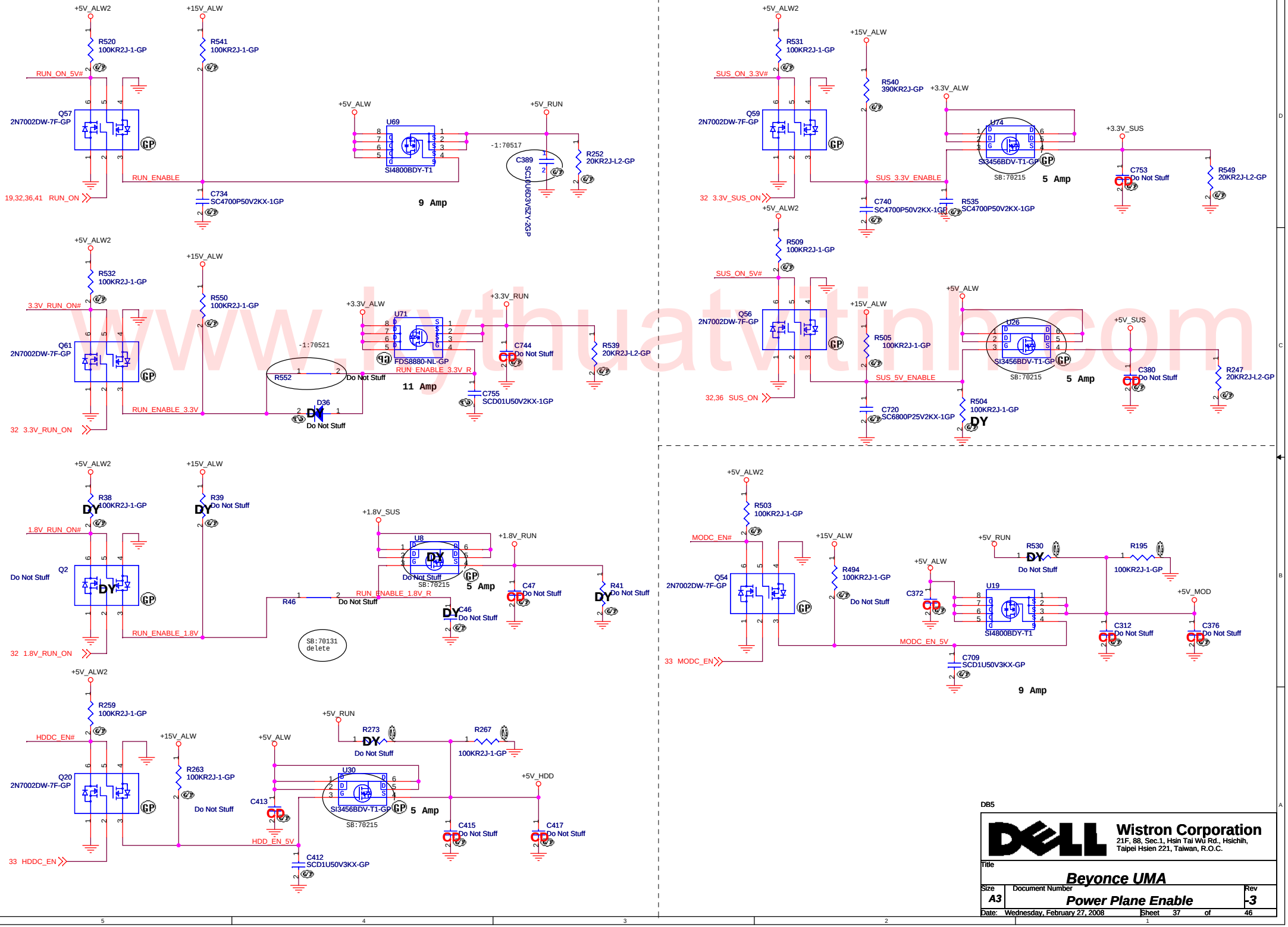




DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Beyonce UMA	
Size: A3	Document Number: Power On Logic	Rev: -3
Date: Wednesday, February 27, 2008	Sheet 36 of 46	



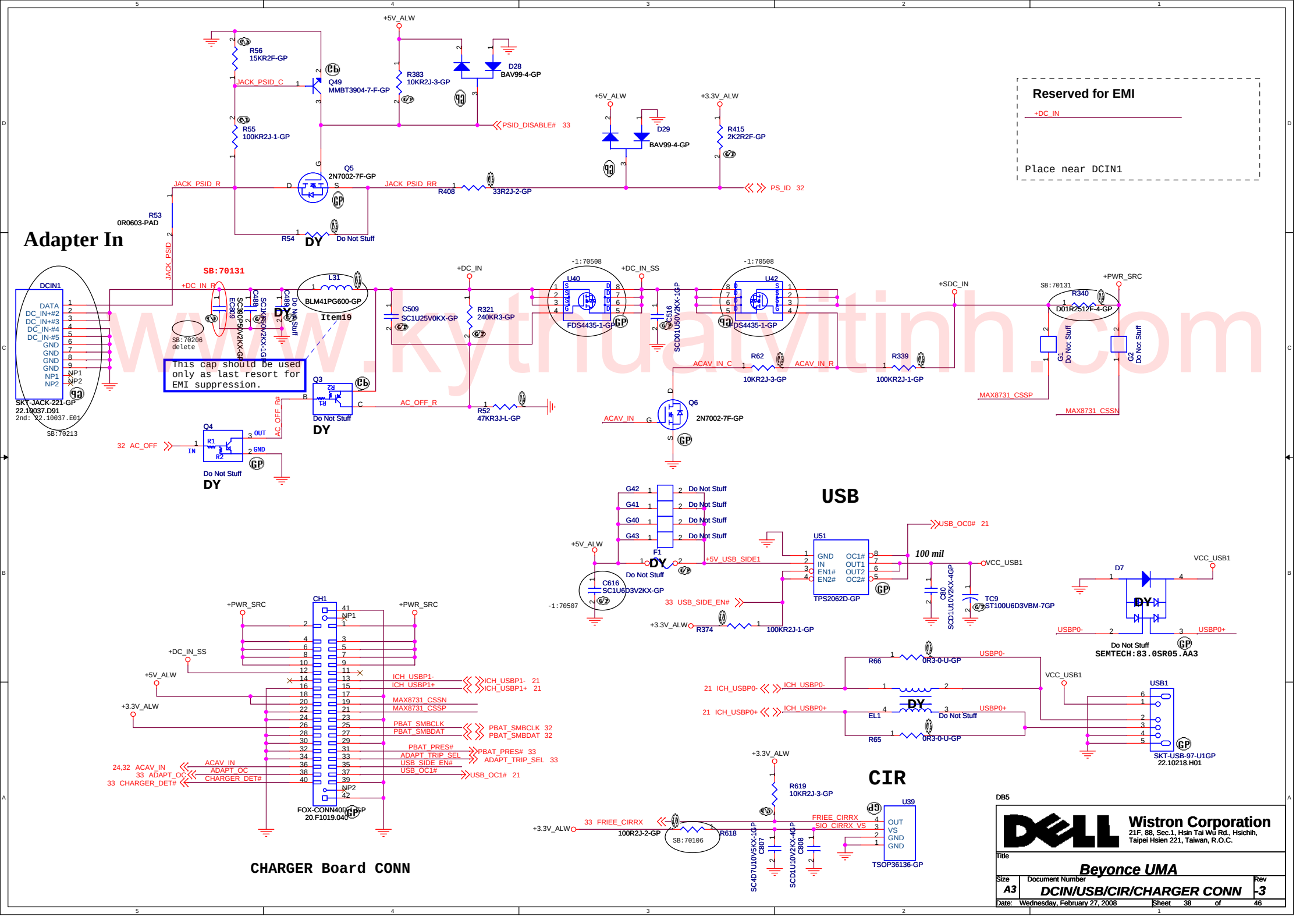
DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA

Size: A3 | Document Number: Power Plane Enable | Rev: -3

Date: Wednesday, February 27, 2008 | Sheet 37 of 46

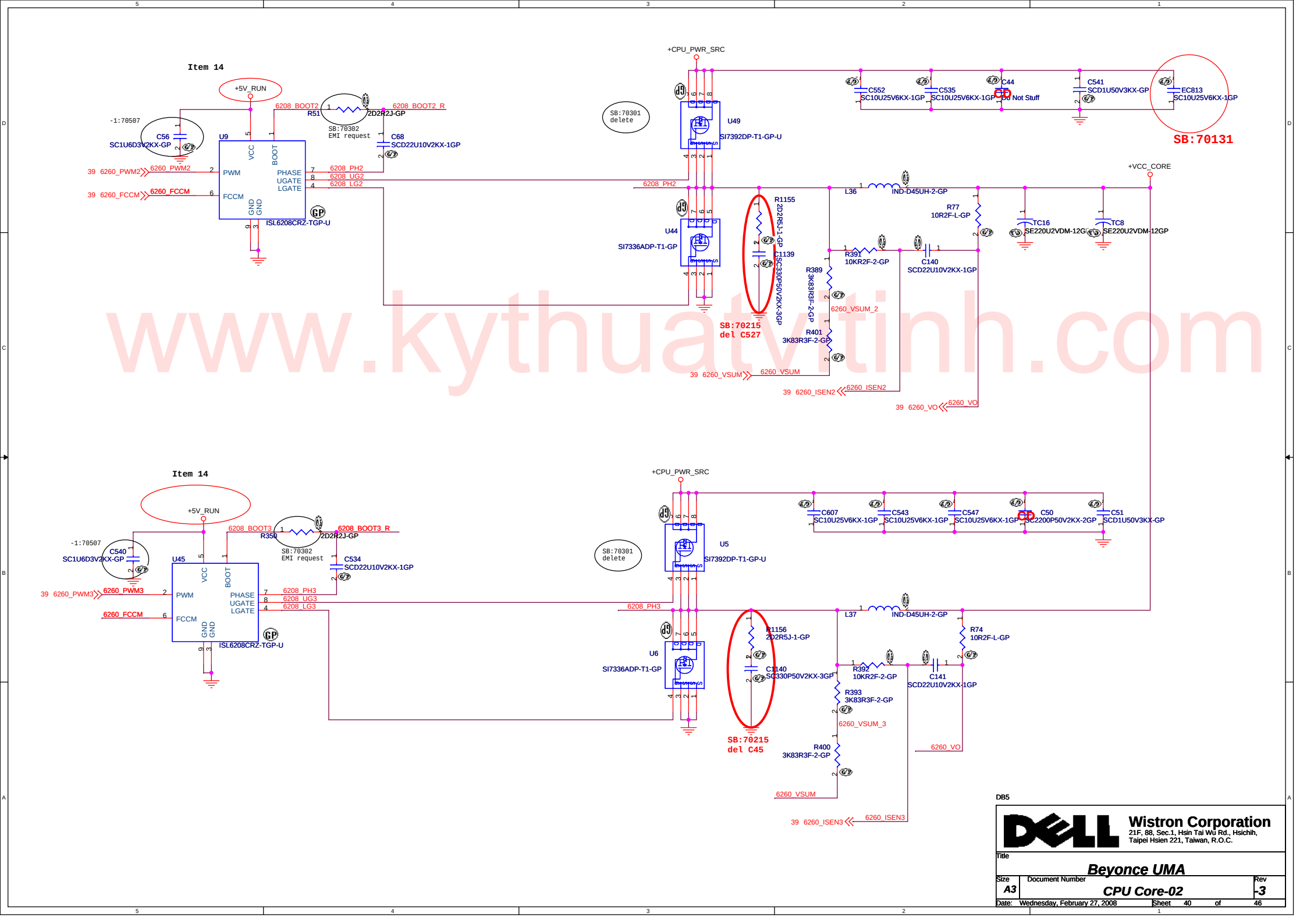


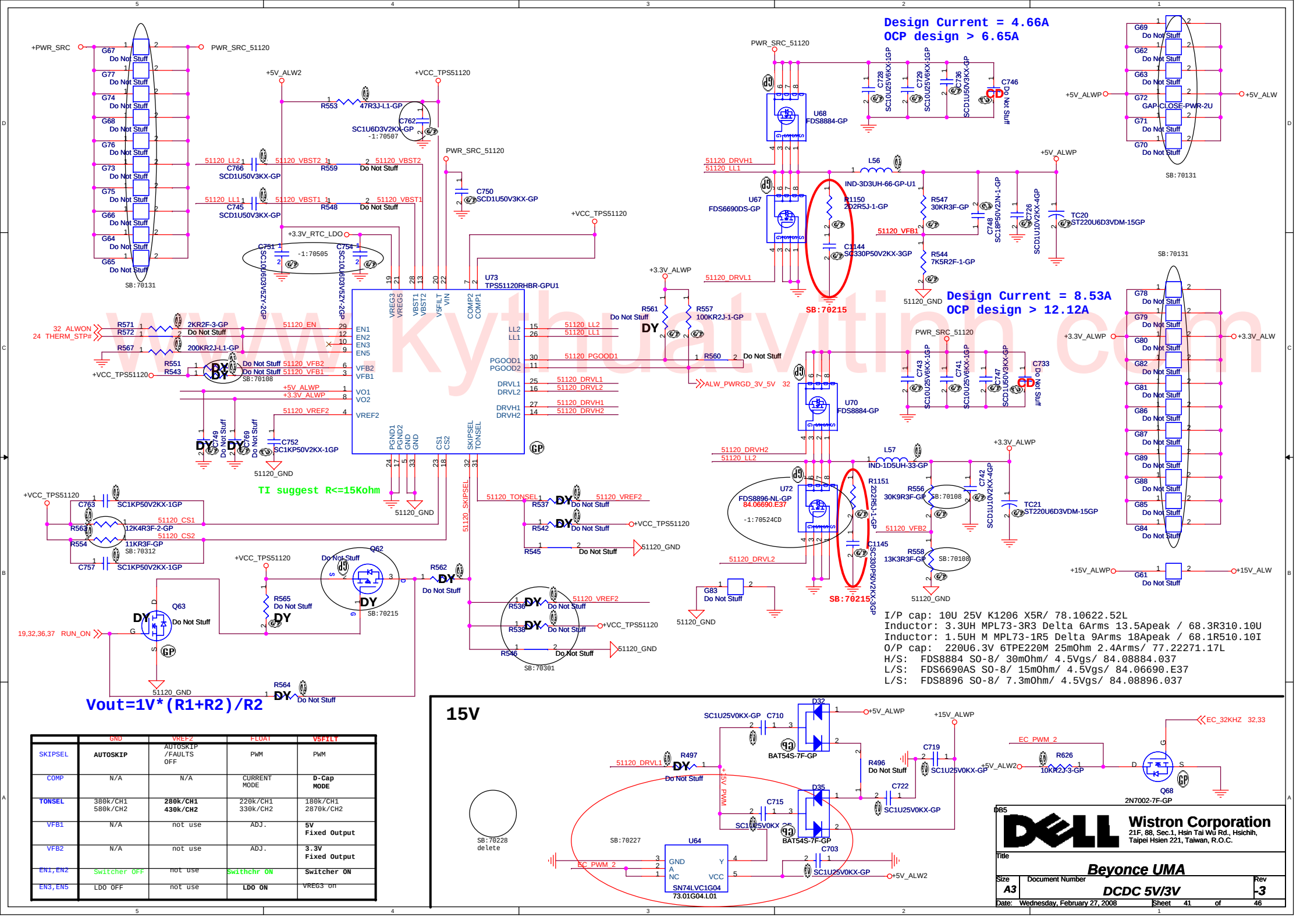
Thermal Design = 35.2A
Peak Current [Ipeak]= 44A
OCP design = 1.2 * Ipeak

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.45UH ETQP4LR45XFC/ 68.R4510.10A
O/P cap: 330U 2V EEFSX0D331XE/ 79.33719.20L
H/S: SI7392DP/ POWERPAK-8/ 16.5mOhm/ 4.5Vgs/ 84.07392.A37
L/S: SI7336ADP/ POWERPAK-8/ 4mOhm/ 4.5Vgs/ 84.07336.B37

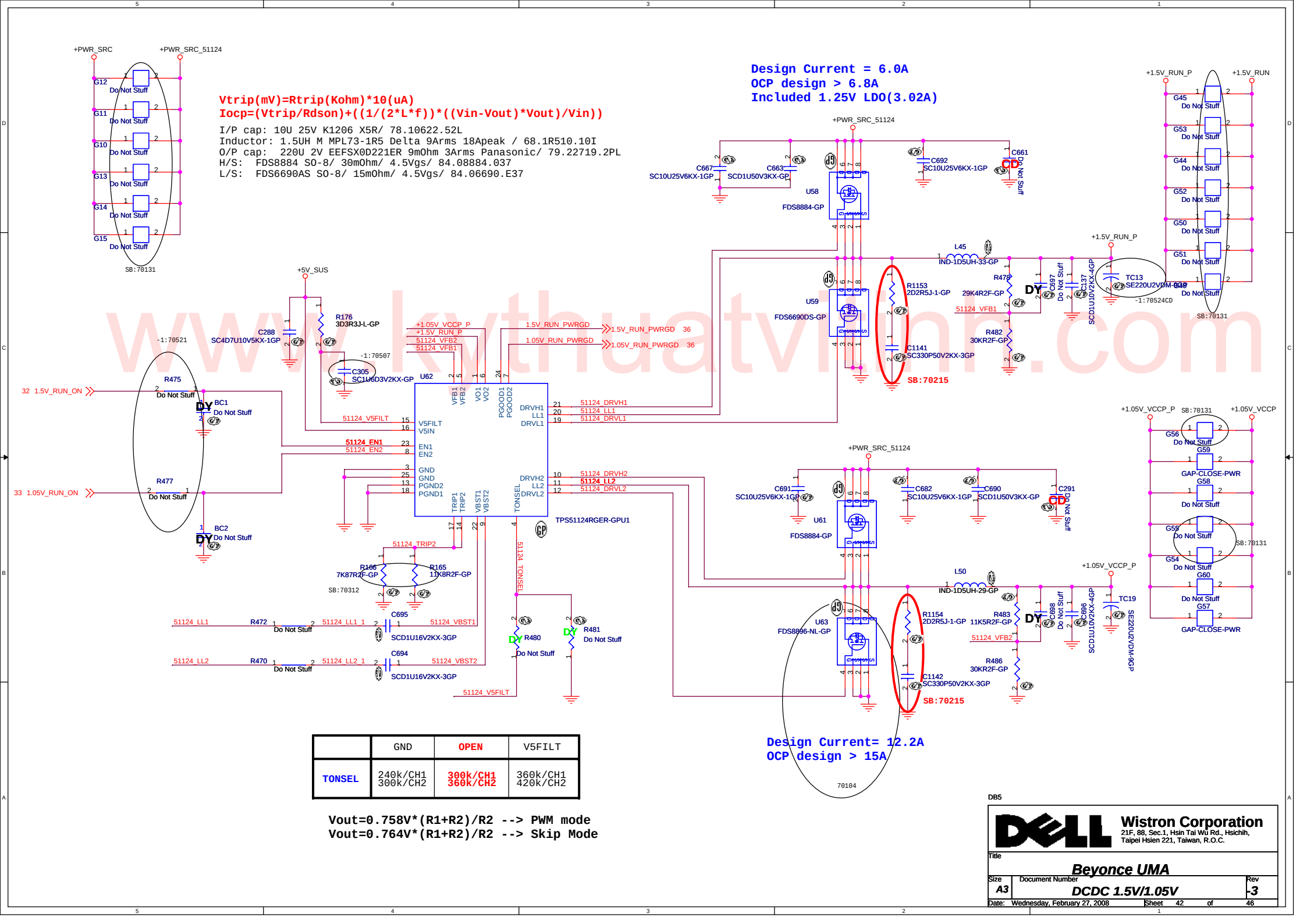
Item 14

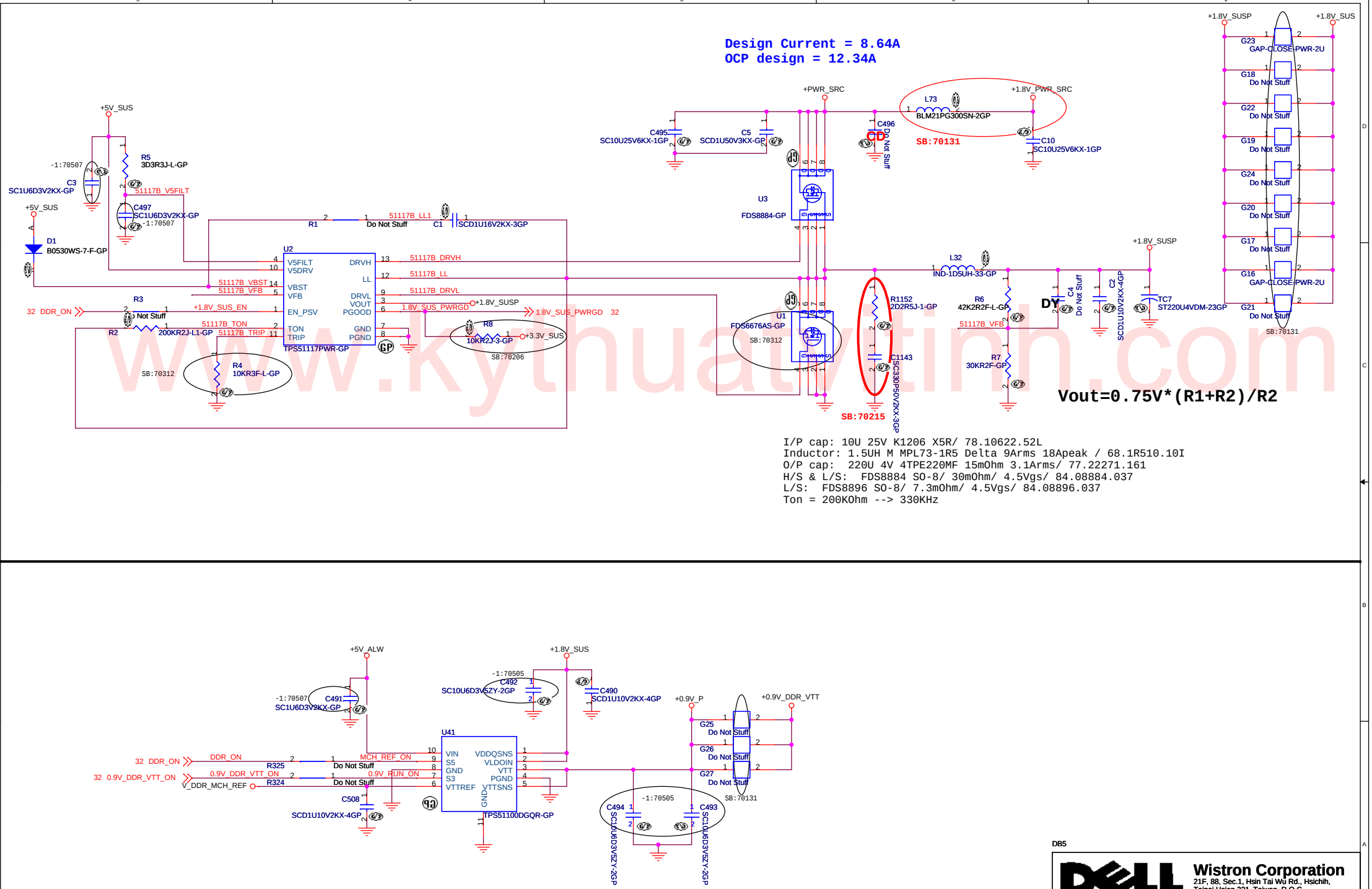
DB5	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Beyonce UMA
Size	A3
Document Number	CPU Core-01
Rev	-3
Date:	Wednesday, February 27, 2008
Sheet	39 of 46





	GND	VREF2	FLOAT	VFILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 580k/CH2	**280k/CH1 430k/CH2**	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on


Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
O/P cap: 220U 2V EEFSX0D221ER 9mOhm 3Arms Panasonic/ 79.22719.2PL
H/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 15mOhm/ 4.5Vgs/ 84.06690.E37
Design Current = 6.0A
OCP design > 6.8A
Included 1.25V LDO(3.02A)
Design Current= 12.2A
OCP design > 15A
TPS51124RGER-GPU1
Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode
GND
OPEN
V5FILT
TONSEL
240k/CH1
300k/CH2
300k/CH1
360k/CH2
360k/CH2
420k/CH2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Beyonce UMA
DCDC 1.5V/1.05V
Wednesday, February 27, 2008



DB5

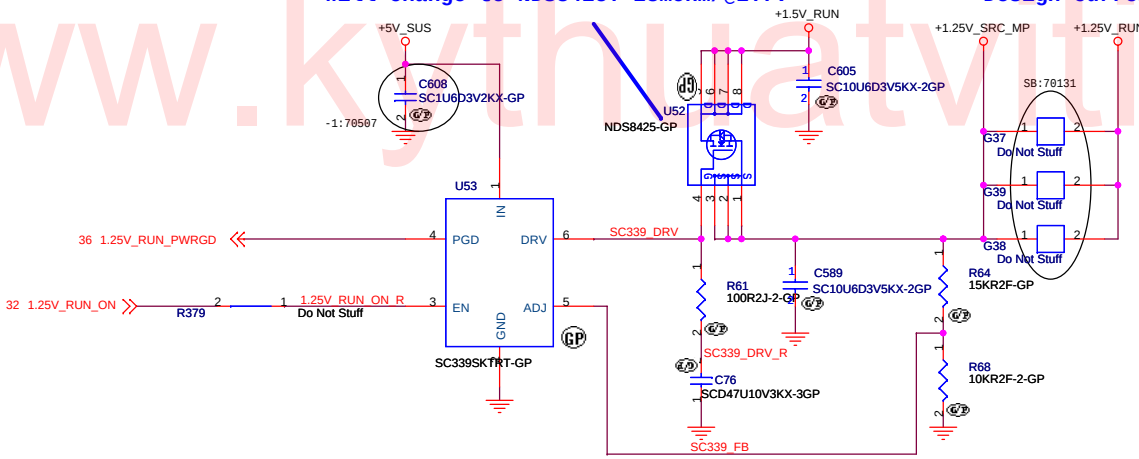
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA

Size	Document Number	Rev
A3	DCDC 1.8V/0.9V	-3

Date: Wednesday, February 27, 2008 Sheet 43 of 46

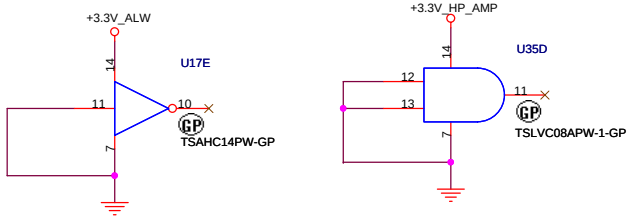
Will Change to NDS8425. 28mOhm/@2.7V **Design Current = 3.0A**

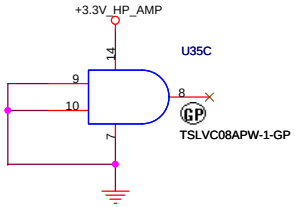


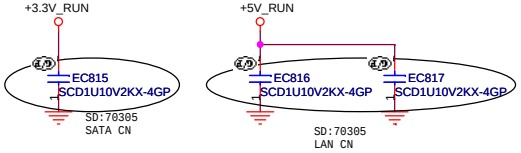
DB5

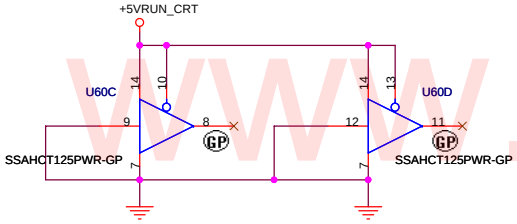
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Beyonce UMA	
Size: A3	Document Number: DCDC 1.25V	Rev: -3
Date: Wednesday, February 27, 2008	Sheet 44 of 46	

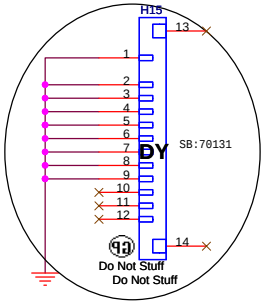


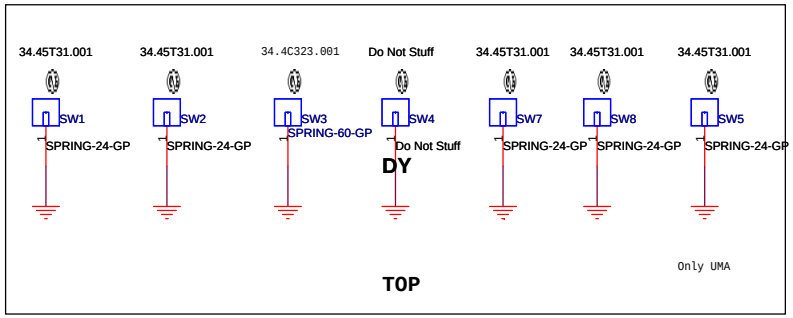


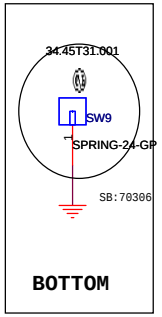


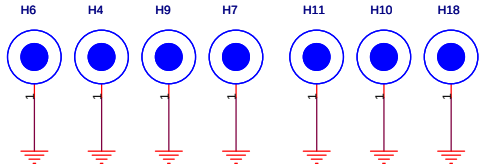


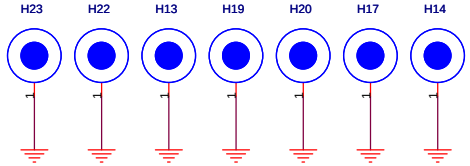
SW3 - 34.43E25.001
SW9 - 34.49Q02.001
SW5 - 34.34T31.001 (Only for UMA)
others-34.45T31.001



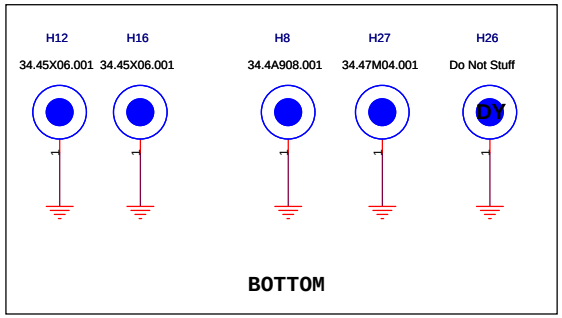


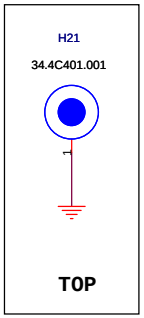






H12, H16: 34.45X06.001
H8: 34.4A908.001
H27: 34.47M04.001
H26: 34.4G901.001
H21: 34.4C401.001





DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA

Size	Document Number	Rev
A3	EMI&MISC	-3

Date: Wednesday, February 27, 2008 Sheet 45 of 46

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
		1				EE
		2				EE
		3				EE
		4				EE
		5				EE
		6				EE
		7				EE
		8				EE
		9				EE
		10				EE
		11				EE
		12				EE
		13				EE
		14				EE
2006/11/24		15				EE
		16				Power team
		17				EE
		18				EE
		19				EE
		20				EE
		22				
		23				
		24				
		25				
		26				

DB5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Beyonce UMA

Size: A3 | Document Number: HISTORY | Rev: -3

Date: Wednesday, February 27, 2008 | Sheet 46 of 46