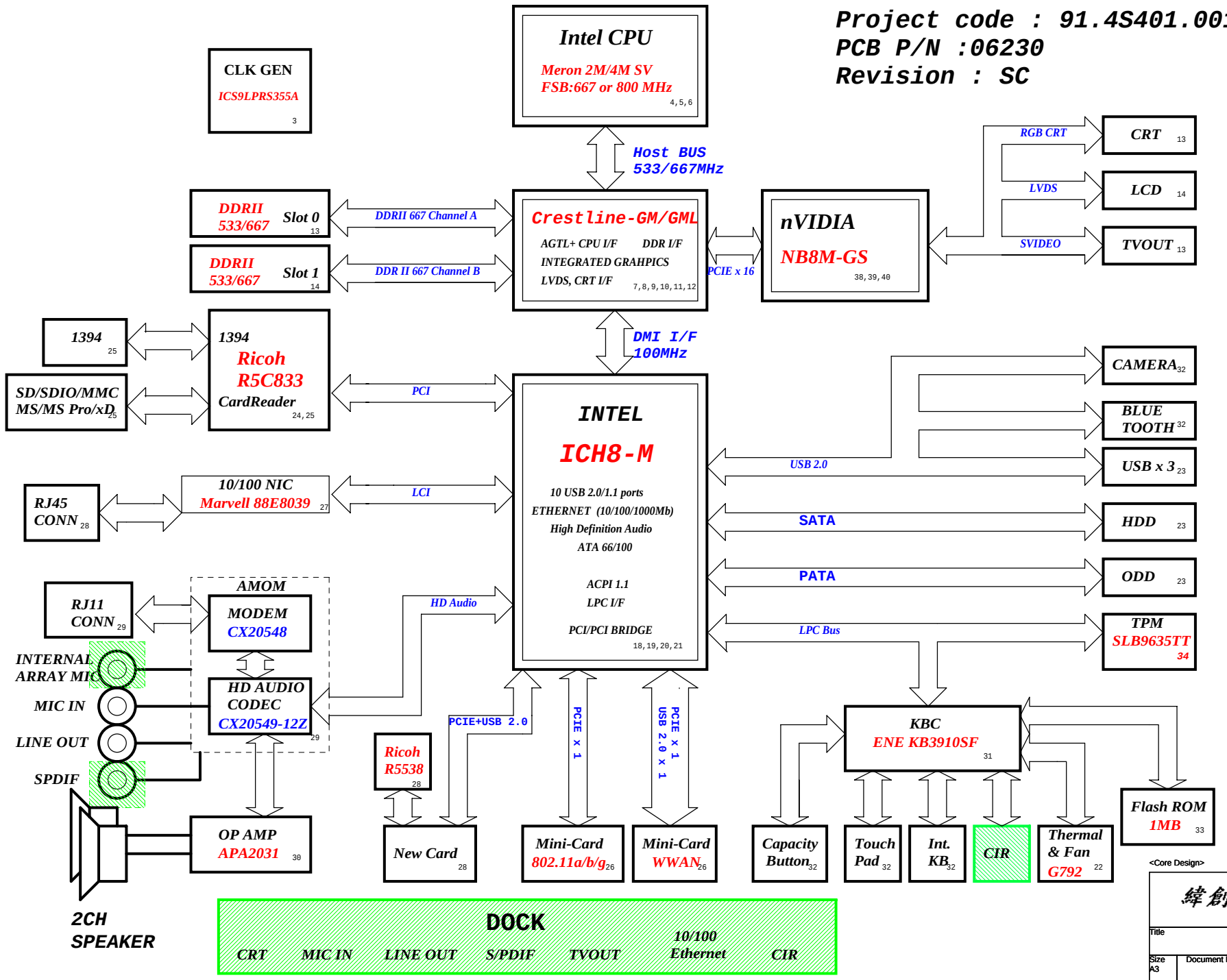
Pamirs-Discrete Block Diagram

Project code : 91.4S401.001
PCB P/N :06230
Revision : SC



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

SYSTEM DC/DC FAN5234	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0 11A

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: GND
L6: VCC
L7: Signal 4
L8: Signal 5
L9: GND
L10: Signal 5

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Title: **Block Diagram**

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INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD	TP3	AZ_DOUT_ICH	Description
0	0	0	RSVD
0	1	1	Enter XOR Chain
1	0	0	Normal Operation(default)
1	1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3: low = A16 swap override enable
high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN: High=Enable Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP: High=Enable Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR: LOW = Defaule
High=No Reboot

8.2K PULL HIGH

19,21 +RTCVCC → +RTCVCC
4,5,6,7,9,10,11,19,21,37,47 1D05V_S0 → 1D05V_S0
3,7,10,21,38 1D25V_S0 → 1D25V_S0
27 1D2V_LAN_S5 → 1D2V_LAN_S5
28 1D5V_NEW_S0 → 1D5V_NEW_S0
5,10,17,19,20,21,26,28,38,47 1D5V_S0 → 1D5V_S0
7,10,11,13,14,34,37,38 1D8V_S3 → 1D8V_S3
27,28 2D5V_LAN_S5 → 2D5V_LAN_S5
29,30 3D3V_AUD_S0 → 3D3V_AUD_S0
19,31,32,33,36,39,46 3D3V_AUX_S5 → 3D3V_AUX_S5
27,28 3D3V_LAN_S5 → 3D3V_LAN_S5
3,4,7,10,11,13,14,15,16,18,19,20,21,22,23,24,25,26,27,28,29,31,32,33,34,35,36,40,41,42,43,47 3D3V_S0 → 3D3V_S0
17,18,20,21,22,26,27,28,29,31,34,36,39,47 3D3V_S5 → 3D3V_S5
22,26,29,31,34,36 5V_AUX_S5 → 5V_AUX_S5
16,23,32,33,34,36,37,38 5V_S3 → 5V_S3
15,16,17,20,21,22,23,29,30,31,32,33,34,35,47 5V_S0 → 5V_S0
16,21,34,37,40 5V_S5 → 5V_S5
17,39,46,47 AD+ → AD+
16,17,34,35,36,37,39,40,47 DCBATOUT → DCBATOUT
13,14,38 DDR_VREF_S0 → DDR_VREF_S0
7,13,14,38 DDR_VREF_S3 → DDR_VREF_S3
22,31,33,39 KBC_3D3V_AUX → KBC_3D3V_AUX
16 LCDVDD_S0 → LCDVDD_S0
5,6,35 VCC_CORE_S0 → VCC_CORE_S0

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

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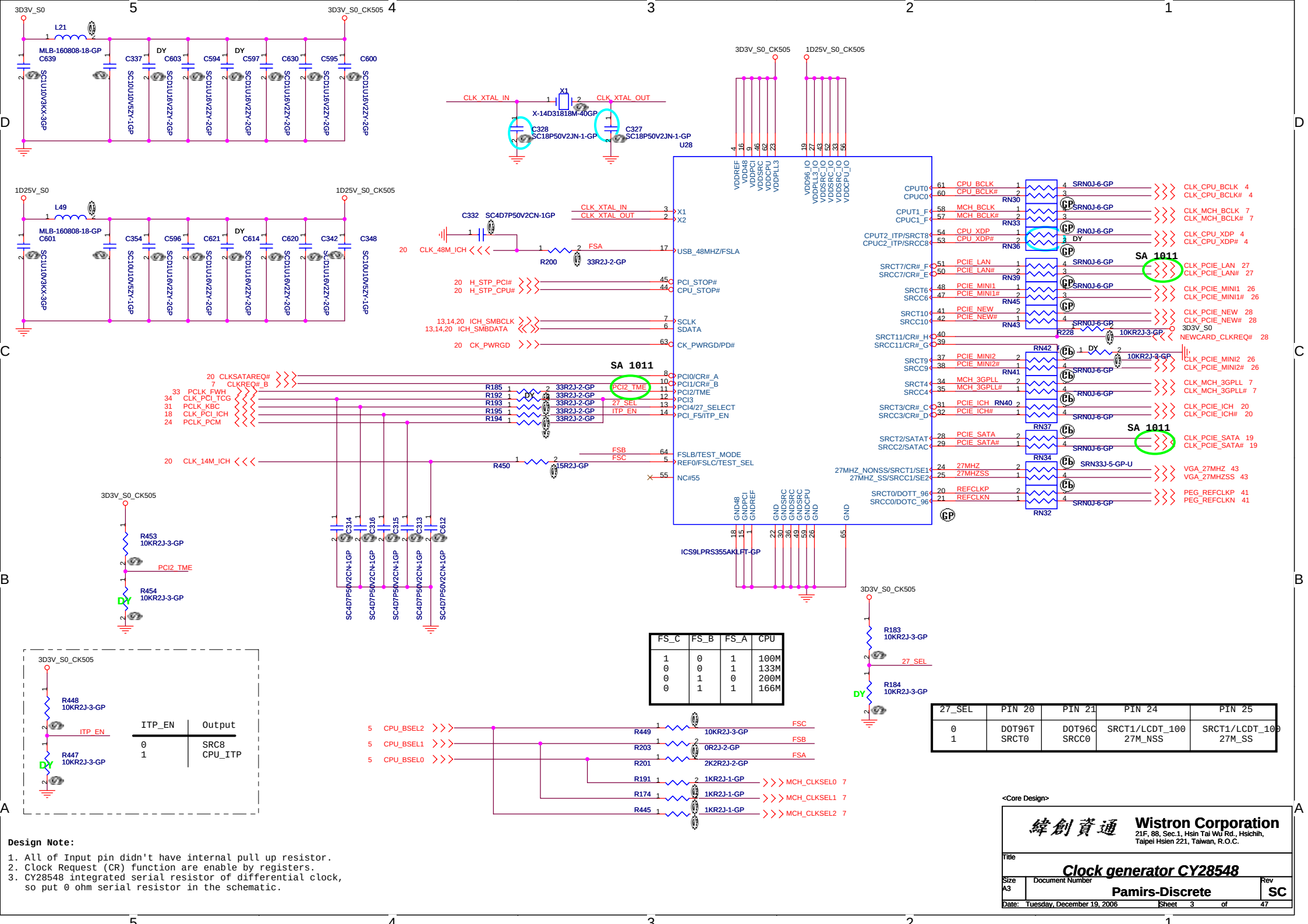


ITP_EN	Output
0	SRC8
1	CPU_ITP

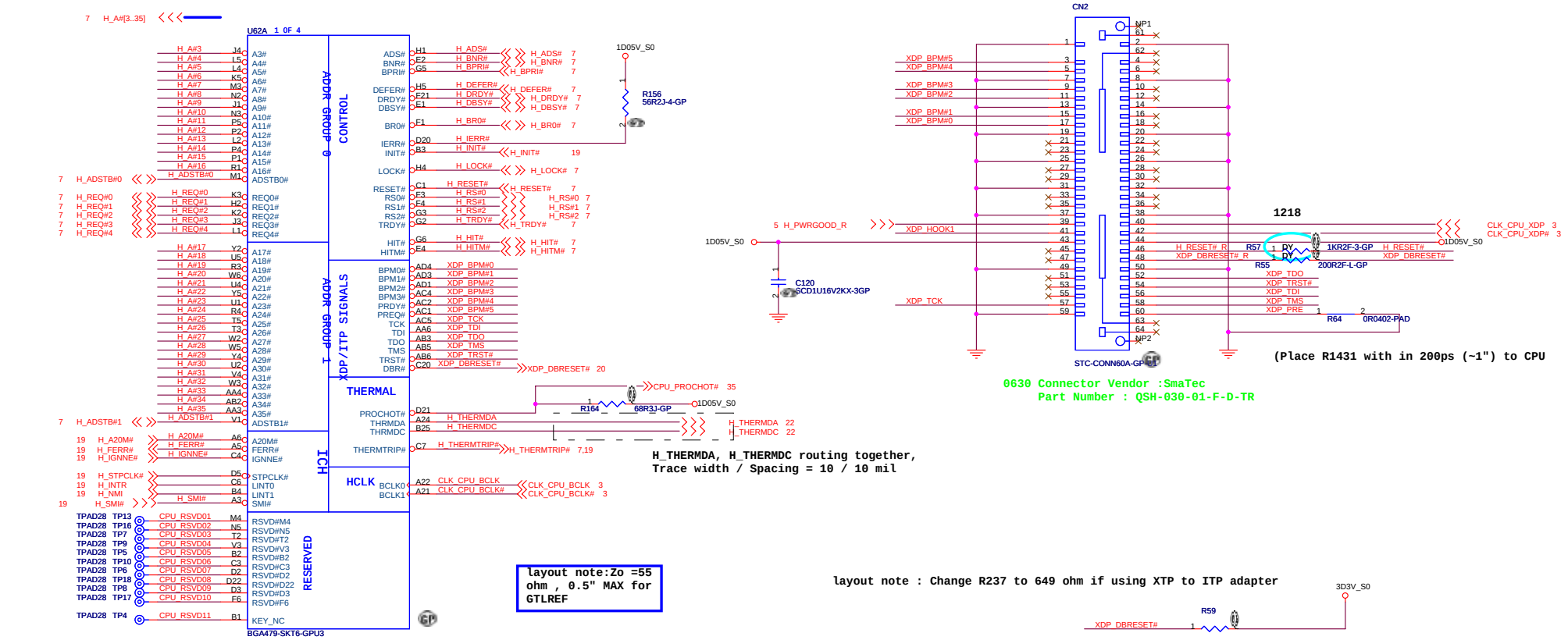
FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1	SRCT0	SRCC0	27M_NSS	27M_SS

Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

XDP Connector



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Title: Meron(1/3)-AGTL+/XDP

Size: Custom | Document Number: Pamirs-Discrete | Rev: SC

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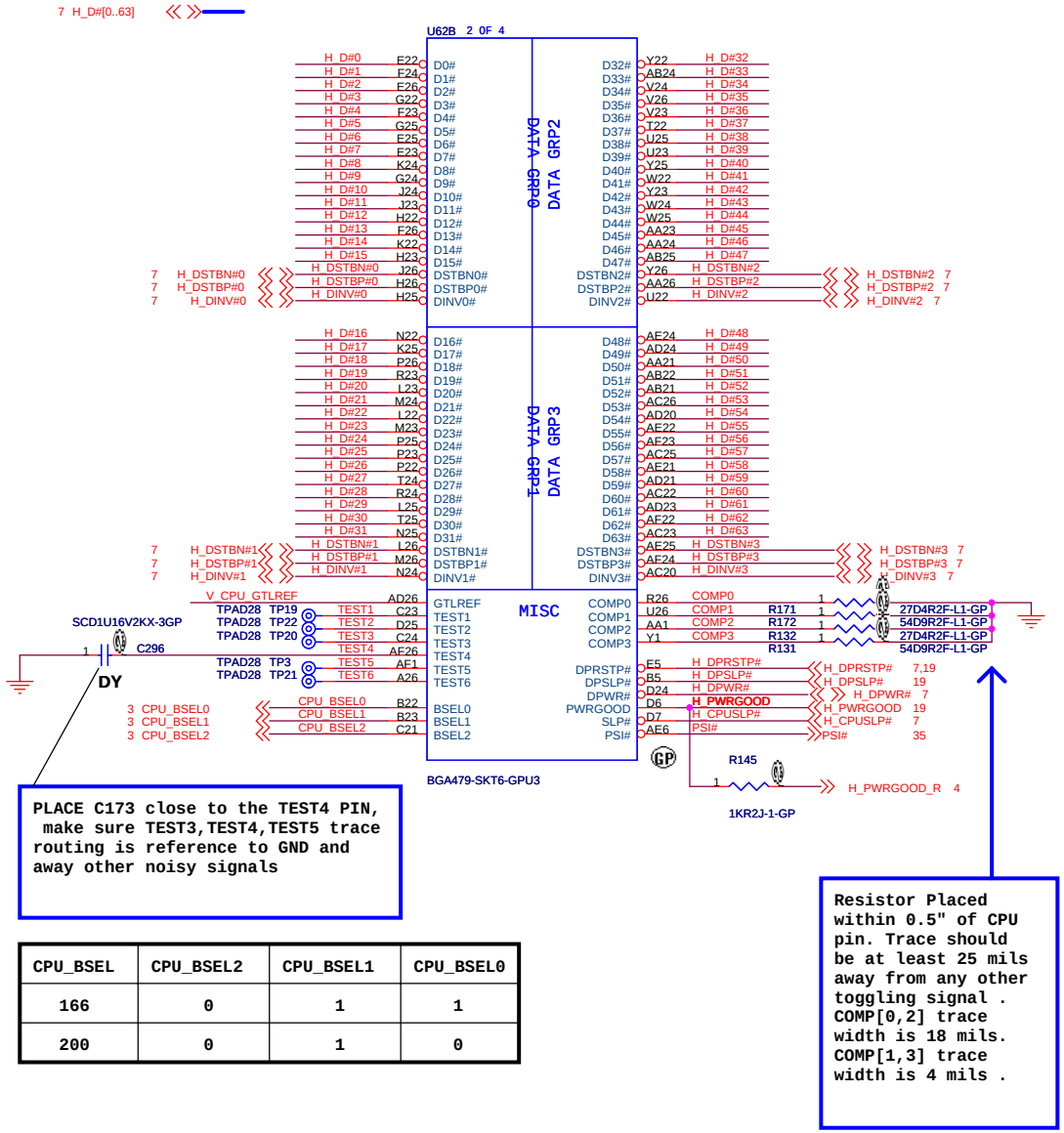
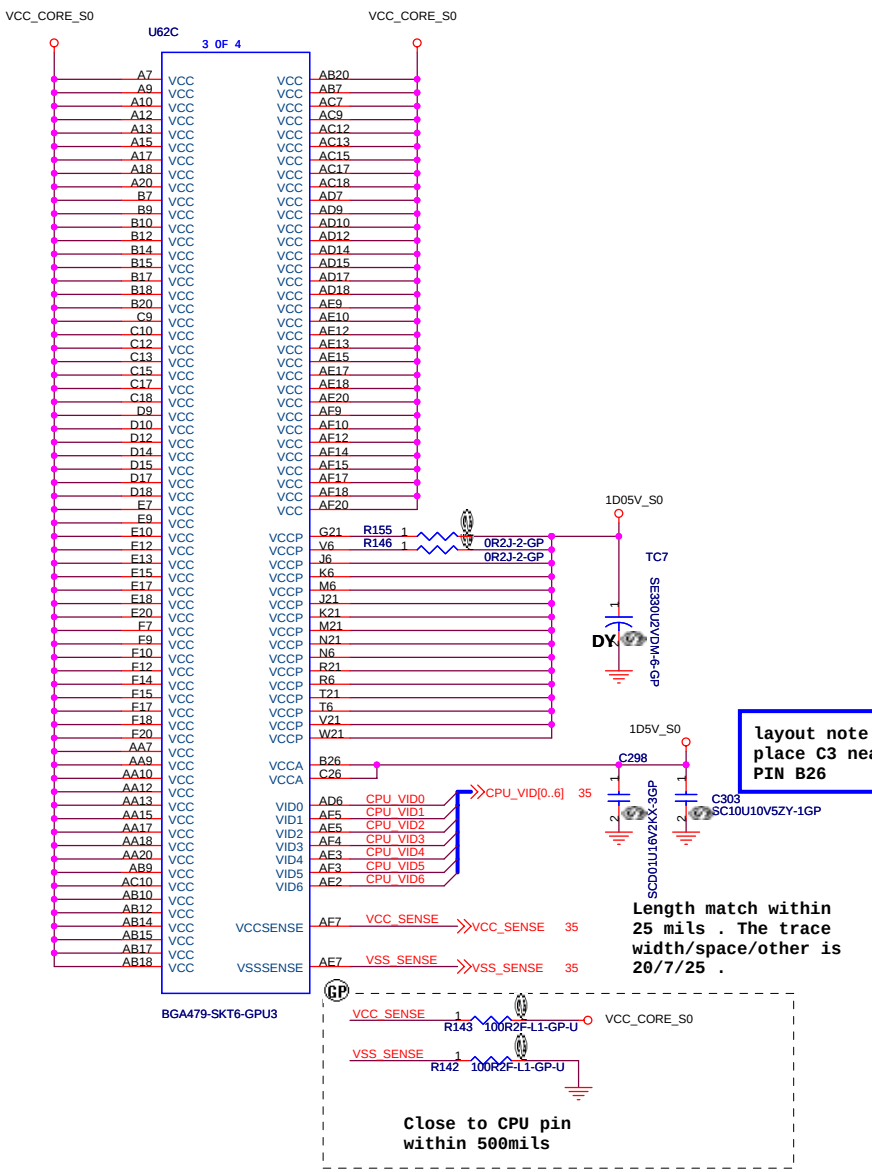




CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

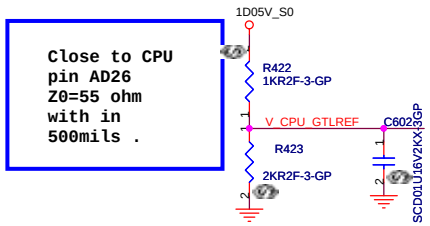
PLACE C173 close to the TEST4 PIN, make sure TEST3,TEST4,TEST5 trace routing is reference to GND and away other noisy signals

Resistor Placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal . COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils .

layout note: place C3 near PIN B26

Length match within 25 mils . The trace width/space/other is 20/7/25 .

Close to CPU pin within 500mils



Close to CPU pin AD26 Z0=55 ohm with in 500mils .

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Title: Meron(2/3)-AGTL+/PWR

Size: A3 | Document Number: Pamirs-Discrete | Rev: SC

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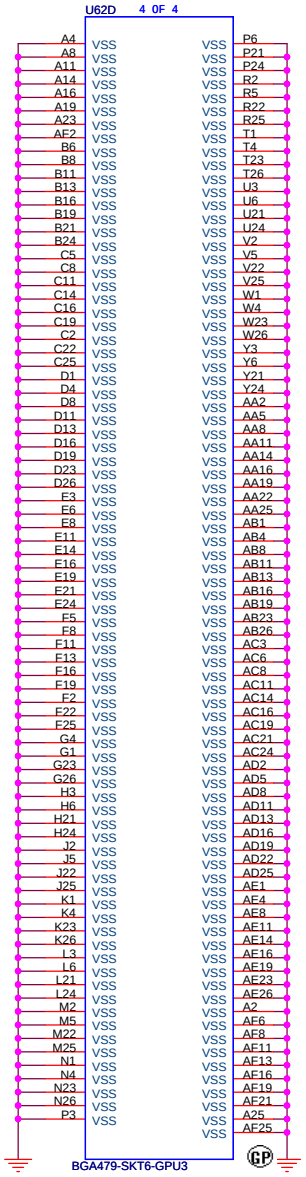
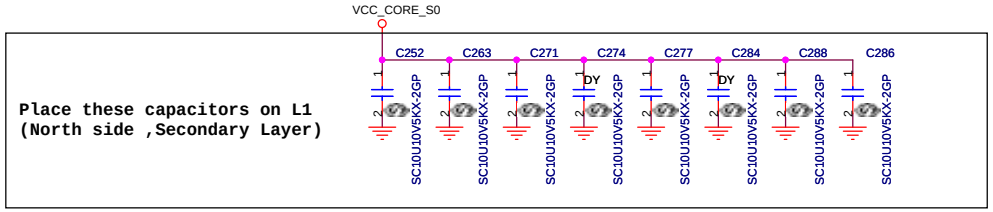
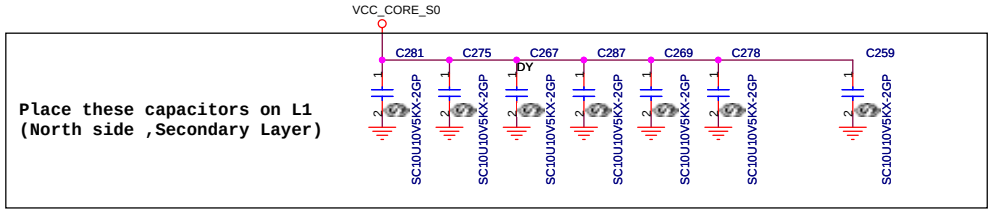
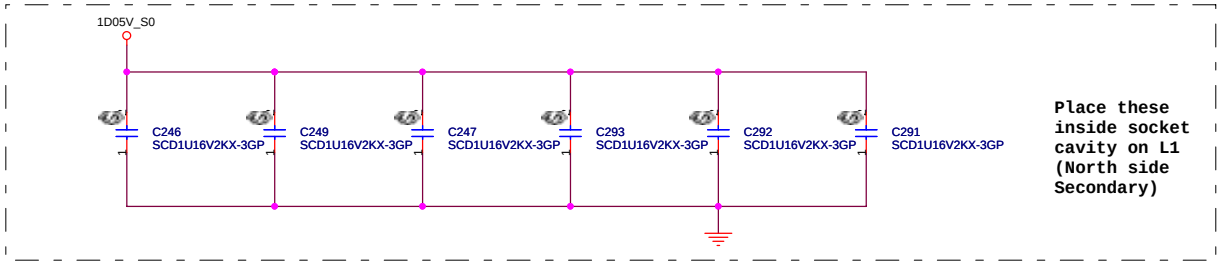






Mid Frequencd Decoupling



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Title: Meron(3/3)-GND&Bypass

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FOR Calero: 80.6 ohm
Crestline: 20 ohm

layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

Layout Note :
Place C151 within 100 mils of NB

Layout Note :
Place C153 near pin B3 of NB

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

From Astro demo schematic

SA 0928

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Title: CRESTLINE(1/6)-AGTL+/DMI/DDR2

Size: Custom | Document Number: Pamirs-Discrete | Rev: SA

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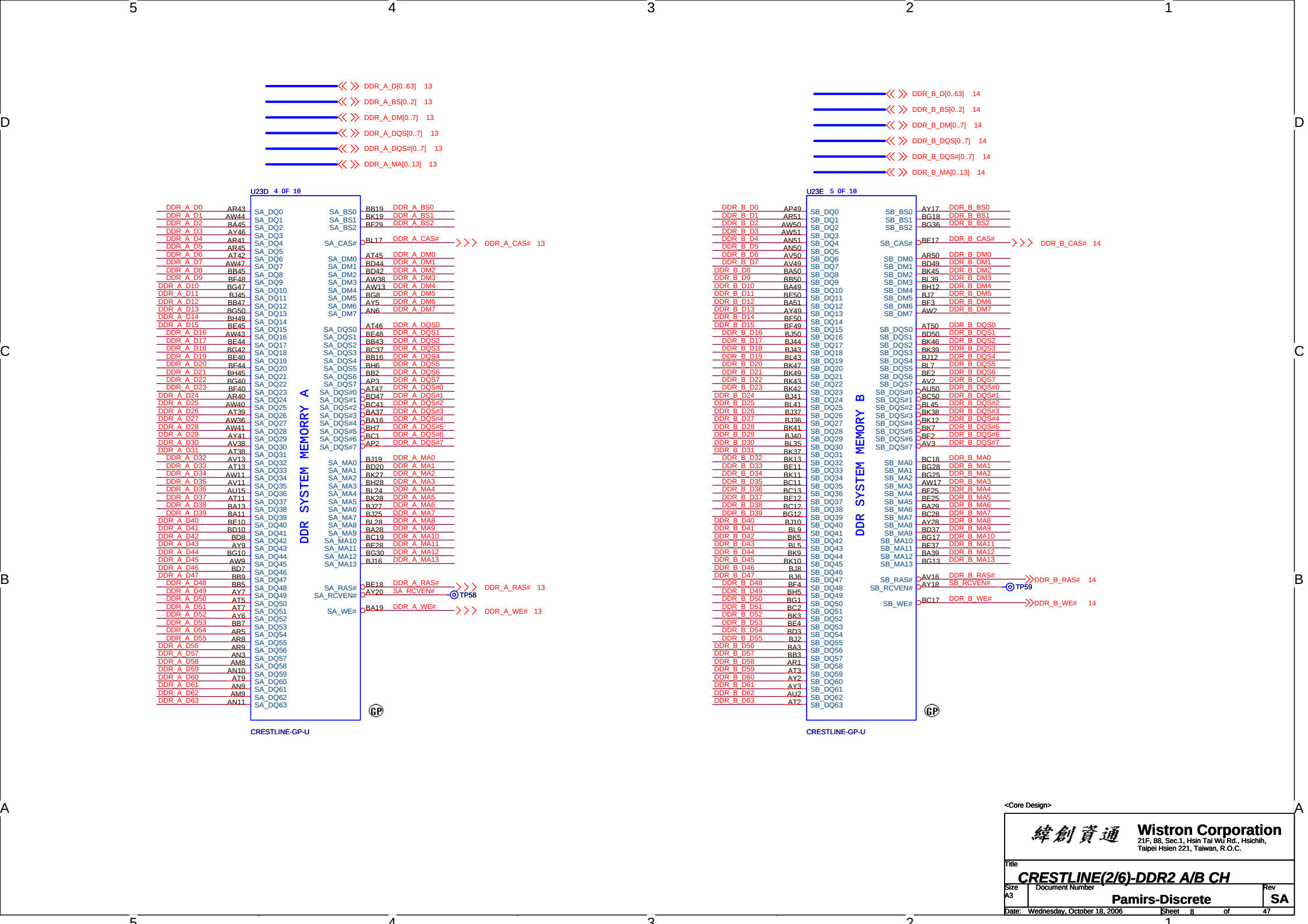

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Title: CRESTLINE(2/6)-DDR2 A/B CH

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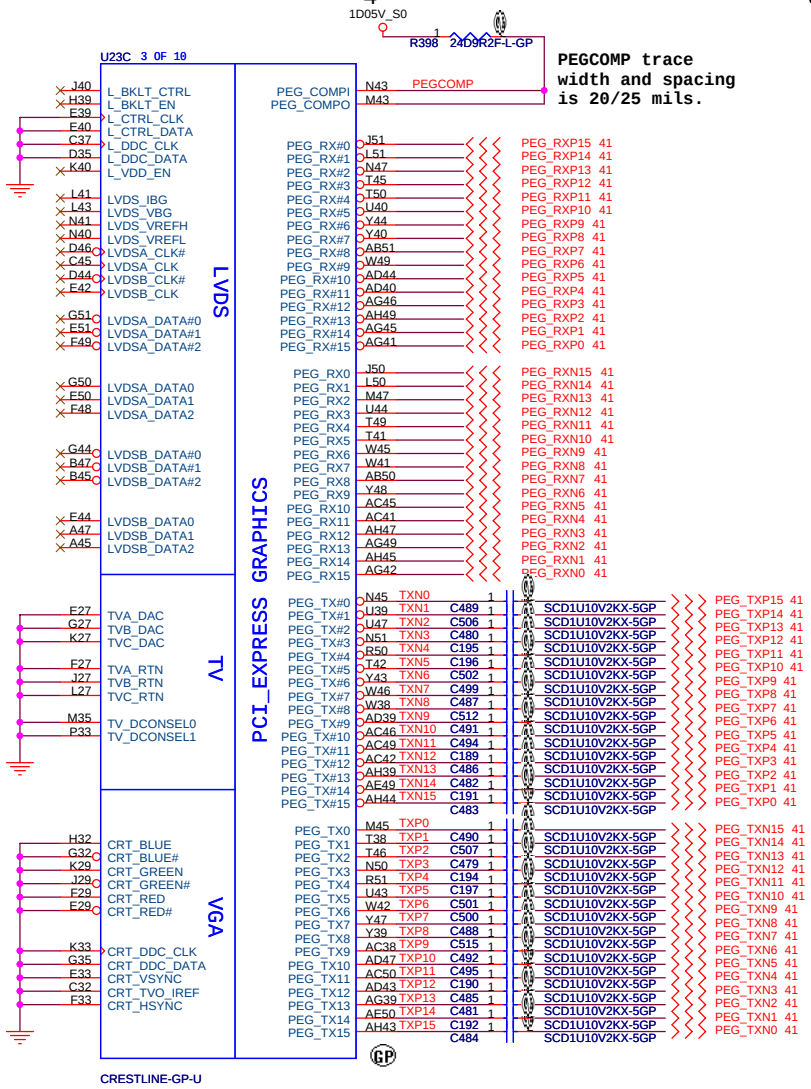

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

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Title: CRESTLINE(3/6)-VGA/LVDS/TV

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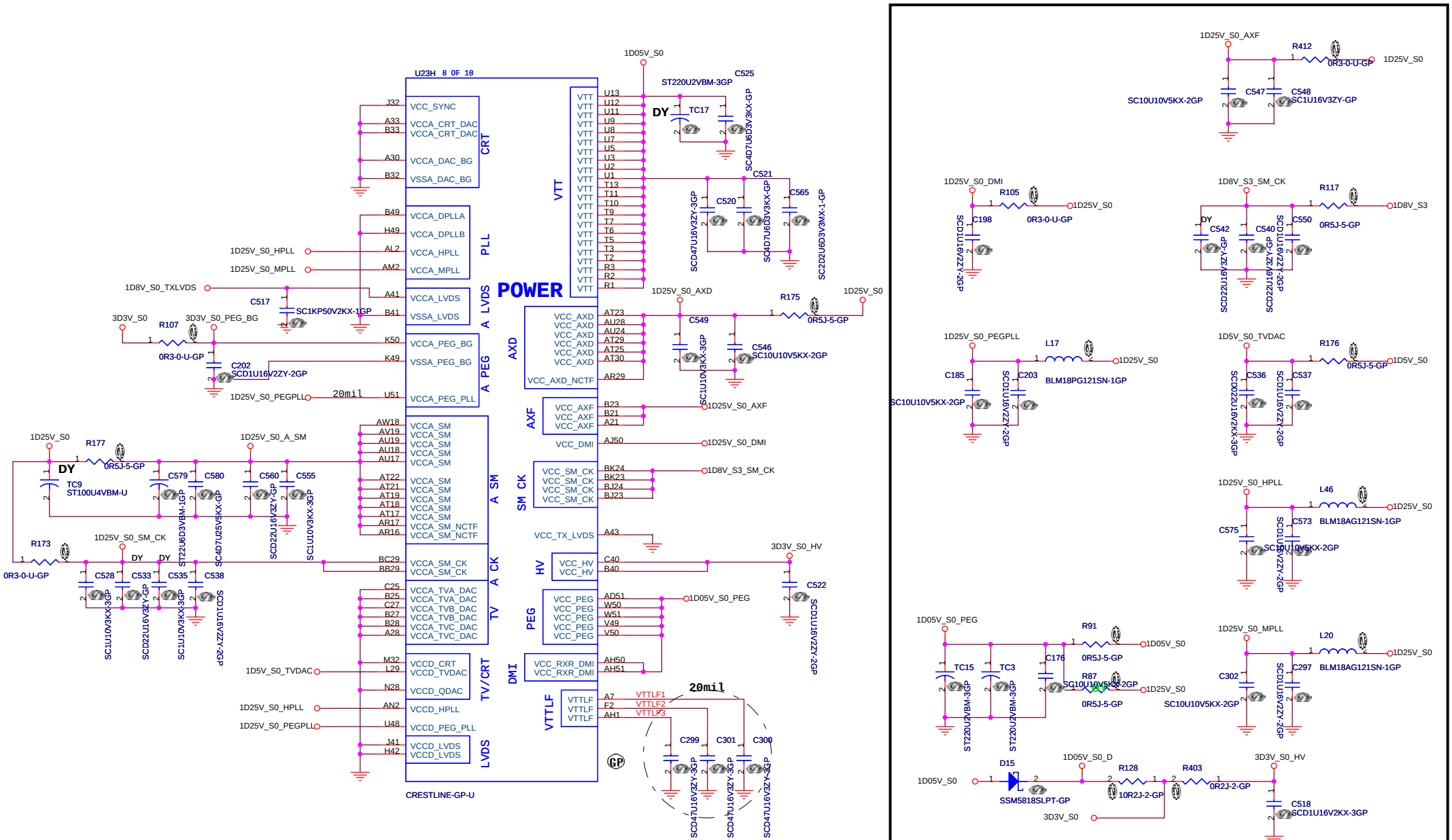

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Title: CRESTLINE(4/6)-PWR

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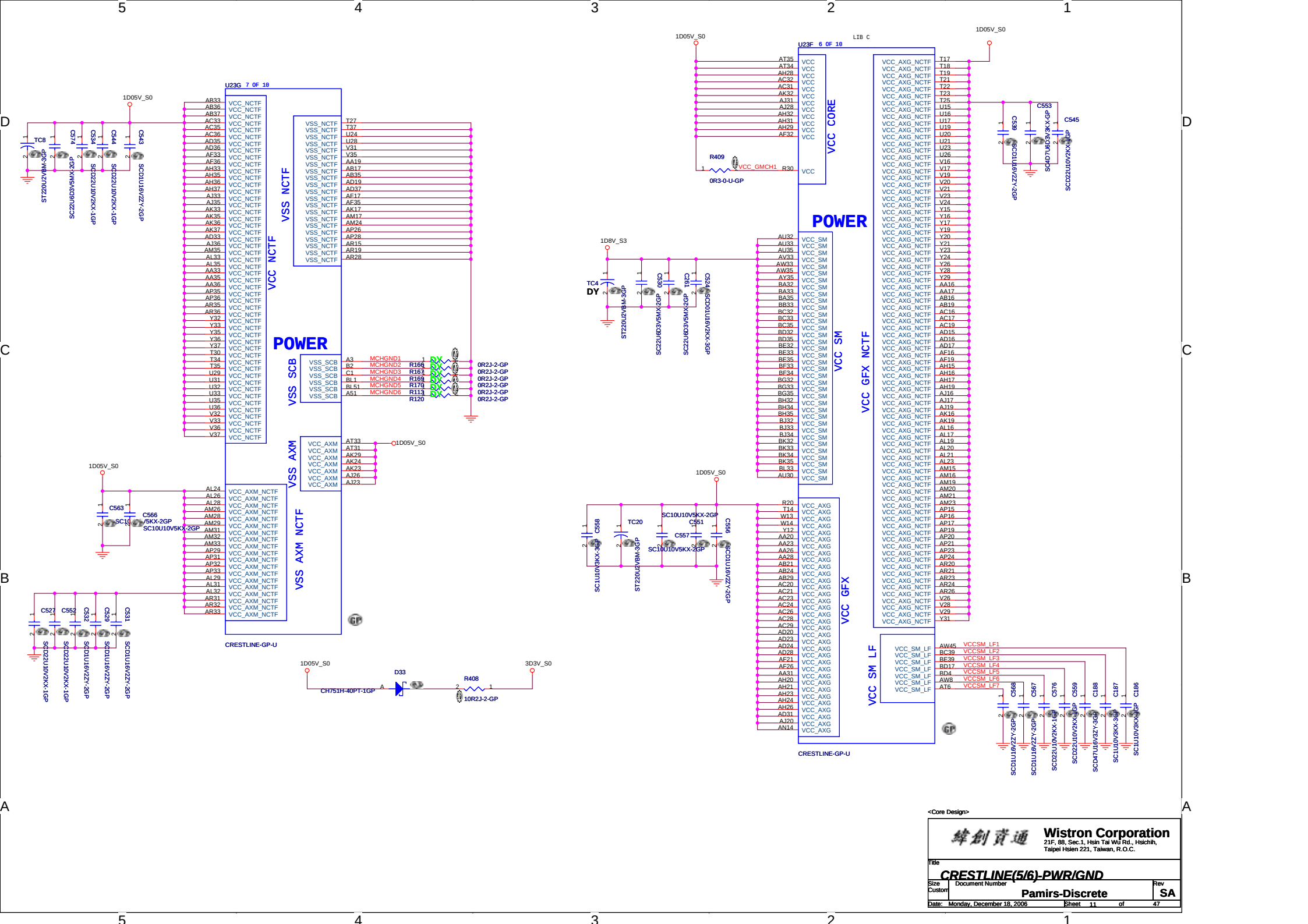
U23G 7 OF 10
U23F 6 OF 10
LIB C
POWER
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
VCC NCTF
VSS NCTF
VSS SCB
VSS AXM
VSS AXM NCTF
1D05V_S0
1D8V_S3
3D3V_S0
R409
0R3-0-U-GP
VCC_GMCH1
D33
CH751H-40PT-1GP
R408
10R2J-2-GP
CRESTLINE-GP-U
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Title
CRESTLINE(5/6)-PWR/GND
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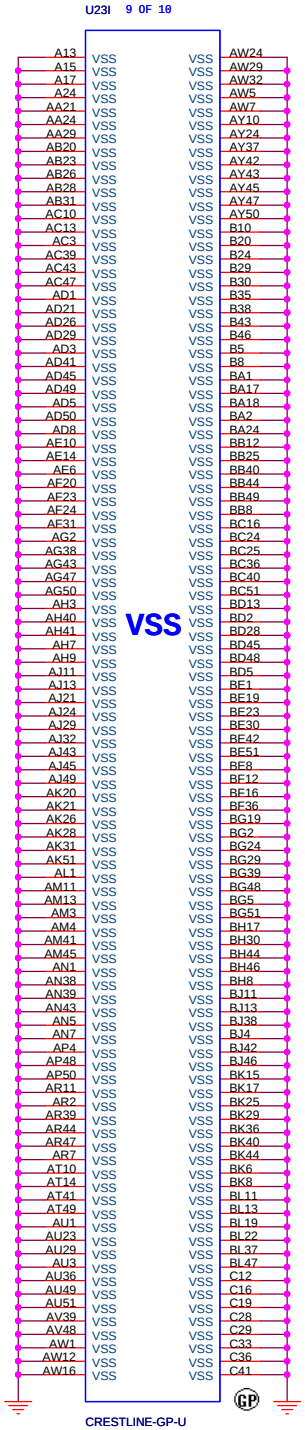

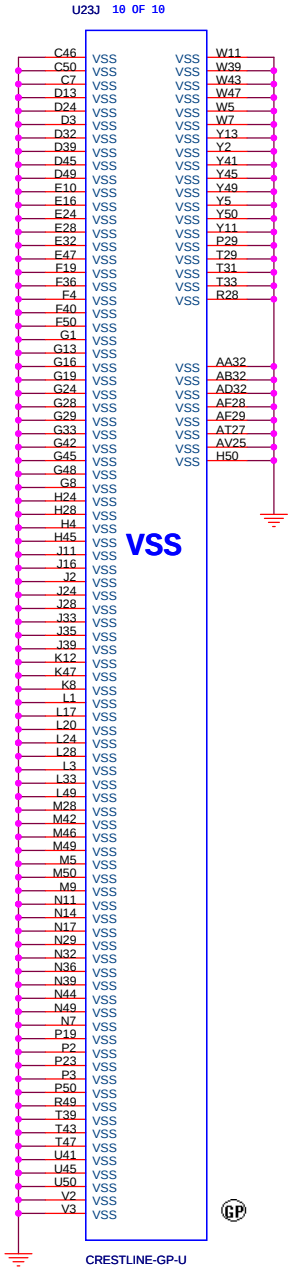

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Title: CRESTLINE(6/6)-PWR/GND

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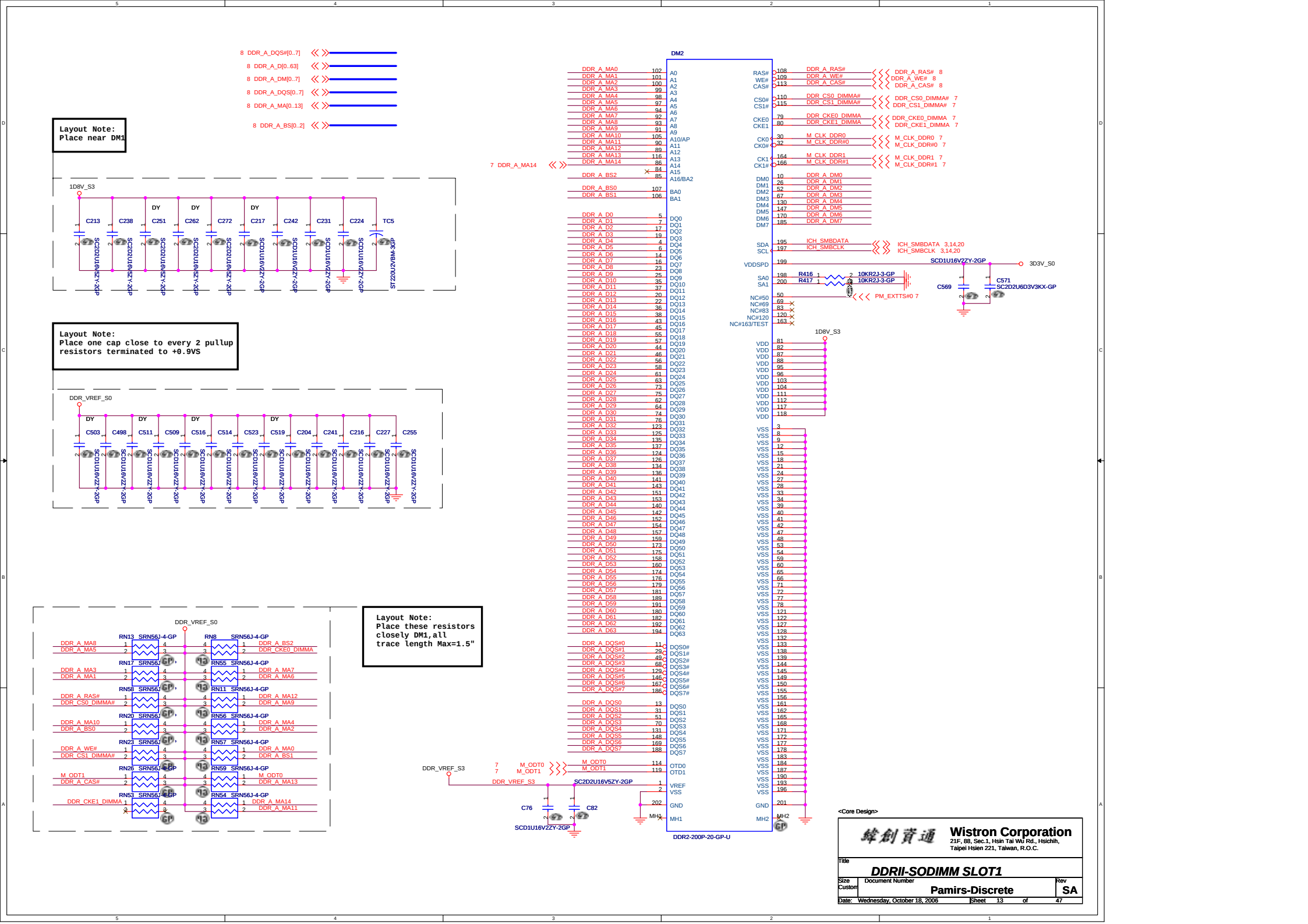
8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]
8 DDR_A_BS[0..2]
Layout Note:
Place near DM1
1D8V_S3
C213
C238
C251
C262
C272
C217
C242
C231
C224
TC5
DY
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C503
C498
C511
C509
C516
C514
C523
C519
C204
C241
C216
C227
C255
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
RN13 SRN56J-4-GP
RN8 SRN56J-4-GP
RN17 SRN56J-4-GP
RN55 SRN56J-4-GP
RN58 SRN56J-4-GP
RN11 SRN56J-4-GP
RN20 SRN56J-4-GP
RN56 SRN56J-4-GP
RN23 SRN56J-4-GP
RN57 SRN56J-4-GP
RN26 SRN56J-4-GP
RN59 SRN56J-4-GP
RN53 SRN56J-4-GP
RN54 SRN56J-4-GP
DDR_A_MA8
DDR_A_MA5
DDR_A_MA3
DDR_A_MA1
DDR_A_RAS#
DDR_CS0_DIMMA#
DDR_A_MA10
DDR_A_BS0
DDR_A_WE#
DDR_CS1_DIMMA#
M_ODT1
DDR_A_CAS#
DDR_CKE1_DIMMA
DDR_A_BS2
DDR_CKE0_DIMMA
DDR_A_MA7
DDR_A_MA6
DDR_A_MA12
DDR_A_MA9
DDR_A_MA4
DDR_A_MA2
DDR_A_MA0
DDR_A_BS1
M_ODT0
DDR_A_MA13
DDR_A_MA14
DDR_A_MA11
DM2
DDR_A_MA0
DDR_A_MA1
DDR_A_MA2
DDR_A_MA3
DDR_A_MA4
DDR_A_MA5
DDR_A_MA6
DDR_A_MA7
DDR_A_MA8
DDR_A_MA9
DDR_A_MA10
DDR_A_MA11
DDR_A_MA12
DDR_A_MA13
DDR_A_MA14
DDR_A_BS2
DDR_A_BS0
DDR_A_BS1
DDR_A_D0
DDR_A_D1
DDR_A_D2
DDR_A_D3
DDR_A_D4
DDR_A_D5
DDR_A_D6
DDR_A_D7
DDR_A_D8
DDR_A_D9
DDR_A_D10
DDR_A_D11
DDR_A_D12
DDR_A_D13
DDR_A_D14
DDR_A_D15
DDR_A_D16
DDR_A_D17
DDR_A_D18
DDR_A_D19
DDR_A_D20
DDR_A_D21
DDR_A_D22
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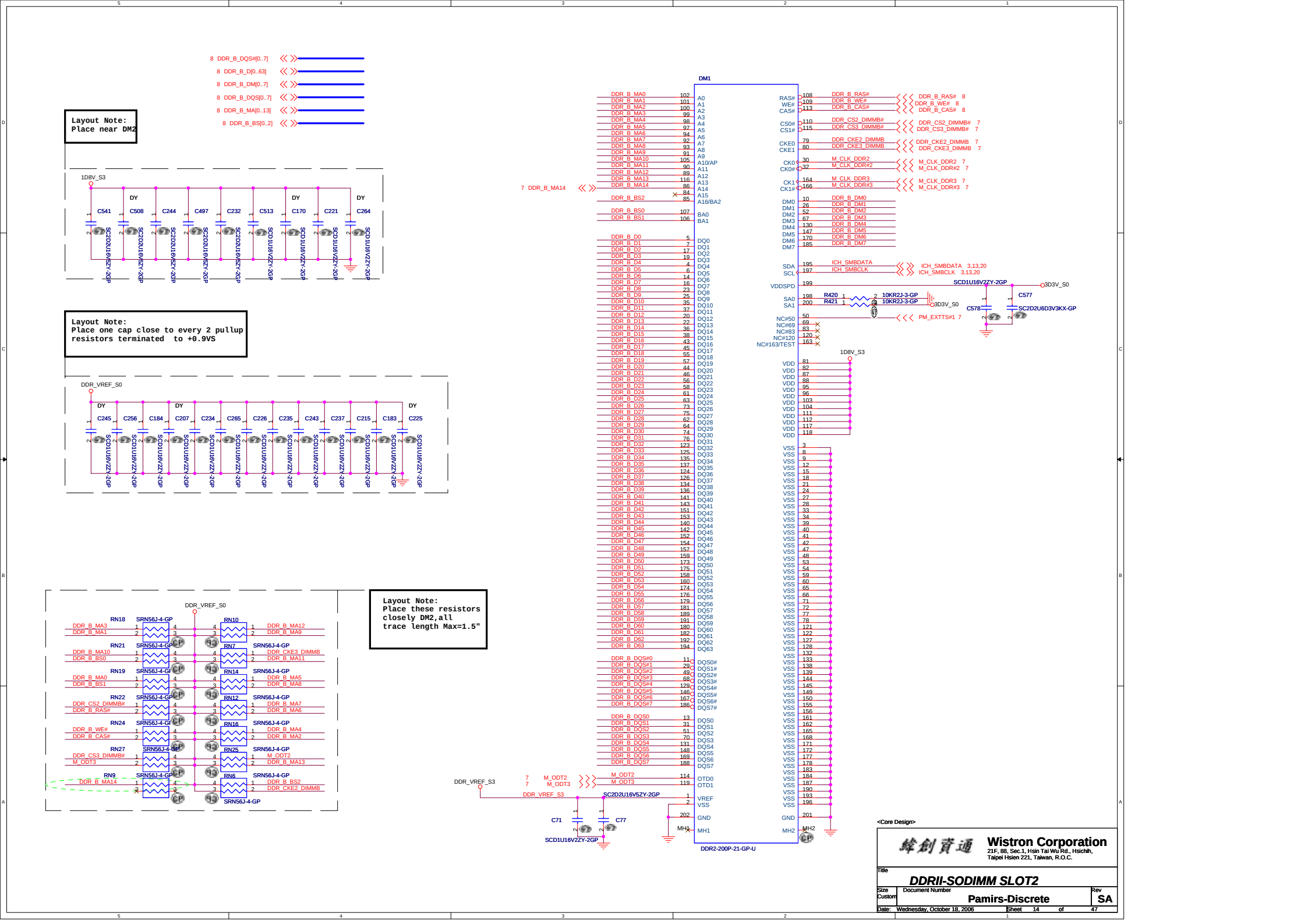
DDR_A_D33
DDR_A_D34
DDR_A_D35
DDR_A_D36
DDR_A_D37
DDR_A_D38
DDR_A_D39
DDR_A_D40
DDR_A_D41
DDR_A_D42
DDR_A_D43
DDR_A_D44
DDR_A_D45
DDR_A_D46
DDR_A_D47
DDR_A_D48
DDR_A_D49
DDR_A_D50
DDR_A_D51
DDR_A_D52
DDR_A_D53
DDR_A_D54
DDR_A_D55
DDR_A_D56
DDR_A_D57
DDR_A_D58
DDR_A_D59
DDR_A_D60
DDR_A_D61
DDR_A_D62
DDR_A_D63
DDR_A_DQS#0
DDR_A_DQS#1
DDR_A_DQS#2
DDR_A_DQS#3
DDR_A_DQS#4
DDR_A_DQS#5
DDR_A_DQS#6
DDR_A_DQS#7
DDR_A_DQS0
DDR_A_DQS1
DDR_A_DQS2
DDR_A_DQS3
DDR_A_DQS4
DDR_A_DQS5
DDR_A_DQS6
DDR_A_DQS7
DDR_VREF_S3
M_ODT0
M_ODT1
SC2D2U16V5ZY-2GP
C76
C82
SCD1U16V2ZY-2GP
MH1
MH2
DDR2-200P-20-GP-U
RAS#
WE#
CAS#
CS0#
CS1#
CKE0
CKE1
CK0
CK0#
CK1
CK1#
DDR_A_RAS#
DDR_A_WE#
DDR_A_CAS#
DDR_CS0_DIMMA#
DDR_CS1_DIMMA#
DDR_CKE0_DIMMA
DDR_CKE1_DIMMA
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
DDR_A_DM0
DDR_A_DM1
DDR_A_DM2
DDR_A_DM3
DDR_A_DM4
DDR_A_DM5
DDR_A_DM6
DDR_A_DM7
SDA
SCL
ICH_SMBDATA
ICH_SMBCLK
VDDSPD
SA0
SA1
R416
R417
10KR2J-3-GP
PM_EXTTS#0
NC#50
NC#69
NC#83
NC#120
NC#163/TEST
C569
C571
SC2D2U6D3V3KX-GP
3D3V_S0
VDD
VSS
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT1
Size
Custom
Document Number
Pamirs-Discrete
Rev
SA
Date: Wednesday, October 18, 2006
Sheet 13 of 47


8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]
8 DDR_B_BS[0..2]
Layout Note:
Place near DM2
1D8V_S3
DY
C541 C508 C244 C497 C232 C513 C170 C221 C264
SCD2U16V2ZY-2GP
SCD1U16V2ZY-2GP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C245 C256 C184 C207 C234 C265 C226 C235 C243 C237 C215 C183 C225
SCD1U16V2ZY-2GP
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
RN18 RN21 RN19 RN22 RN24 RN27 RN9 RN10 RN7 RN14 RN12 RN16 RN25 RN6
SRN56J-4-GP
DDR_B_MA3 DDR_B_MA1 DDR_B_MA10 DDR_B_BS0 DDR_B_MA0 DDR_B_BS1 DDR_CS2_DIMMB# DDR_B_RAS# DDR_B_WE# DDR_B_CAS# DDR_CS3_DIMMB# M_ODT3 DDR_B_MA14
DDR_B_MA12 DDR_B_MA9 DDR_CKE3_DIMMB DDR_B_MA11 DDR_B_MA5 DDR_B_MA8 DDR_B_MA7 DDR_B_MA6 DDR_B_MA4 DDR_B_MA2 M_ODT2 DDR_B_MA13 DDR_B_BS2 DDR_CKE2_DIMMB
DM1
DDR2-200P-21-GP-U
DDR_B_MA0 DDR_B_MA1 DDR_B_MA2 DDR_B_MA3 DDR_B_MA4 DDR_B_MA5 DDR_B_MA6 DDR_B_MA7 DDR_B_MA8 DDR_B_MA9 DDR_B_MA10 DDR_B_MA11 DDR_B_MA12 DDR_B_MA13 DDR_B_MA14
DDR_B_BS2 DDR_B_BS0 DDR_B_BS1
DDR_B_D0 DDR_B_D1 DDR_B_D2 DDR_B_D3 DDR_B_D4 DDR_B_D5 DDR_B_D6 DDR_B_D7 DDR_B_D8 DDR_B_D9 DDR_B_D10 DDR_B_D11 DDR_B_D12 DDR_B_D13 DDR_B_D14 DDR_B_D15 DDR_B_D16 DDR_B_D17 DDR_B_D18 DDR_B_D19 DDR_B_D20 DDR_B_D21 DDR_B_D22 DDR_B_D23 DDR_B_D24 DDR_B_D25 DDR_B_D26 DDR_B_D27 DDR_B_D28 DDR_B_D29 DDR_B_D30 DDR_B_D31 DDR_B_D32 DDR_B_D33 DDR_B_D34 DDR_B_D35 DDR_B_D36 DDR_B_D37 DDR_B_D38 DDR_B_D39 DDR_B_D40 DDR_B_D41 DDR_B_D42 DDR_B_D43 DDR_B_D44 DDR_B_D45 DDR_B_D46 DDR_B_D47 DDR_B_D48 DDR_B_D49 DDR_B_D50 DDR_B_D51 DDR_B_D52 DDR_B_D53 DDR_B_D54 DDR_B_D55 DDR_B_D56 DDR_B_D57 DDR_B_D58 DDR_B_D59 DDR_B_D60 DDR_B_D61 DDR_B_D62 DDR_B_D63
DDR_B_DQS#0 DDR_B_DQS#1 DDR_B_DQS#2 DDR_B_DQS#3 DDR_B_DQS#4 DDR_B_DQS#5 DDR_B_DQS#6 DDR_B_DQS#7
DDR_B_DQS0 DDR_B_DQS1 DDR_B_DQS2 DDR_B_DQS3 DDR_B_DQS4 DDR_B_DQS5 DDR_B_DQS6 DDR_B_DQS7
M_ODT2 M_ODT3
DDR_VREF_S3
SC2D2U16V5ZY-2GP
C71 C77
SCD1U16V2ZY-2GP
DDR_B_RAS# DDR_B_WE# DDR_B_CAS# DDR_CS2_DIMMB# DDR_CS3_DIMMB# DDR_CKE2_DIMMB DDR_CKE3_DIMMB M_CLK_DDR2 M_CLK_DDR#2 M_CLK_DDR3 M_CLK_DDR#3
DDR_B_DM0 DDR_B_DM1 DDR_B_DM2 DDR_B_DM3 DDR_B_DM4 DDR_B_DM5 DDR_B_DM6 DDR_B_DM7
ICH_SMBDATA 3,13,20
ICH_SMBCLK 3,13,20
SCD1U16V2ZY-2GP
3D3V_S0
R420 R421 10KR2J-3-GP
C577 C578 SC2D2U6D3V3KX-GP
PM_EXTTS#1 7
1D8V_S3
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT2
Size Custom
Document Number
Pamirs-Discrete
Rev SA
Date: Wednesday, October 18, 2006
Sheet 14 of 47

CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

42 VGA_RED
42 VGA_GREEN
42 VGA_BLUE

L8 BLM18BB470SN1-GP
L2 BLM18BB470SN1-GP
L1 BLM18BB470SN1-GP

R23 150R2F-1-GP
R20 150R2F-1-GP
R19 150R2F-1-GP

C35 SC10P50V2JN-4GP
C29 SC10P50V2JN-4GP
C22 SC10P50V2JN-4GP
C32 SC10P50V2JN-4GP
C26 SC10P50V2JN-4GP
C21 SC10P50V2JN-4GP

CRT_R → CRT_R 17
CRT_G → CRT_G 17
CRT_B → CRT_B 17

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

5V_CRT_S0 → F1 FUSE-1D1A6V-8GP → 5V_S0
C13 SCD01U16V2KX-3GP
D4 CH751H-40PT-1GP
5V_CRT1_S0
RN1 SRN2K2J-1-GP

CRT1 20.20424.015
CRT_R, CRT_G, CRT_B
DDC_DATA_CON, DDC_CLK_CON
JVGA_HS, JVGA_VS

C15 SC33P50V2JN-3GP DY
C20 SC33P50V2JN-3GP DY
C11 SC22P50V2JN-4GP
C9 SC22P50V2JN-4GP

DDC_DATA_CON → D12 BAV99W-1-GP DY
DDC_CLK_CON → D11 BAV99W-1-GP DY

5V_CRT1_S0 → U3 PACDN009MR-GP-U DY
GMCH_HSYNC, GMCH_VSYNC
CRT_G, CRT_R, CRT_B

5V_S0 → C464 SCD1U16V2ZY-2GP
PR_INSERT 17

17,42 GMCH_HSYNC → U6A TSAHCT125PW-GP → HSYNC_5
17,42 GMCH_VSYNC → U6B TSAHCT125PW-GP → VSYNC_5
RN4 SRN33J-5-GP-U → JVGA_HS, JVGA_VS

3D3V_S0
RN2 SRN2K2J-1-GP

U1 2N7002DW-1-GP
42 VGA_DDCDATA ↔ DDC_DATA_CON ↔ DDC_DATA_CON 17
17 DDC_CLK_CON ↔ DDC_CLK_CON ↔ VGA_DDCCLK 42

5V @ ext. CRT side

TV OUT CONN

connector

42 VGA_TV_CRMA → L32 BLM18BB470SN1-GP → TV_CRMA 17
R1 150R2F-1-GP
C432 SC10P50V2JN-4GP
C431 SC10P50V2JN-4GP

42 VGA_TV_COMP → L33 BLM18BB470SN1-GP → TV_COMP 17
R3 150R2F-1-GP
C434 SC10P50V2JN-4GP
C433 SC10P50V2JN-4GP

42 VGA_TV_LUMA → L34 BLM18BB470SN1-GP → TV_LUMA 17
R2 150R2F-1-GP
C438 SC10P50V2JN-4GP
C437 SC10P50V2JN-4GP

Place this 2 resistors close to the TV-out connector

TV1 MINDIN7-16-GP-U
TV_LUMA, TV_CRMA, TV_COMP
LUMA, CRMA, COMP, NC#2, NC#5, GND, GND, GND, GND

D1 BAV99W-1-GP DY
VGA_TV_COMP → C1 SCD1U16V2ZY-2GP DY

D3 BAV99W-1-GP DY
VGA_TV_LUMA → C3 SCD1U16V2ZY-2GP DY

D2 BAV99W-1-GP DY
VGA_TV_CRMA → C2 SCD1U16V2ZY-2GP DY

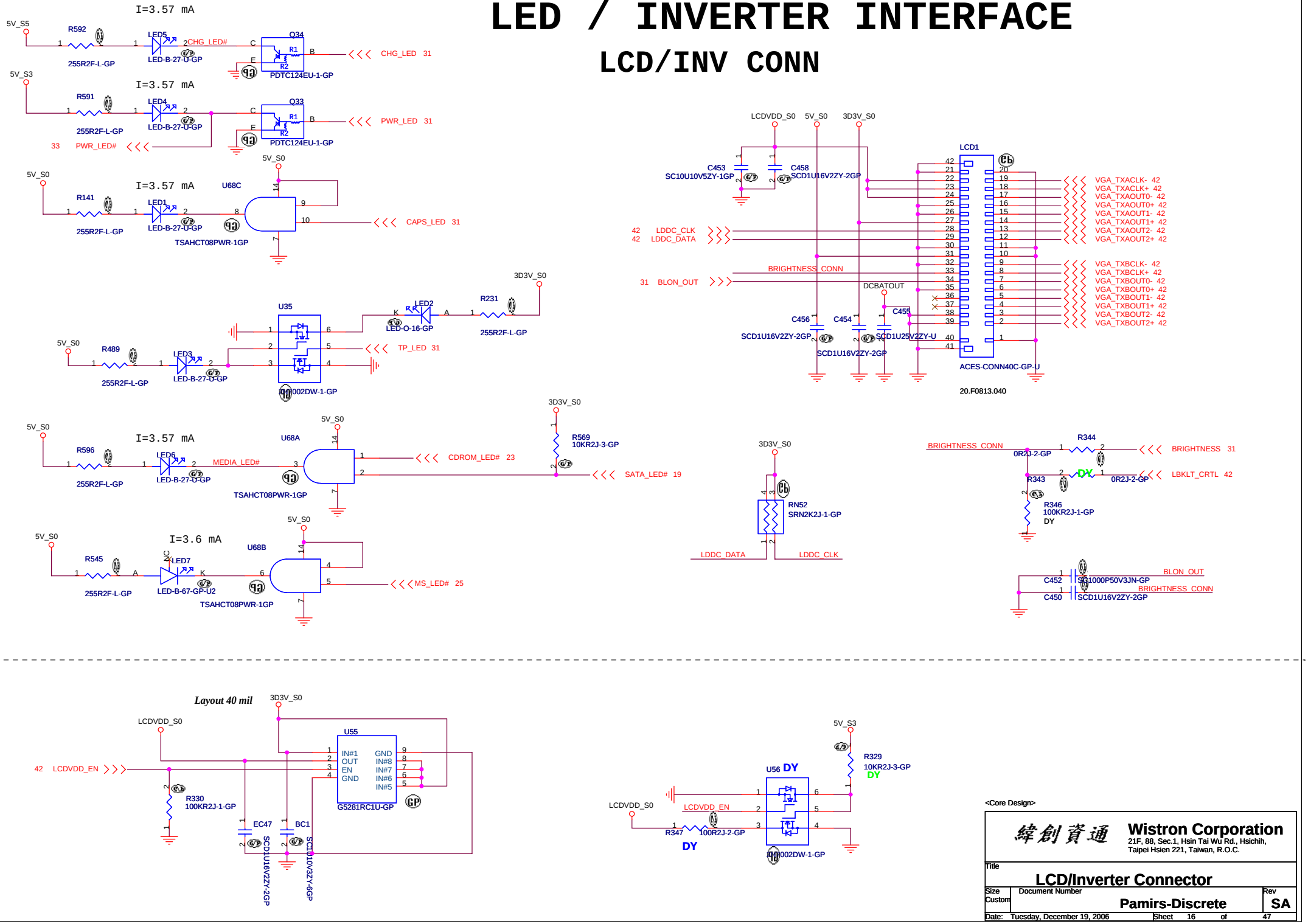
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT/TV Connector**
Size: A3 | Document Number: Pamirs-Discrete | Rev: SA
Date: Friday, November 24, 2006 | Sheet 15 of 47

LED / INVERTER INTERFACE

LCD/INV CONN



<Core Design>

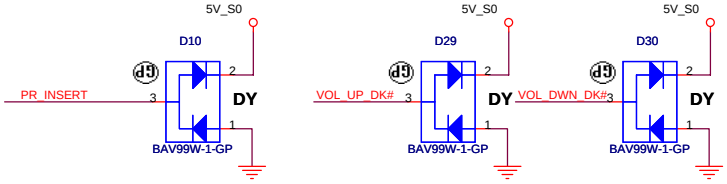
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

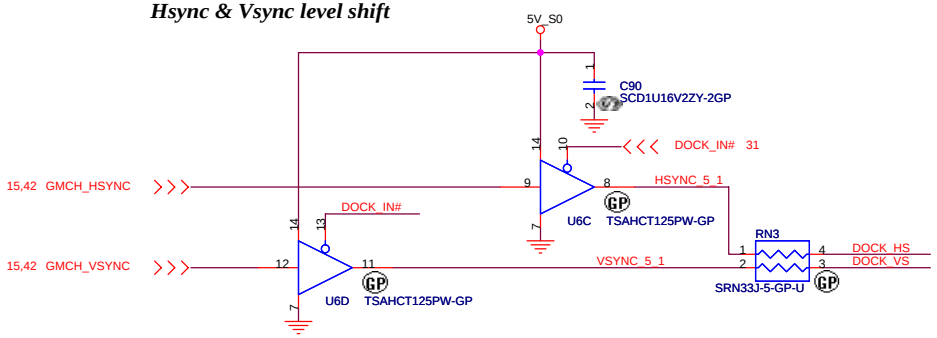
Size	Document Number	Rev
Custom	Pamirs-Discrete	SA

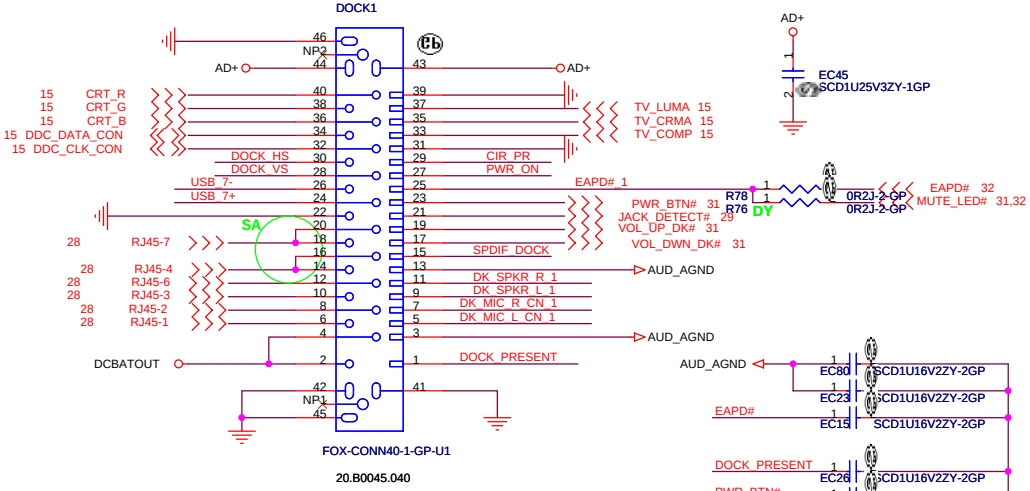
Date: Tuesday, December 19, 2006 Sheet 16 of 47

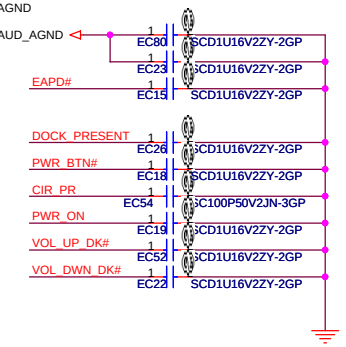
Docking Connector

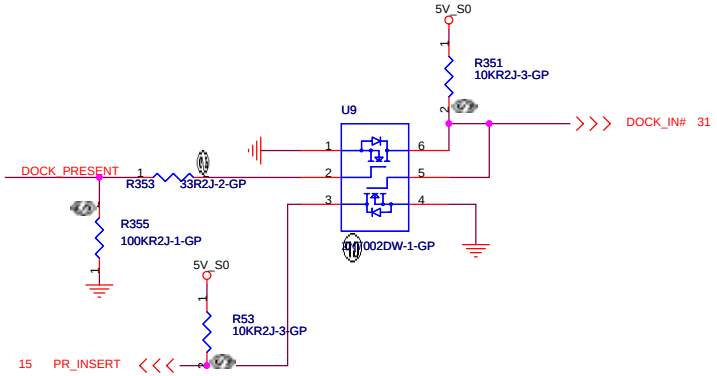


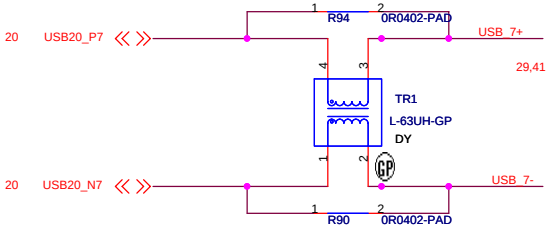
Hsync & Vsync level shift

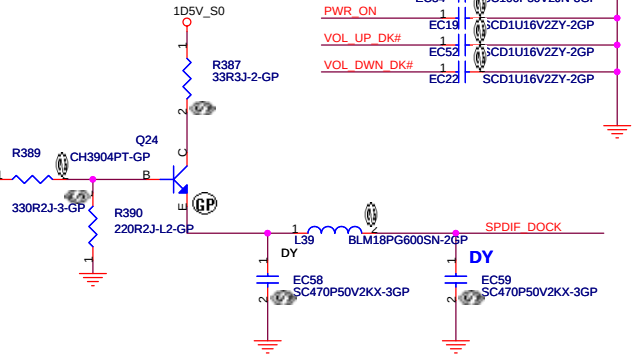


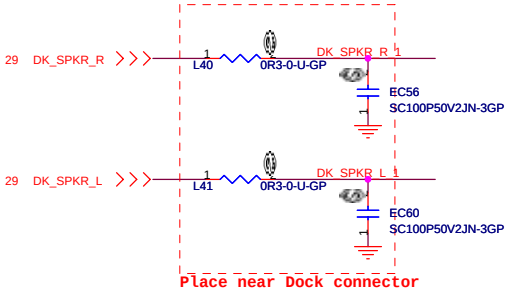


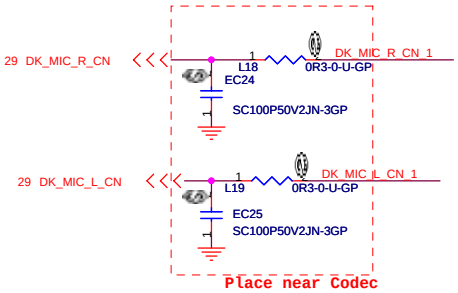


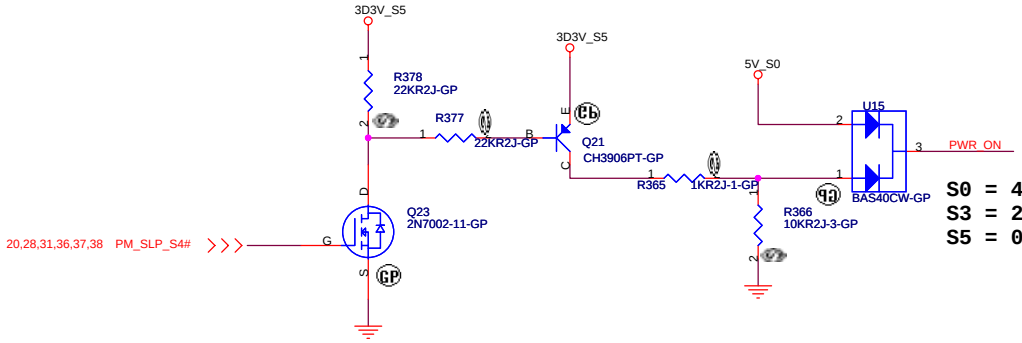












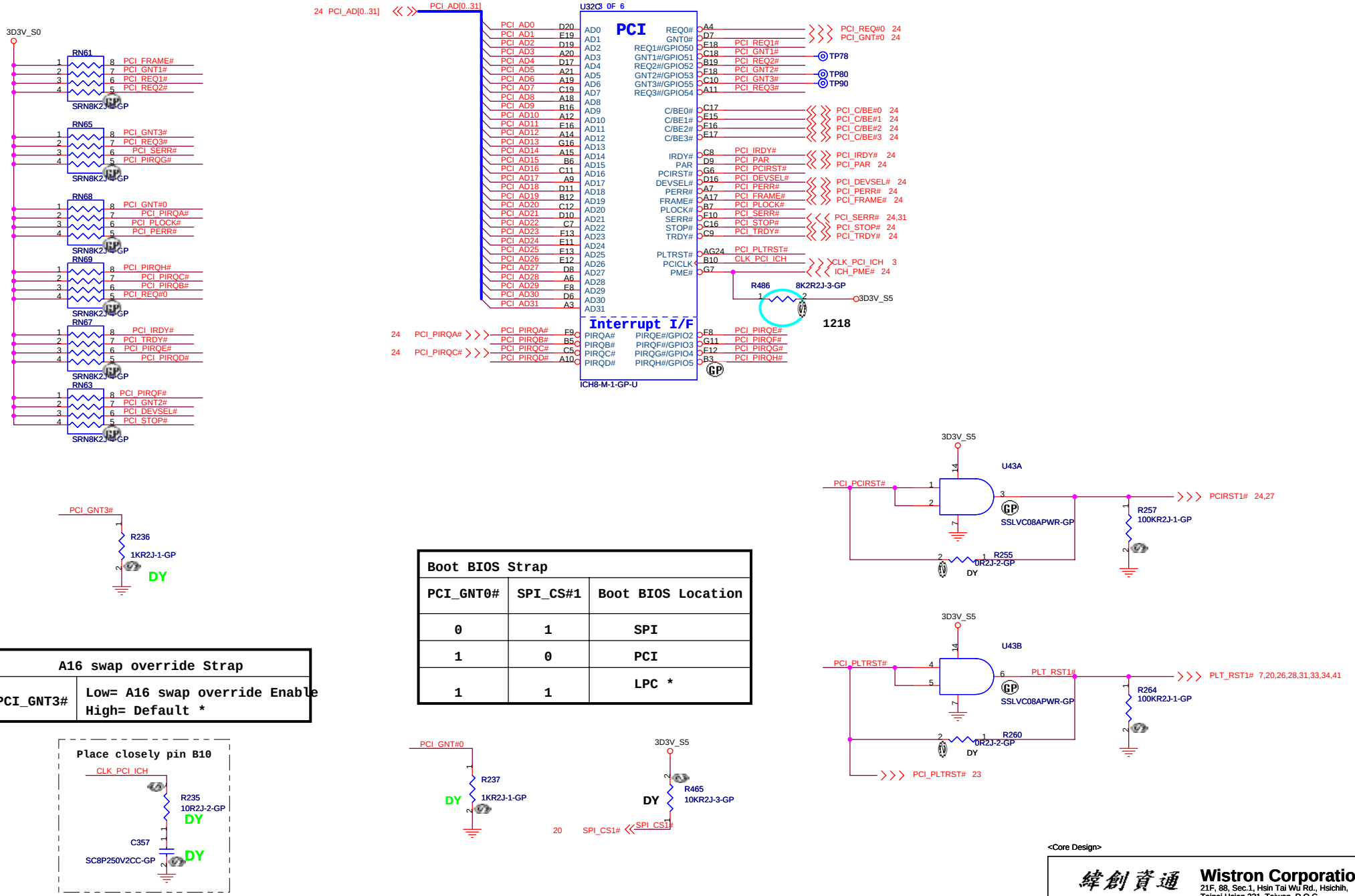
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Board to board conn/ Docking***

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Friday, November 24, 2006 Sheet 17 of 47



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

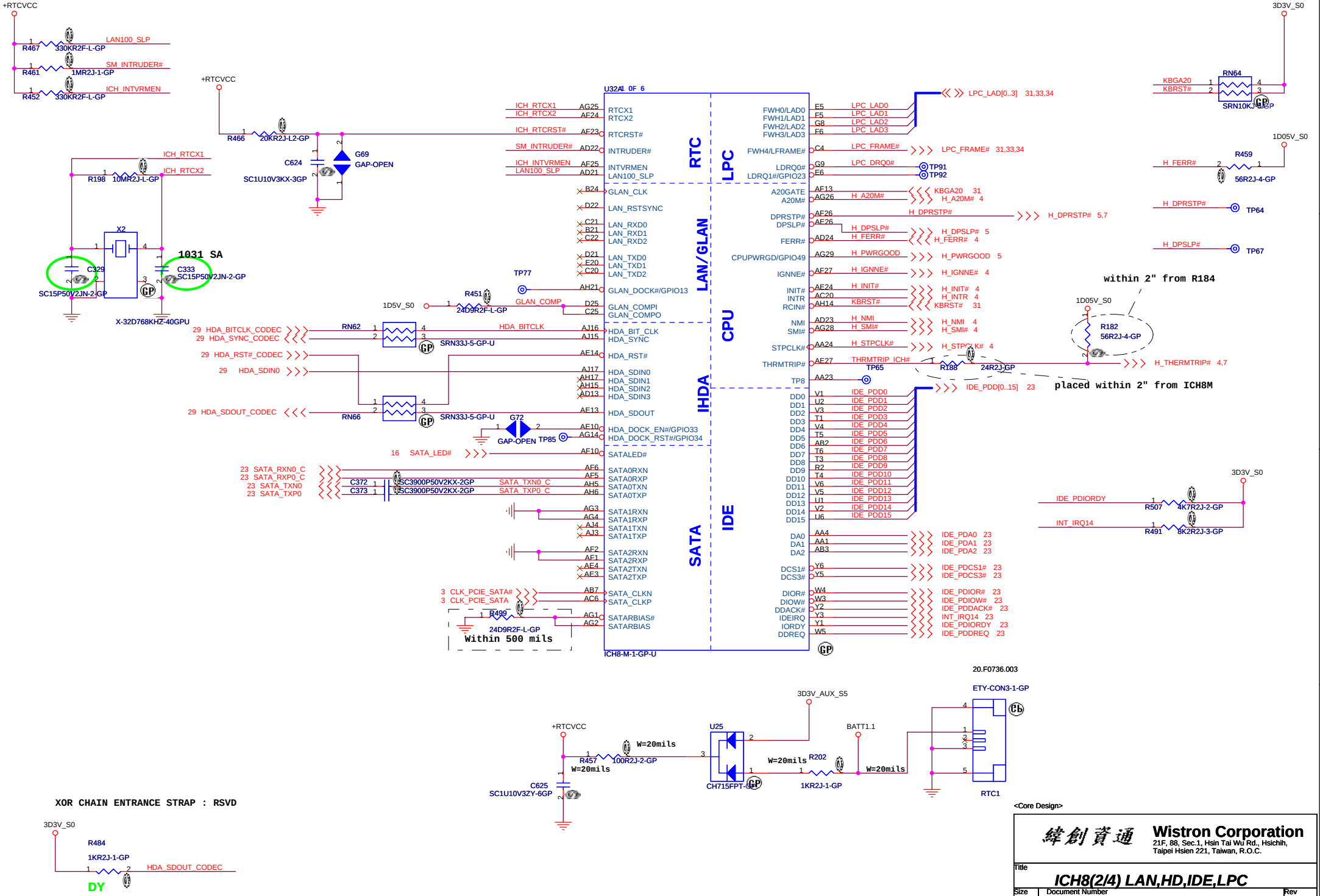
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(1/4)-PCI/INT

Size: A3 | Document Number: Pamirs-Discrete | Rev: SA

Date: Monday, December 18, 2006 | Sheet 18 of 47

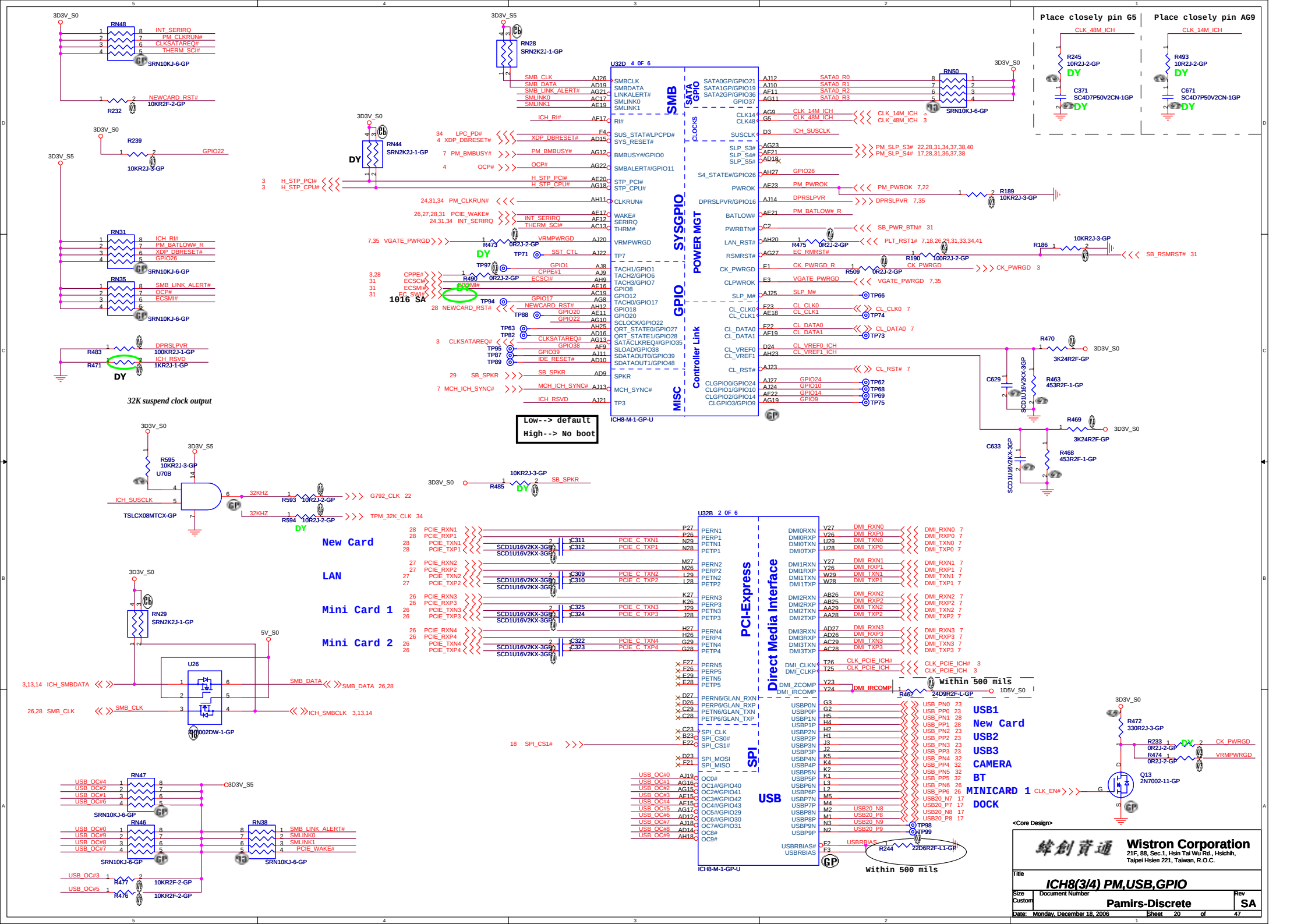


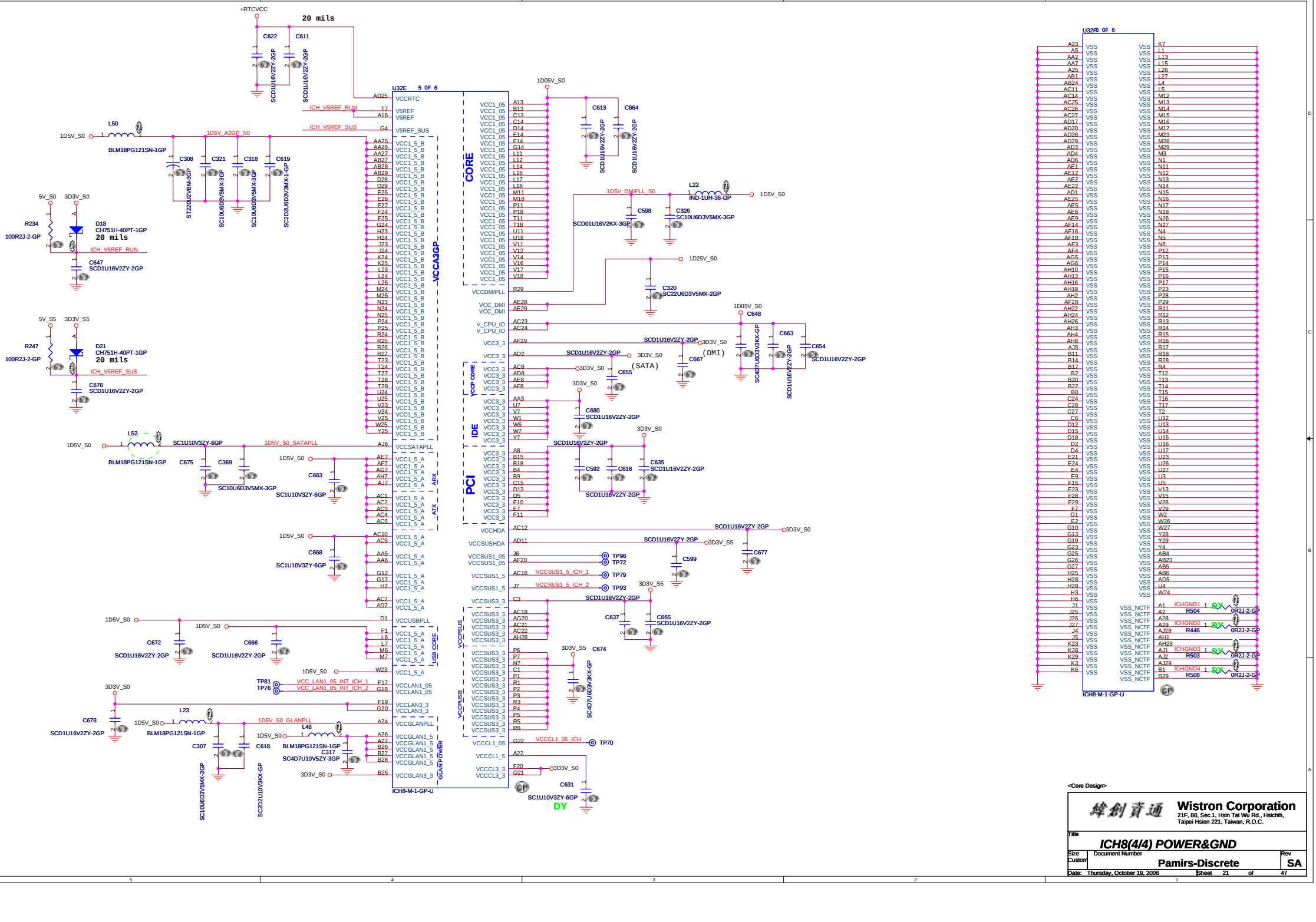
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

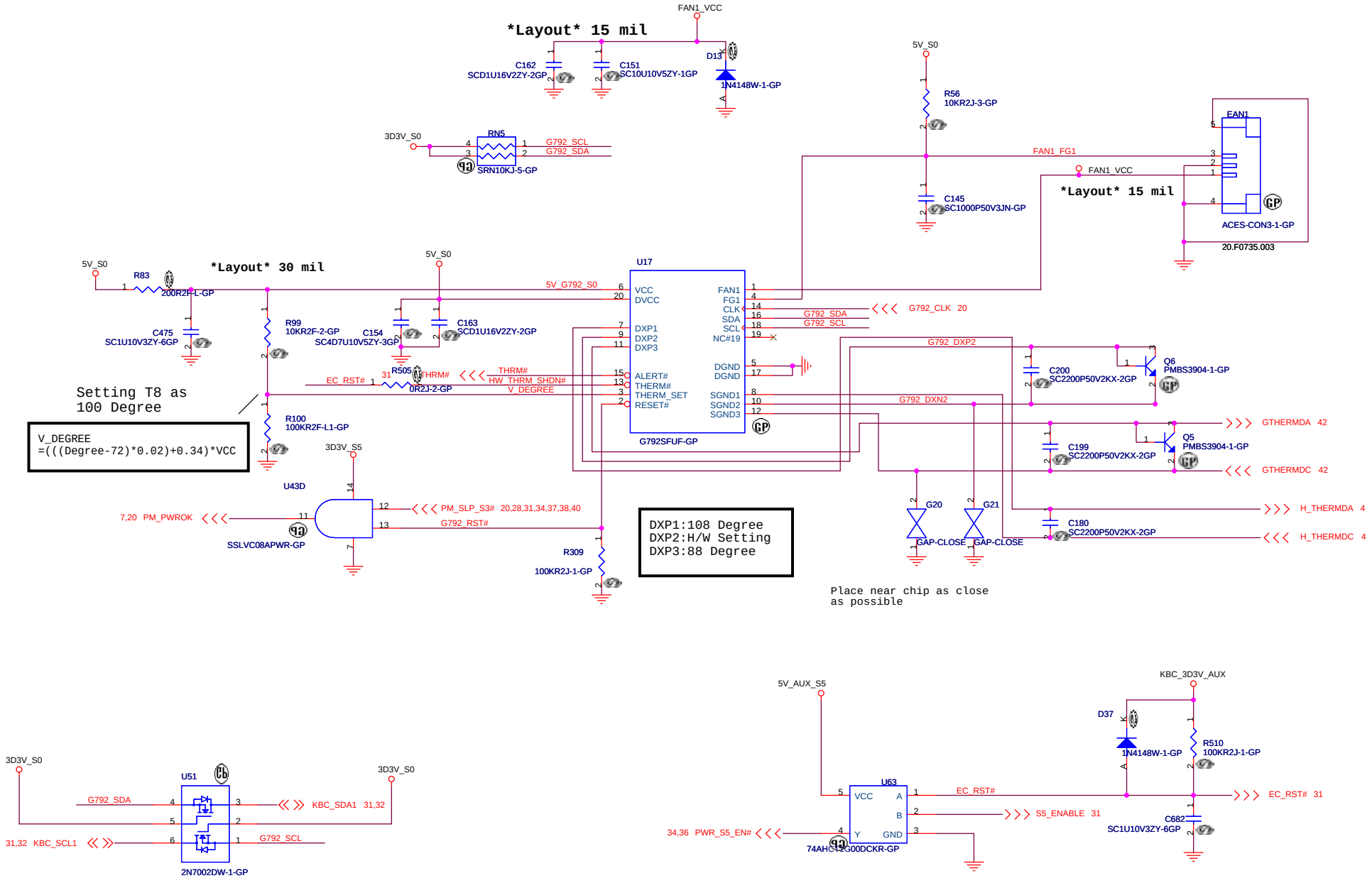
Title: ICH8(2/4) LAN,HD,IDE,LPC

Size: A3 | Document Number: Pamirs-Discrete | Rev: SA

Date: Wednesday, December 13, 2006 | Sheet 19 of 47


Place closely pin G5
Place closely pin AG9
U32D 4 OF 6
ICH8-M-1-GP-U
U32B 2 OF 6
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
PCI-Express
Direct Media Interface
SPI
USB
Low--> default
High--> No boot
1016 SA
32K suspend clock output
New Card
LAN
Mini Card 1
Mini Card 2
USB1
New Card
USB2
USB3
CAMERA
BT
MINICARD 1
DOCK
Within 500 mils
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH8(3/4) PM,USB,GPIO
Pamirs-Discrete
SA
Monday, December 18, 2006
Sheet 20 of 47


+RTCVCC
20 mils
C622
C611
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
U32E 5 0F 6
ICH_V5REF_RUN
ICH_V5REF_SUS
1D5V_S0
L50
BLM18PG121SN-1GP
1D5V_A3GP_S0
C308
C321
C318
C619
ST22DU2V8M-3GP
SC10U6D3V5MX-3GP
SC10U6D3V5MX-3GP
SC22D2U6D3V3MX-1-GP
5V_S0
3D3V_S0
R234
100R2J-2-GP
D18
CH751H-40PT-1GP
20 mils
C647
SCD1U16V2ZY-2GP
5V_S5
3D3V_S5
R247
100R2J-2-GP
D21
CH751H-40PT-1GP
20 mils
C676
SCD1U16V2ZY-2GP
L52
BLM18PG121SN-1GP
SC1U10V3ZY-6GP
1D5V_S0_SATAPLL
C675
C369
SC10U6D3V5MX-3GP
C683
SC1U10V3ZY-6GP
C668
SC1U10V3ZY-6GP
C672
SCD1U16V2ZY-2GP
C666
SCD1U16V2ZY-2GP
TP81
TP76
VCC_LAN1_05_INT_ICH_1
VCC_LAN1_05_INT_ICH_2
L23
BLM18PG121SN-1GP
C678
SCD1U16V2ZY-2GP
1D5V_S0_GLANPLL
L48
BLM18PG121SN-1GP
C307
C618
C317
SC4D7U10V5ZY-3GP
SC10U6D3V5MX-3GP
SC22D2U10V3KX-GP
ICH8-M-1-GP-U
VCCA3GP
CORE
PCI
IDE
USB CORE
GLAN POWER
VCCPSUS
VCCPUSB
1D05V_S0
C613
C664
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
1D5V_DMIPLL_S0
L22
IND-1UH-38-GP
C598
SCD01U16V2KX-3GP
C326
SC10U6D3V5MX-3GP
1D25V_S0
C320
SC22U6D3V5MX-2GP
1D05V_S0
C648
SCD1U16V2ZY-2GP
3D3V_S0
(DMI)
C667
C663
SC4D7U6D3V3KX-GP
C654
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
(SATA)
C655
3D3V_S0
C680
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
C592
C616
C635
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
3D3V_S0
C677
SCD1U16V2ZY-2GP
3D3V_S5
C599
TP96
TP72
TP79
TP93
VCCSUS1_5_ICH_1
VCCSUS1_5_ICH_2
3D3V_S5
C637
C665
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
3D3V_S5
C674
SC4D7U6D3V3KX-GP
TP70
VCCCL1_05_ICH
3D3V_S0
C631
SC1U10V3ZY-6GP
DY
U32F6 0F 6
ICH8-M-1-GP-U
ICHGND1
ICHGND2
ICHGND3
ICHGND4
R504
R446
R503
R508
0R2J-2-GP
DY
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(4/4) POWER&GND
Size
Custom
Document Number
Pamirs-Discrete
Rev
SA
Date: Thursday, October 19, 2006
Sheet 21 of 47



<Core Design>

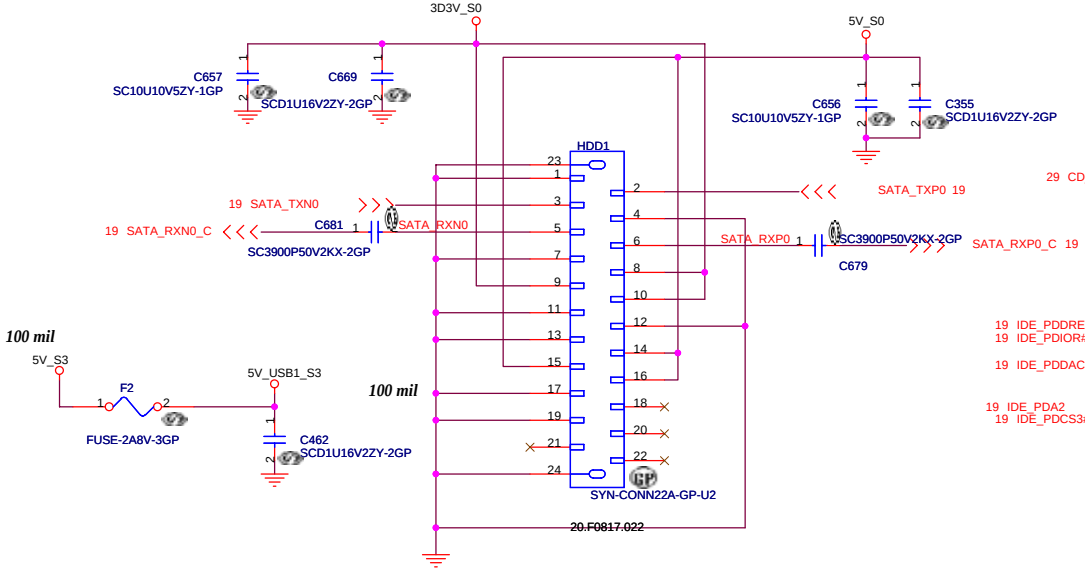
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor G792

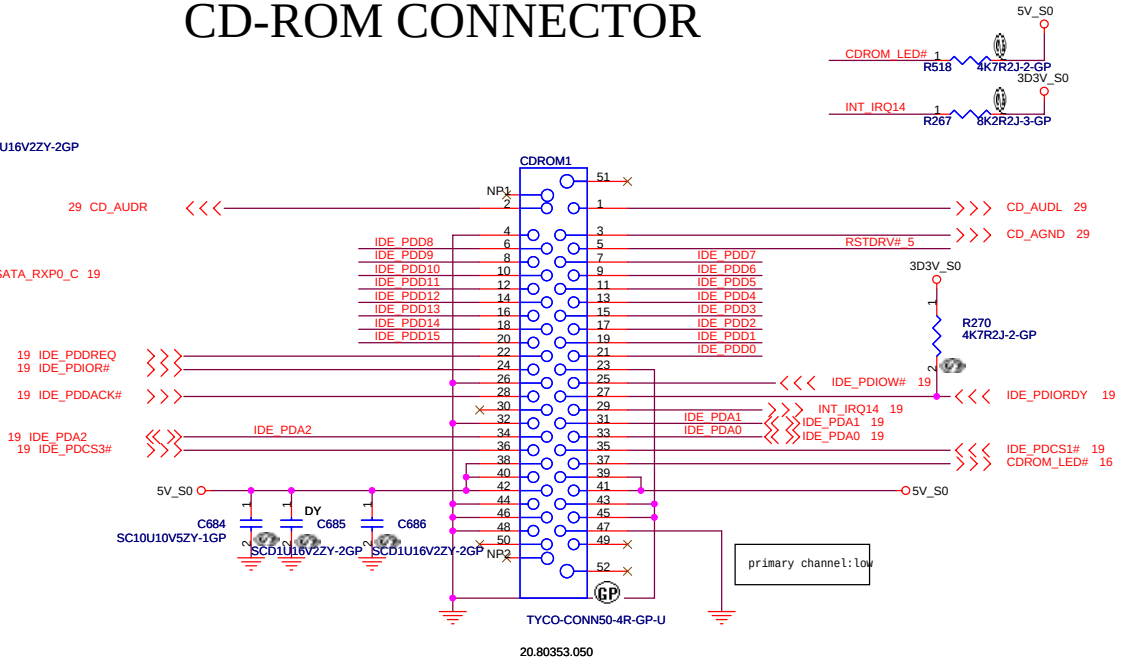
Size	Document Number	Rev
Custom	Pamirs-Discrete	SA

Date: Monday, October 23, 2006 Sheet 22 of 47

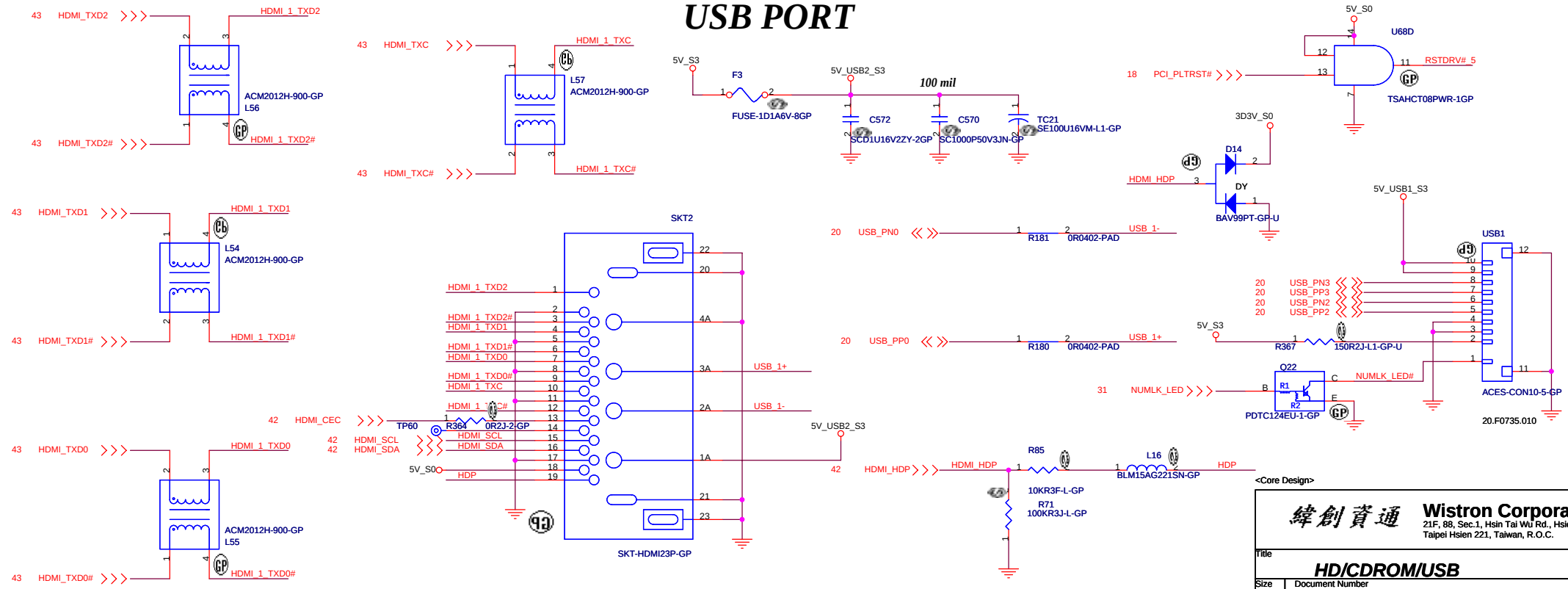
SATA HD Connector



CD-ROM CONNECTOR



USB PORT



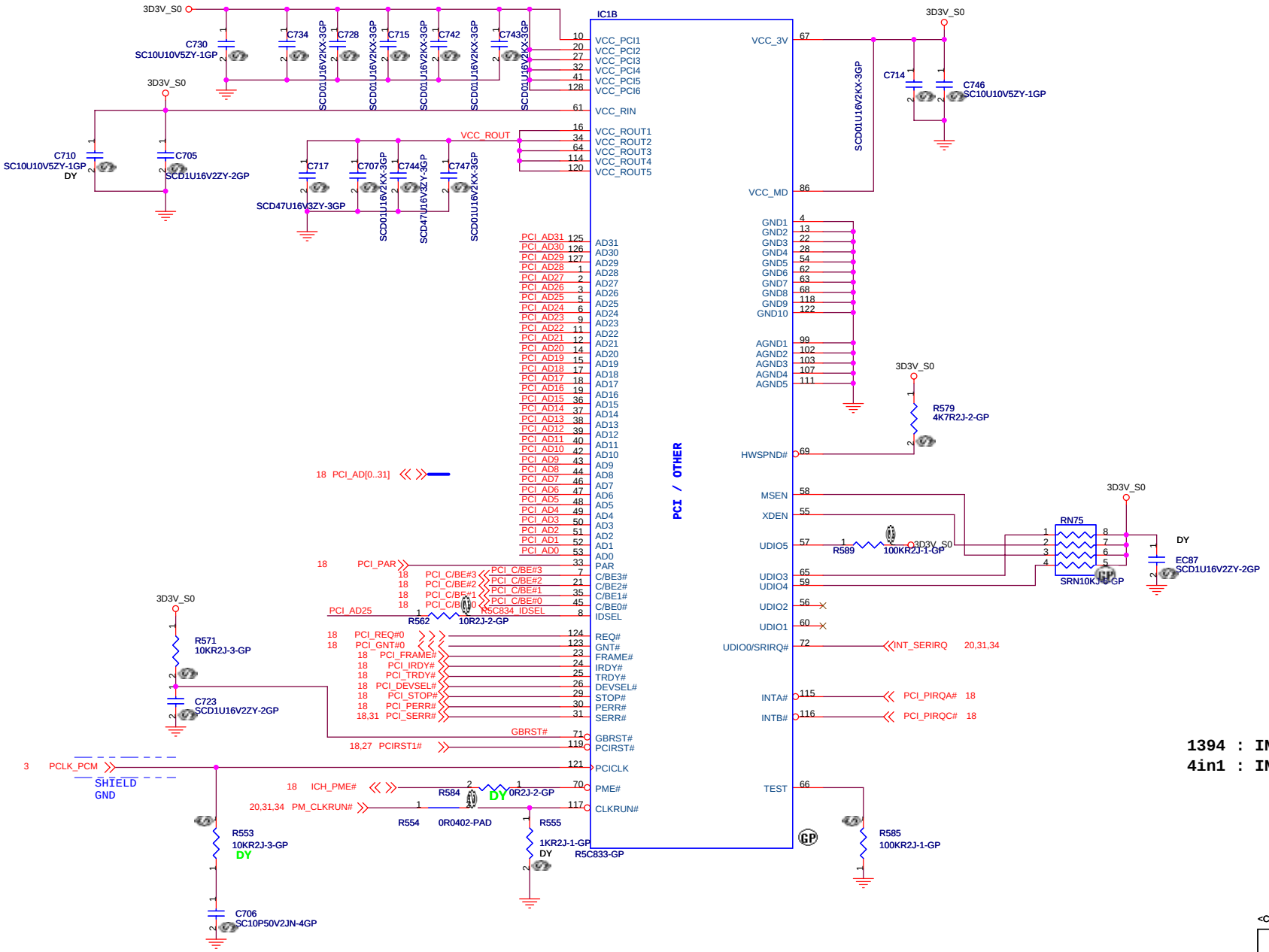
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HD/CDROM/USB**

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Tuesday, December 12, 2006 Sheet 23 of 47



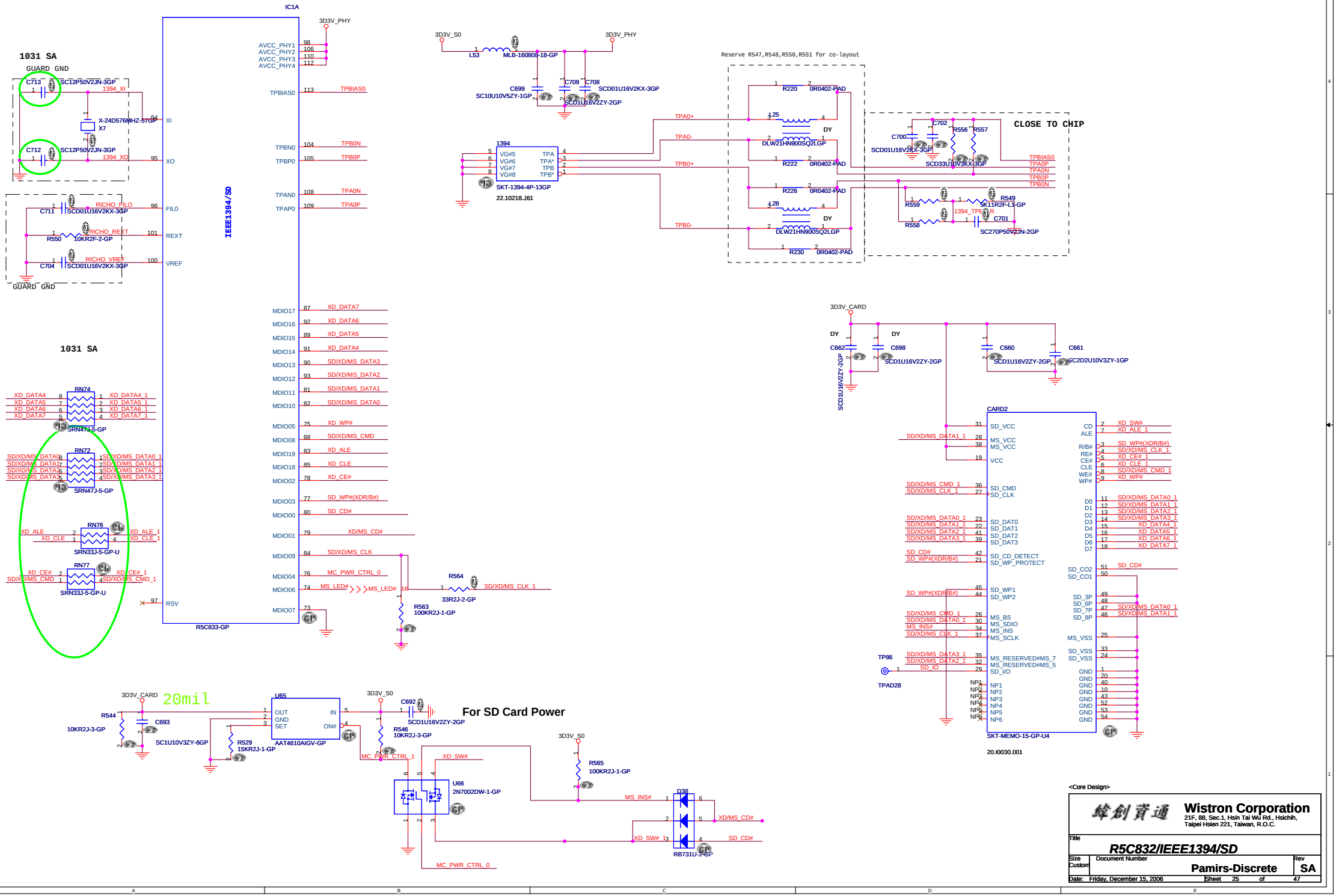
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***R5C832/PCI***

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Wednesday, December 06, 2006 Sheet 24 of 47


IC1A
IEEE1394/SD
R5C833-GP
1031 SA
GUARD GND
3D3V_PHY
3D3V_S0
Reserve R547,R548,R550,R551 for co-layout
CLOSE TO CHIP
1394
SKT-1394-4P-13GP
22.10218.J61
DLW21HN900SQ2LGP
SCD01U16V2KX-3GP
SCD1U16V2ZY-2GP
SC12P50V2JN-3GP
X-24D576MHZ-57GP
SCD33U10V3KX-3GP
SK11R2F-L1-GP
SC270P50V2JN-2GP
SRN47J-5-GP
SRN33J-5-GP-U
SRN47J-5-GP
3D3V_CARD
CARD2
SKT-MEMO-15-GP-U4
20.I0030.001
For SD Card Power
20mil
AAT4610AIGV-GP
SC1U10V3ZY-6GP
SCD1U16V2ZY-2GP
2N7002DW-1-GP
RB731U-2-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
R5C832/IEEE1394/SD
Pamirs-Discrete
SA
Date: Friday, December 15, 2006
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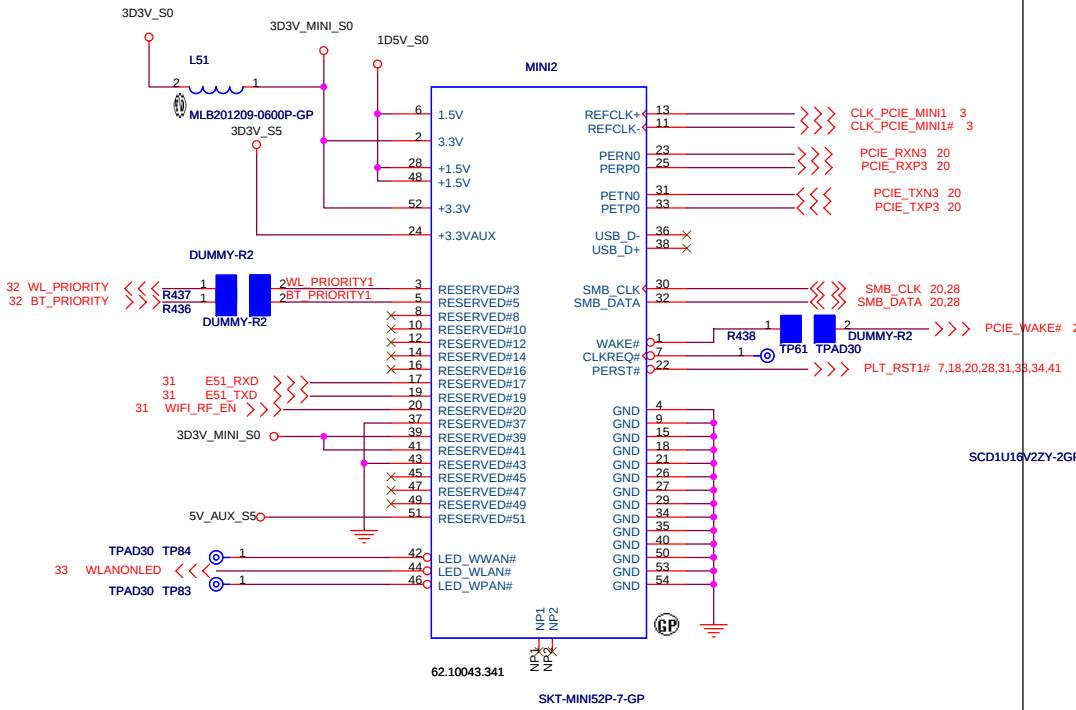
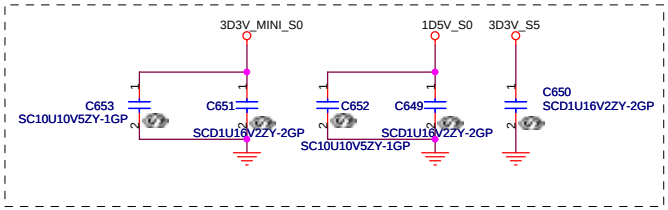
Mini Card Connector 2

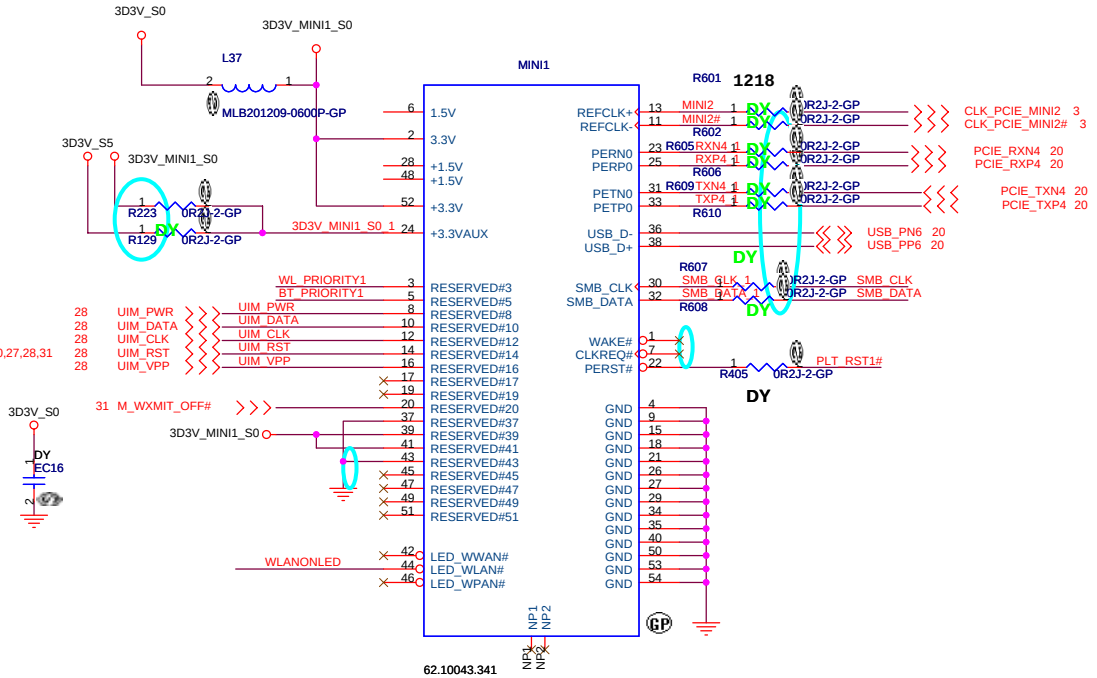
Wireless card

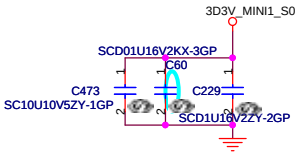




Mini Card Connector 1

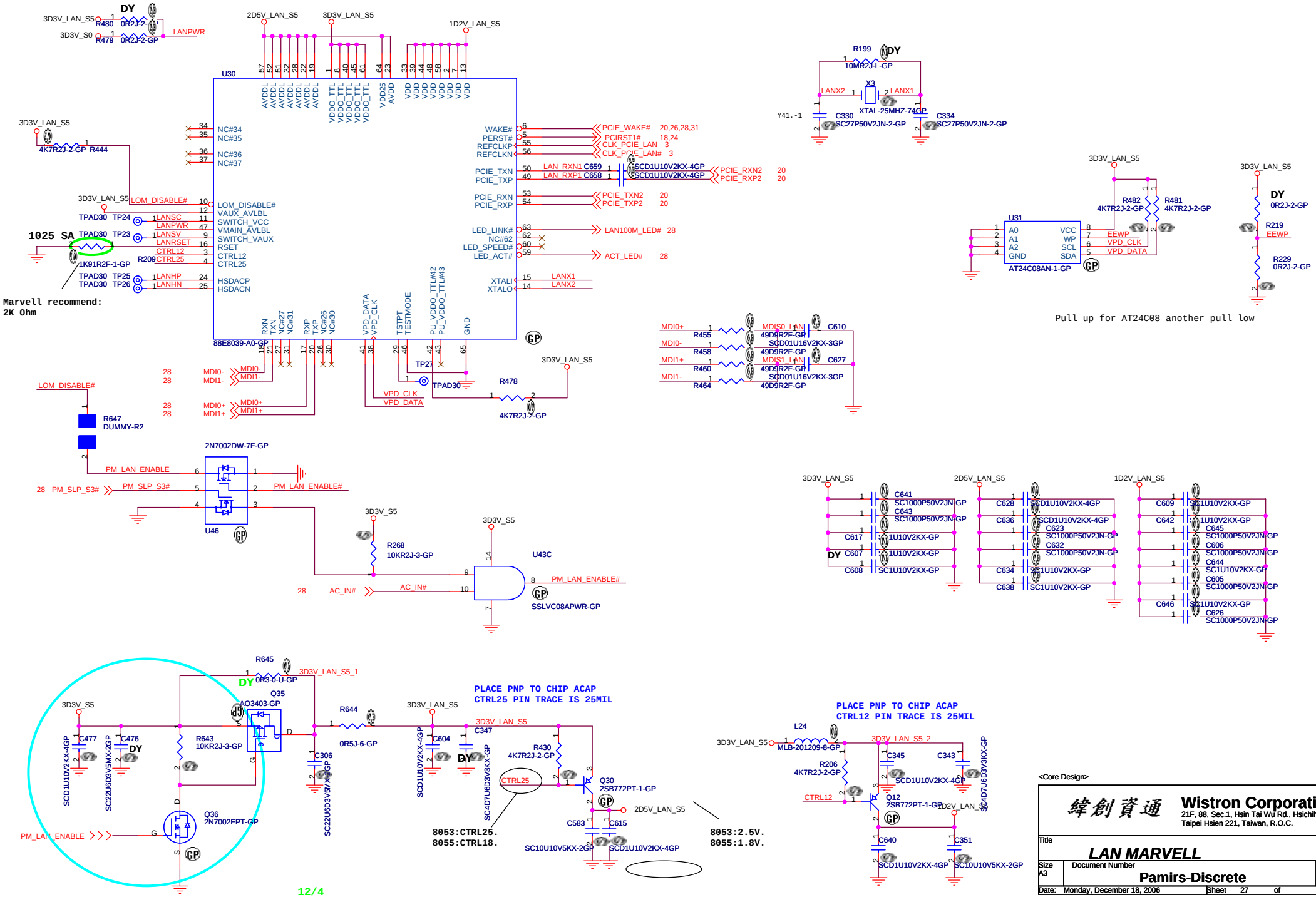
WWAN





<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI CARD CONN .***	
Size A3	Document Number **Pamirs-Discrete**	Rev **SA**
Date: Tuesday, December 19, 2006	Sheet 26 of 47	


U30
88E8039-A0-GP
1025 SA
Marvell recommend:
2K Ohm
LOM_DISABLE#
LANPWR
LANSC
LANSV
LANRSET
CTRL12
CTRL25
LANHP
LANHN
HSDACP
HSDACN
PCIE_WAKE# 20,26,28,31
PCIRST1# 18,24
CLK_PCIE_LAN 3
CLK_PCIE_LAN# 3
PCIE_RXN2 20
PCIE_RXP2 20
PCIE_TXN2 20
PCIE_TXP2 20
LAN100M_LED# 28
ACT_LED# 28
LANX1
LANX2
U31
AT24C08AN-1-GP
EEWP
VPD_CLK
VPD_DATA
Pull up for AT24C08 another pull low
MDI0+
MDI0-
MDI1+
MDI1-
U46
2N7002DW-7F-GP
PM_LAN_ENABLE
PM_SLP_S3#
U43C
SSLVC08APWR-GP
AC_IN#
Q35
AO3403-GP
Q36
2N7002EPT-GP
Q30
2SB772PT-1-GP
Q12
2SB772PT-1-GP
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
8053:CTRL25.
8055:CTRL18.
8053:2.5V.
8055:1.8V.
12/4
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN MARVELL
Size A3
Document Number
Pamirs-Discrete
Rev SA
Date: Monday, December 18, 2006
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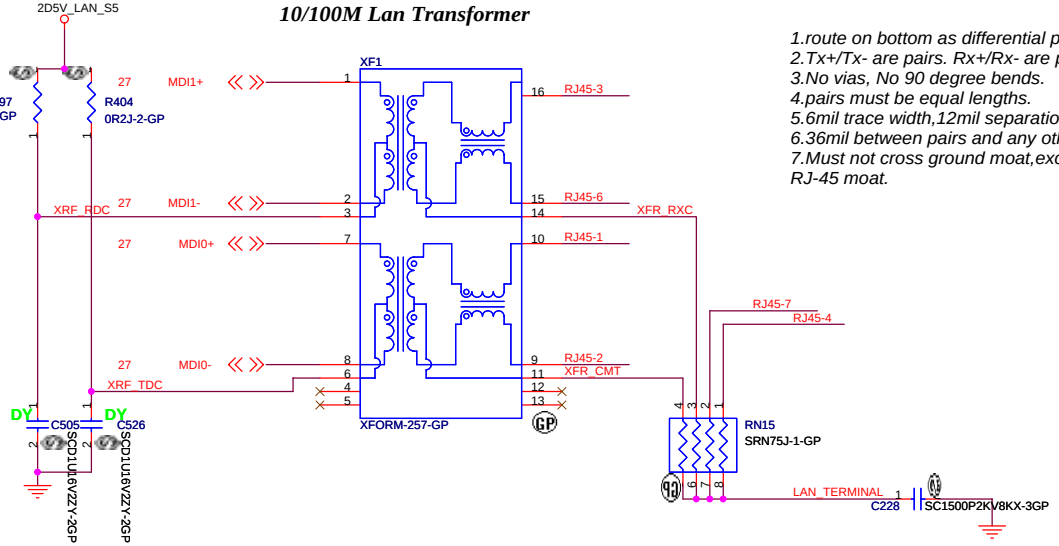
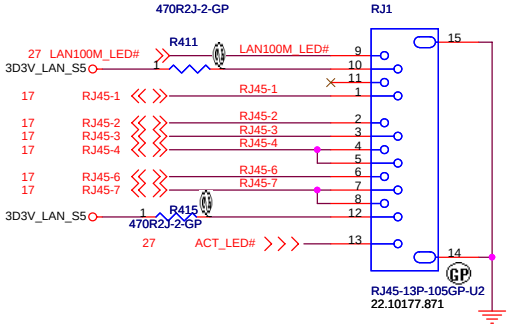
10/100M Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

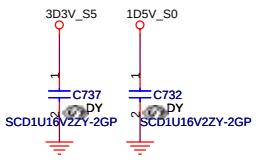
PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW



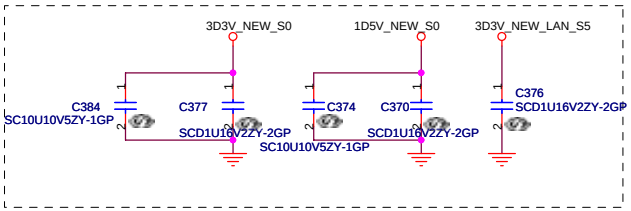
Green : Link up
Blinking : TX/RX activity

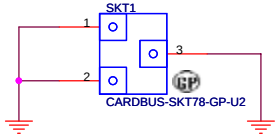
NEWCARD Connector

Place them Near to Chip

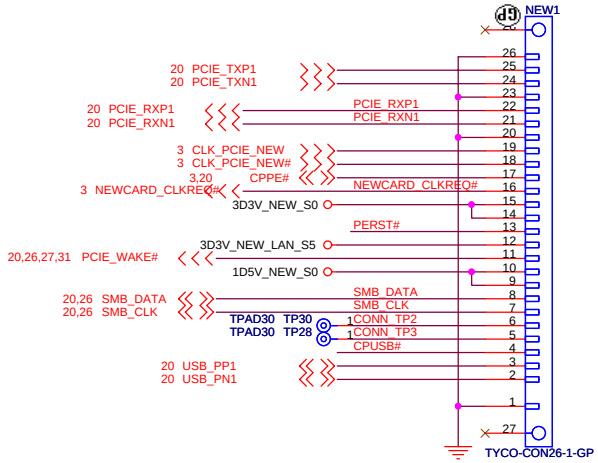


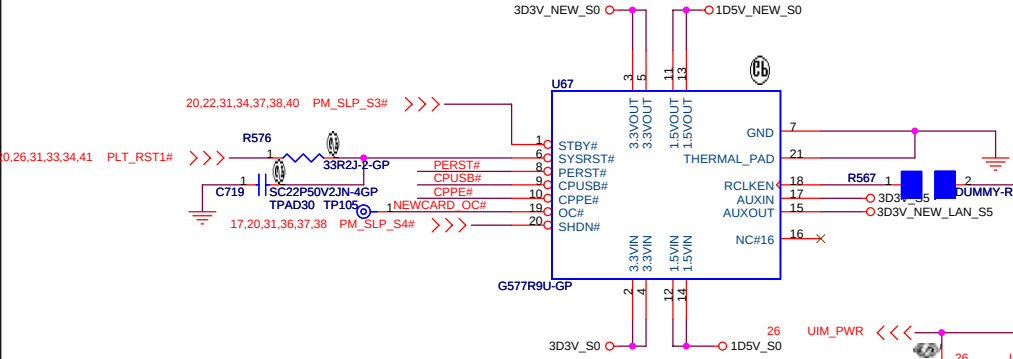
Place them Near to Connector

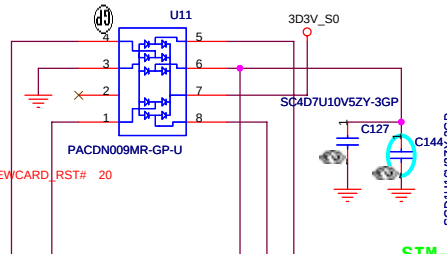




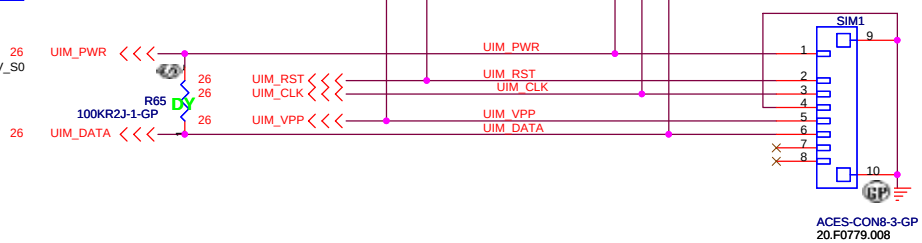
For Newcard socket

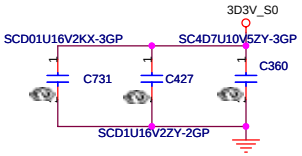






SIM-CARD





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN connector/NEW CARD/SIM**

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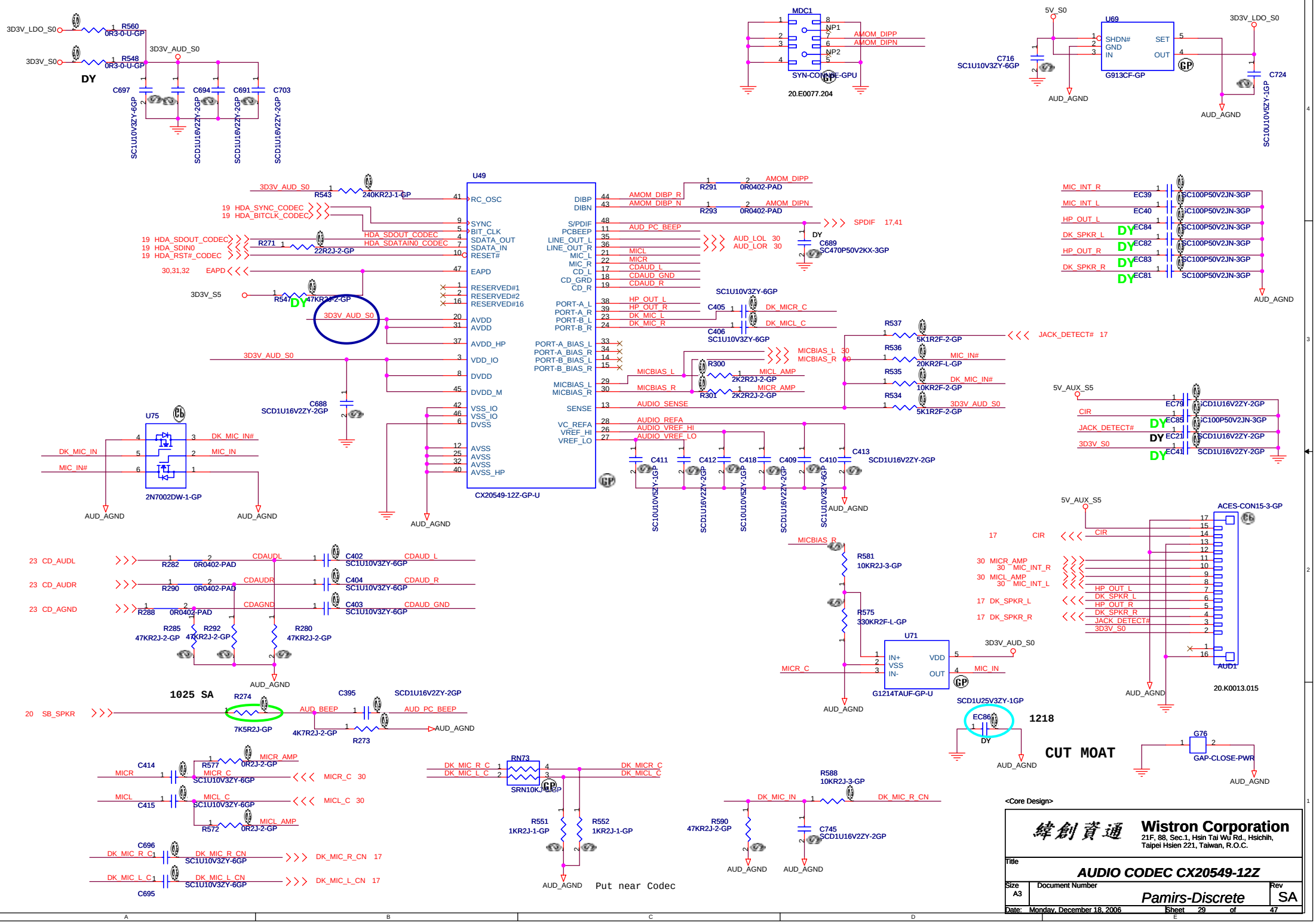
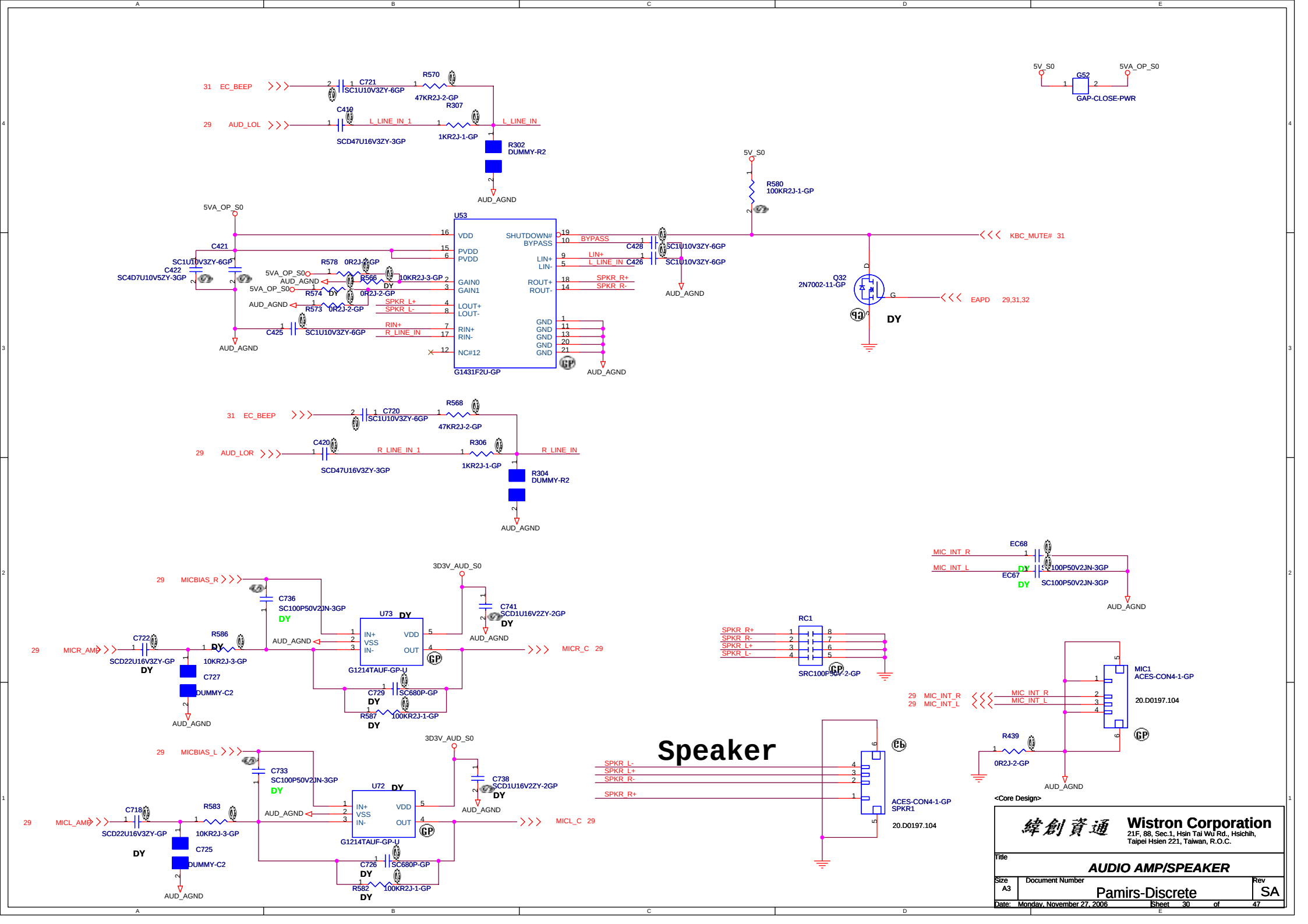
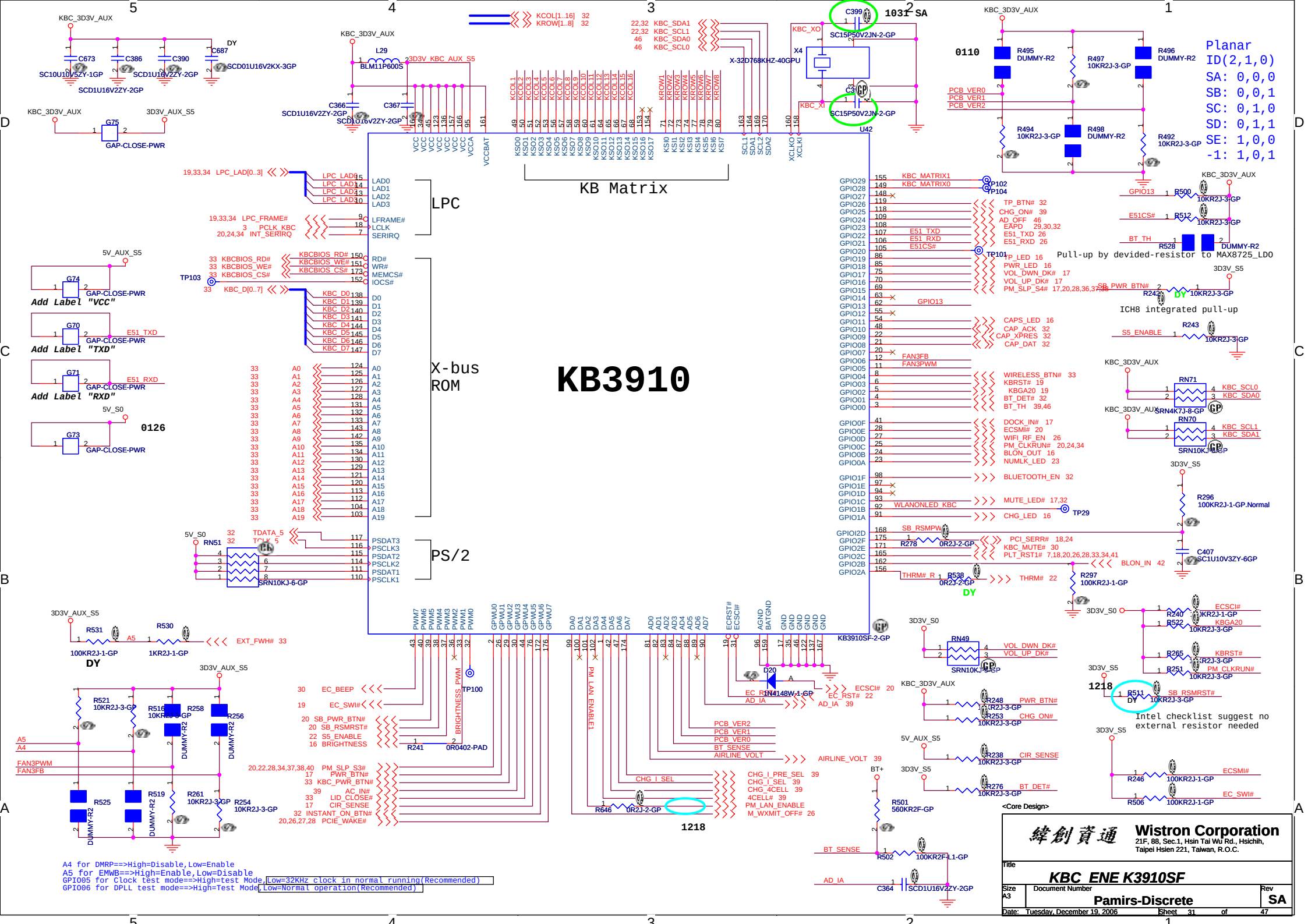
A3	Pamirs-Discrete	SA

Date: Tuesday, December 12, 2006 Sheet 28 of 47


3D3V_LDO_S0
R560 0R3-0-U-GP
3D3V_S0
R548 0R3-0-U-GP
3D3V_AUD_S0
DY
C697 SC1U10V3ZY-6GP
C694 SCD1U16V2ZY-2GP
C691 SCD1U16V2ZY-2GP
C703 SCD1U16V2ZY-2GP
MDC1
NP1
NP2
AMOM_DIPP
AMOM_DIPN
SYN-CONDE-GPU
20.E0077.204
5V_S0
U69
SHDN#
GND
IN
SET
OUT
G913CF-GP
C716 SC1U10V3ZY-6GP
C724 SC10U10V5ZY-1GP
AUD_AGND
3D3V_LDO_S0
U49
RC_OSC
SYNC
BIT_CLK
SDATA_OUT
SDATA_IN
RESET#
EAPD
RESERVED#1
RESERVED#2
RESERVED#16
AVDD
AVDD
AVDD_HP
VDD_IO
DVDD
DVDD_M
VSS_IO
VSS_IO
DVSS
AVSS
AVSS
AVSS
AVSS_HP
CX20549-12Z-GP-U
R543 240KR2J-1-GP
HDA_SYNC_CODEC
HDA_BITCLK_CODEC
HDA_SDOUT_CODEC
HDA_SDATAIN0_CODEC
R271 22R2J-2-GP
HDA_SDOUT_CODEC
HDA_SDIN0
HDA_RST#_CODEC
EAPD
R54 47KR2J-2-GP
C688 SCD1U16V2ZY-2GP
DIBP
DIBN
S/PDIF
PCBEEP
LINE_OUT_L
LINE_OUT_R
MIC_L
MIC_R
CD_L
CD_GRD
CD_R
PORT-A_L
PORT-A_R
PORT-B_L
PORT-B_R
PORT-A_BIAS_L
PORT-A_BIAS_R
PORT-B_BIAS_L
PORT-B_BIAS_R
MICBIAS_L
MICBIAS_R
SENSE
VC_REFA
VREF_HI
VREF_LO
AMOM_DIBP_R
AMOM_DIBN_N
R291 0R0402-PAD
R293 0R0402-PAD
AUD_PC_BEEP
SPDIF 17,41
AUD_LOL 30
AUD_LOR 30
C689 SC470P50V2KX-3GP
MICL
MICR
CDAUD_L
CDAUD_GND
CDAUD_R
HP_OUT_L
HP_OUT_R
DK_MIC_L
DK_MIC_R
C405 DK_MICR_C
C406 DK_MICL_C
SC1U10V3ZY-6GP
MICBIAS_L 30
MICBIAS_R 30
R300 2K2R2J-2-GP
R301 2K2R2J-2-GP
MICL_AMP
MICR_AMP
AUDIO_SENSE
AUDIO_REFA
AUDIO_VREF_HI
AUDIO_VREF_LO
C411 SC10U10V5ZY-1GP
C412 SCD1U16V2ZY-2GP
C418 SC10U10V5ZY-1GP
C409 SCD1U16V2ZY-2GP
C410 SC10U10V3ZY-6GP
C413 SCD1U16V2ZY-2GP
R537 5K1R2F-2GP
R536 20KR2F-L-GP
R535 10KR2F-2GP
R534 5K1R2F-2GP
JACK_DETECT# 17
MIC_IN#
DK_MIC_IN#
3D3V_AUD_S0
MIC_INT_R
MIC_INT_L
HP_OUT_L
DK_SPKR_L
HP_OUT_R
DK_SPKR_R
EC39 SC100P50V2JN-3GP
EC40 SC100P50V2JN-3GP
EC84 SC100P50V2JN-3GP
EC82 SC100P50V2JN-3GP
EC83 SC100P50V2JN-3GP
EC81 SC100P50V2JN-3GP
5V_AUX_S5
CIR
JACK_DETECT#
3D3V_S0
EC79 SCD1U16V2ZY-2GP
EC85 SC100P50V2JN-3GP
EC21 SCD1U16V2ZY-2GP
EC41 SCD1U16V2ZY-2GP
U75
DK_MIC_IN
MIC_IN#
MIC_IN
2N7002DW-1-GP
23 CD_AUDL
23 CD_AUDR
23 CD_AGND
R282 0R0402-PAD
R290 0R0402-PAD
R288 0R0402-PAD
CDAUDL
CDAUDR
CDAGND
C402 SC1U10V3ZY-6GP
C404 SC1U10V3ZY-6GP
C403 SC1U10V3ZY-6GP
R285 47KR2J-2-GP
R292 47KR2J-2-GP
R280 47KR2J-2-GP
1025 SA
20 SB_SPKR
R274 7K5R2J-GP
C395 SCD1U16V2ZY-2GP
AUD_BEEP
AUD_PC_BEEP
4K7R2J-2-GP
R273
MICBIAS_R
R581 10KR2J-3-GP
R575 330KR2F-L-GP
U71
IN+
VSS
IN-
VDD
OUT
G1214TAUF-GP-U
MICR_C
MIC_IN
3D3V_AUD_S0
17 CIR
30 MICR_AMP
30 MICL_AMP
30 MIC_INT_R
30 MIC_INT_L
17 DK_SPKR_L
17 DK_SPKR_R
HP_OUT_L
DK_SPKR_L
HP_OUT_R
DK_SPKR_R
JACK_DETECT#
3D3V_S0
ACES-CON15-3-GP
AUD1
20.K0013.015
SCD1U25V3ZY-1GP
EC86
DY
1218
CUT MOAT
G76
GAP-CLOSE-PWR
C414 MICR
C415 MICL
R577 0R0402-PAD
R572 0R0402-PAD
MICR_C
MICL_C
MICR_C 30
MICL_C 30
C696 DK_MIC_R_C
C695 DK_MIC_L_C
DK_MIC_R_CN
DK_MIC_L_CN
DK_MIC_R_CN 17
DK_MIC_L_CN 17
RN73
DK_MIC_R_C
DK_MIC_L_C
DK_MICR_C
DK_MICL_C
SRN10KJ-GP
R551 1KR2J-1-GP
R552 1KR2J-1-GP
Put near Codec
R588 10KR2J-3-GP
R590 47KR2J-2-GP
C745 SCD1U16V2ZY-2GP
DK_MIC_IN
DK_MIC_R_CN
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC CX20549-12Z
Size A3
Document Number
Pamirs-Discrete
Rev SA
Date: Monday, December 18, 2006
Sheet 29 of 47


31 EC_BEEP
C721
SC1U10V3ZY-6GP
R570
47KR2J-2-GP
R307
29 AUD_LOL
C419
L_LINE_IN_1
1KR2J-1-GP
L_LINE_IN
R302
DUMMY-R2
AUD_AGND
5V_S0
5VA_OP_S0
G52
GAP-CLOSE-PWR
R580
100KR2J-1-GP
U53
VDD
PVDD
GAIN0
GAIN1
LOUT+
LOUT-
RIN+
RIN-
NC#12
SHUTDOWN#
BYPASS
LIN+
LIN-
ROUT+
ROUT-
GND
G1431F2U-GP
C421
C422
SC4D7U10V5ZY-3GP
R578 0R2J-2-GP
R566 10KR2J-3-GP
DY
R574 0R2J-2-GP
R573 0R2J-2-GP
C425
SPKR_L+
SPKR_L-
RIN+
R_LINE_IN
C428
C426
BYPASS
LIN+
L_LINE_IN
SPKR_R+
SPKR_R-
KBC_MUTE# 31
Q32
2N7002-11-GP
EAPD 29,31,32
31 EC_BEEP
C720
R568
47KR2J-2-GP
29 AUD_LOR
C420
R_LINE_IN_1
R306
1KR2J-1-GP
R_LINE_IN
R304
DUMMY-R2
29 MICBIAS_R
C736
SC100P50V2JN-3GP
3D3V_AUD_S0
C741
SCD1U16V2ZY-2GP
U73
IN+
VSS
IN-
VDD
OUT
G1214TAUF-GP-U
29 MICR_AMP
C722
SCD22U16V3ZY-GP
R586
10KR2J-3-GP
C727
DUMMY-C2
C729
SC680P-GP
R587
100KR2J-1-GP
MICR_C 29
RC1
SPKR_R+
SPKR_R-
SPKR_L+
SPKR_L-
SRC100P50V2-GP
EC68
EC67
MIC_INT_R
MIC_INT_L
SC100P50V2JN-3GP
MIC1
ACES-CON4-1-GP
20.D0197.104
R439
0R2J-2-GP
29 MICBIAS_L
C733
U72
C718
SCD22U16V3ZY-GP
R583
10KR2J-3-GP
C725
C726
R582
MICL_C 29
Speaker
SPKR_L-
SPKR_L+
SPKR_R-
SPKR_R+
ACES-CON4-1-GP
SPKR1
20.D0197.104
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO AMP/SPEAKER
Size A3
Document Number
Pamirs-Discrete
Rev SA
Date: Monday, November 27, 2006
Sheet 30 of 47


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
KB3910SF-2-GP
X-32D768KHZ-40GPU
SC15P50V2JN-2-GP
U42
Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
SE: 1,0,0
-1: 1,0,1
Pull-up by devided-resistor to MAX8725_LDO
ICH8 integrated pull-up
Add Label "VCC"
Add Label "TXD"
Add Label "RXD"
0126
0110
1218
DY
Intel checklist suggest no external resistor needed
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_ENE K3910SF
Pamirs-Discrete
Size A3
Document Number
Rev SA
Date: Tuesday, December 19, 2006
Sheet 31 of 47

CAMERA

Blue thumb

Internal KeyBoard Connector

31 KROW[1..8]
31 KCOL[1..16]

KB1
ACES-CON24-2-GP
20.K0220.024

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

TouchPad Connector

SA 1011

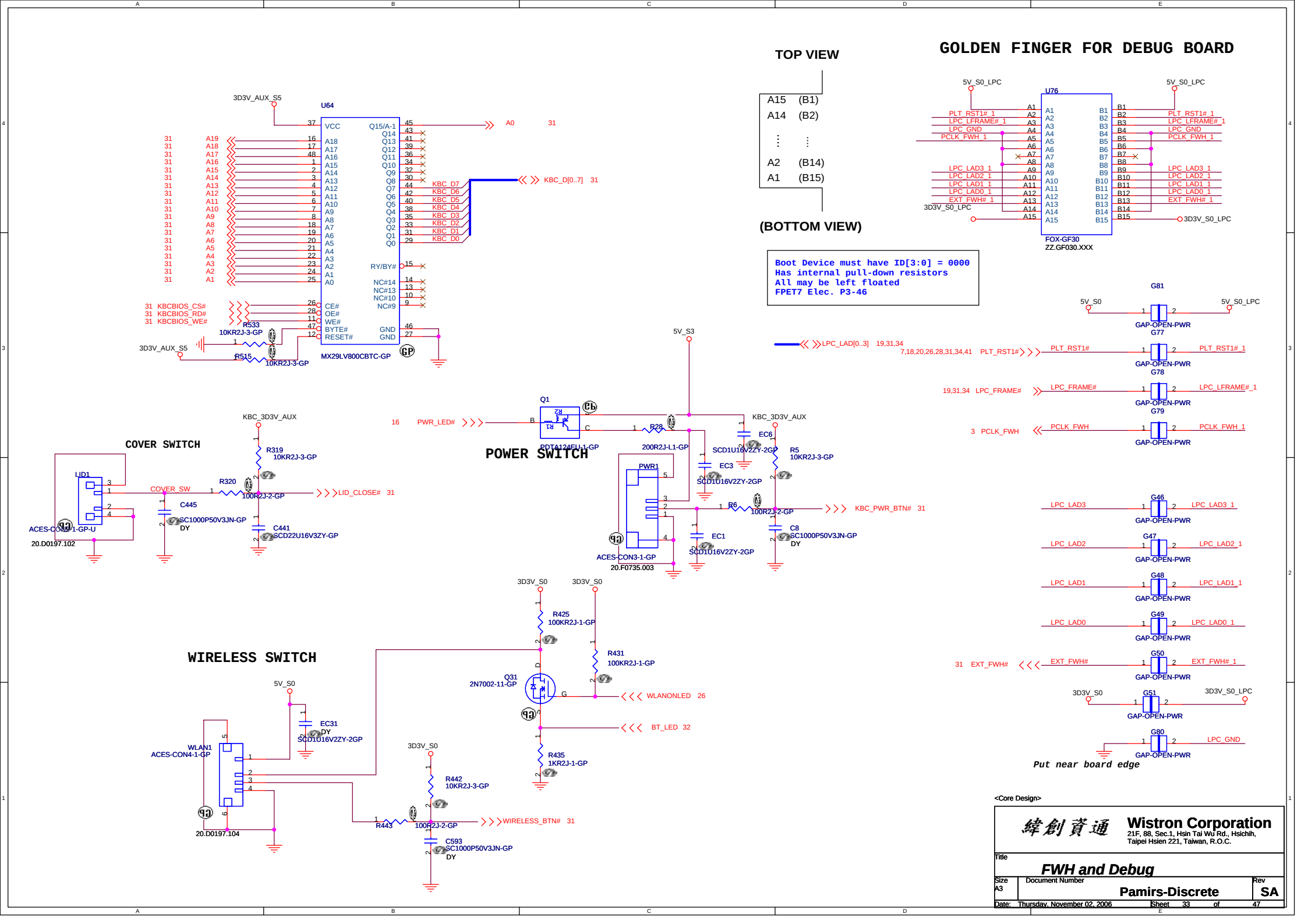
TOUCH-PAD SWITCH

CAPACITY BUTTON

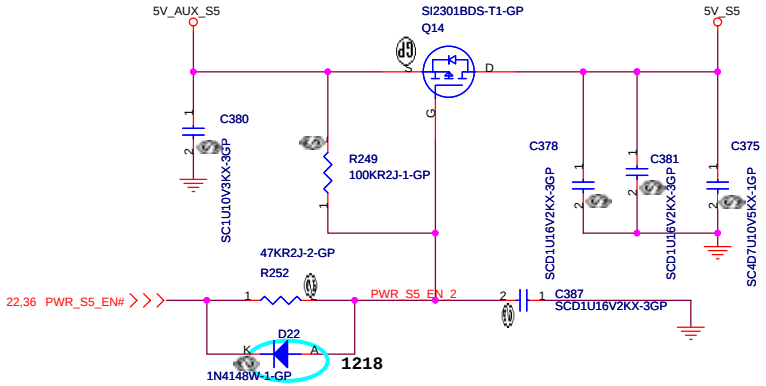
Close to CN8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

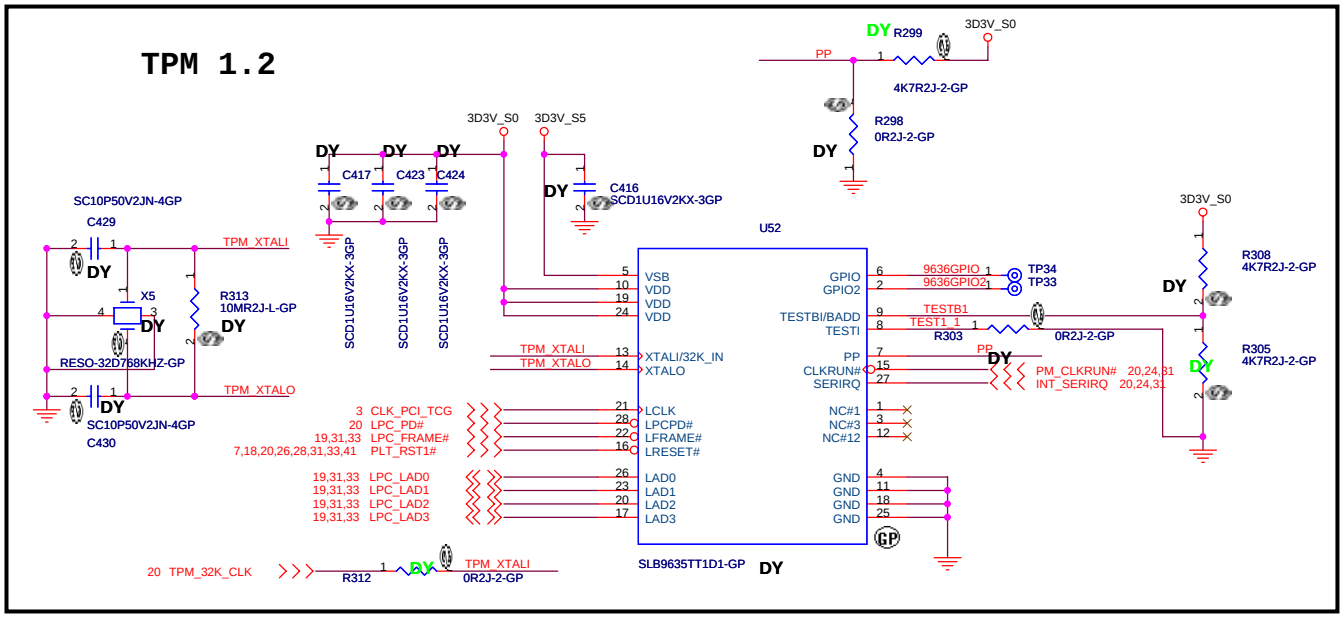
Title: KeyBoard-CONN
Size: A3
Document Number: Pamirs-Discrete
Rev: SA
Date: Monday, December 18, 2006
Sheet 32 of 47


TOP VIEW
A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)
(BOTTOM VIEW)
GOLDEN FINGER FOR DEBUG BOARD
U76
FOX-GF30
ZZ.GF030.XXX
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46
U64
MX29LV800CBTC-GP
COVER SWITCH
POWER SWITCH
WIRELESS SWITCH
Put near board edge
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
FWH and Debug
Pamirs-Discrete
Thursday, November 02, 2006

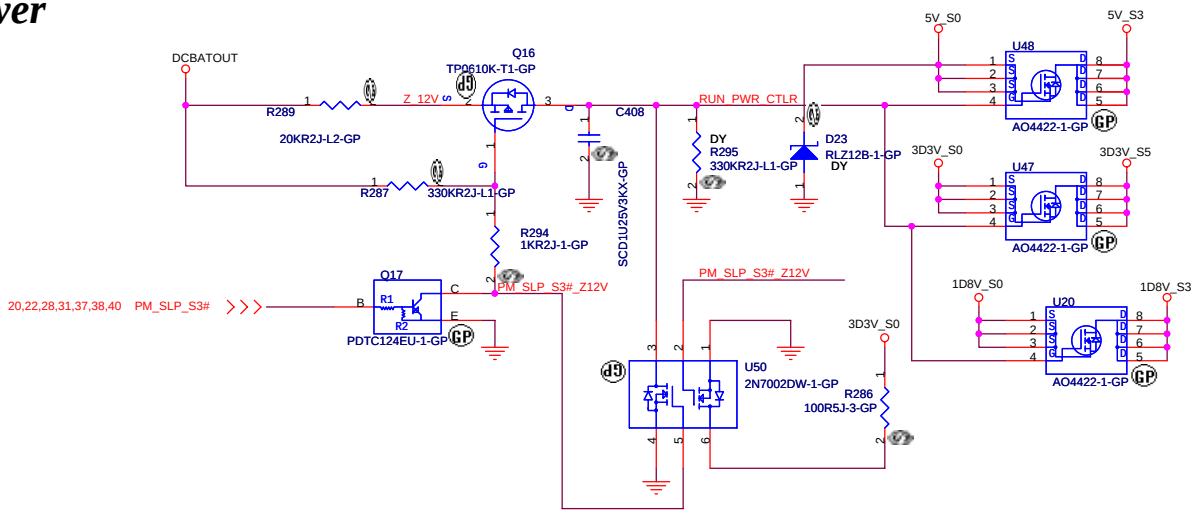
5V_AUX_S5 TO 5V_S5



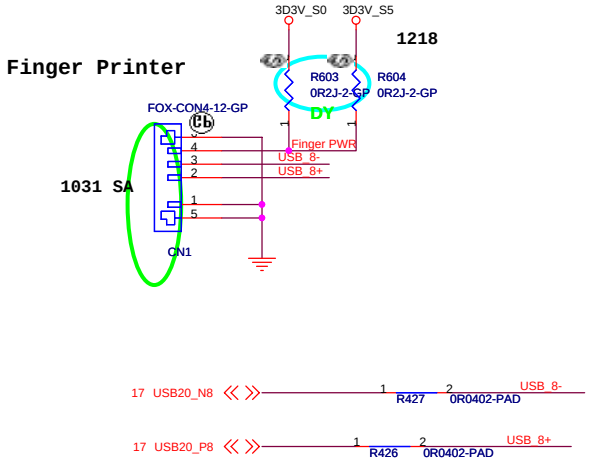
TPM 1.2



Run Power



Finger Printer



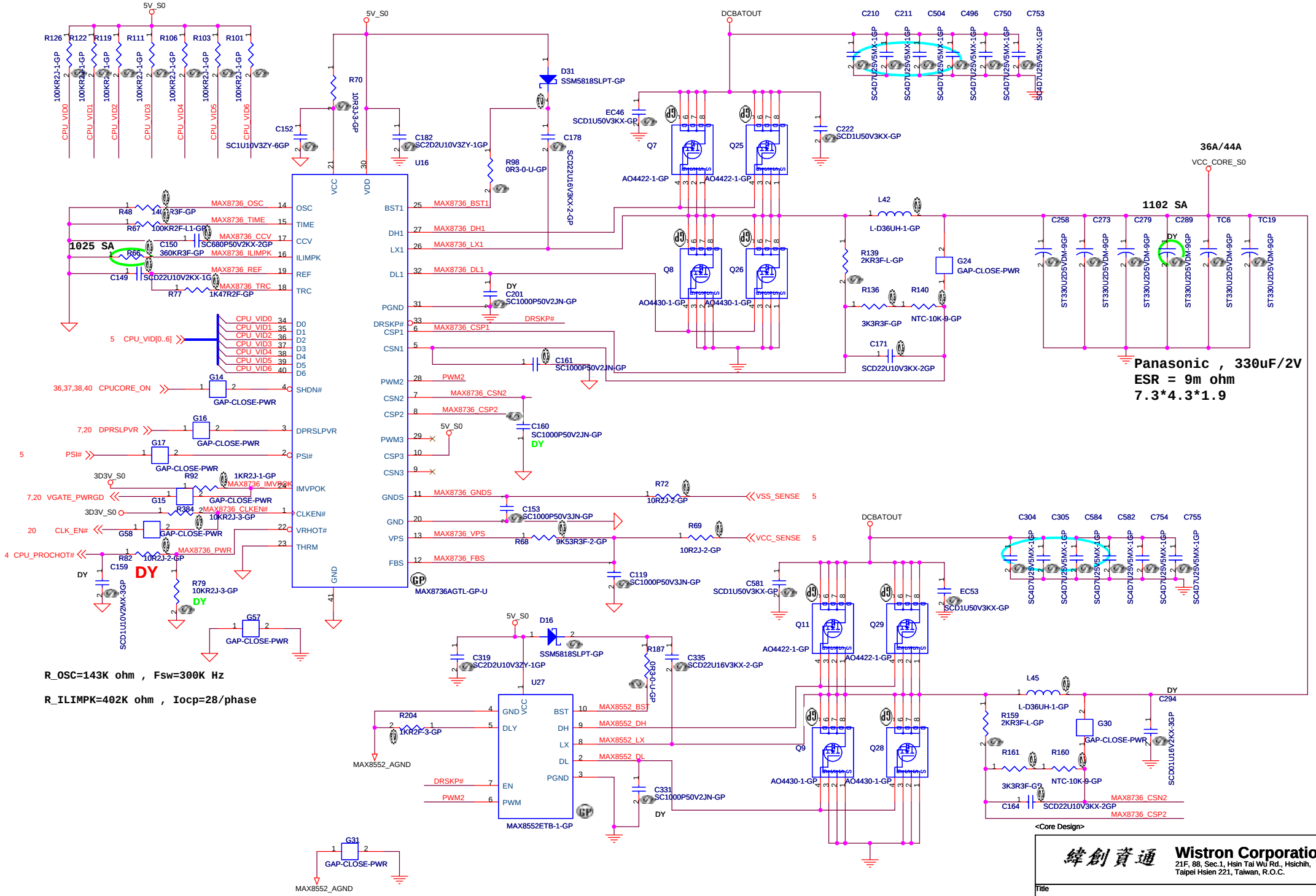
<Core Design>

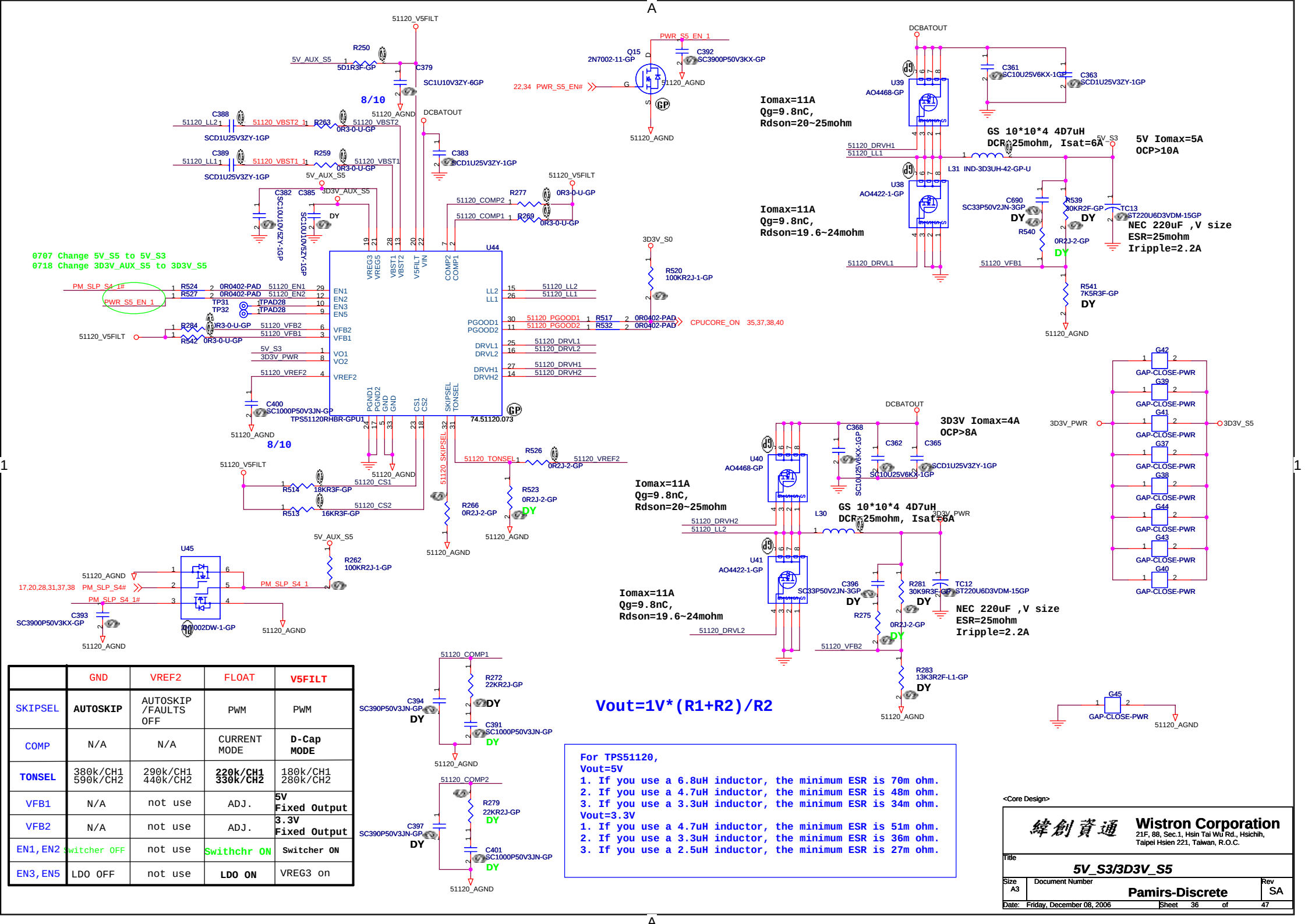
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PWRPLANE&RESETLOGIC**

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Monday, December 18, 2006 Sheet 34 of 47


1025 SA
1102 SA
36A/44A
DY
Panasonic , 330uF/2V
ESR = 9m ohm
7.3*4.3*1.9
R_OSC=143K ohm , Fsw=300K Hz
R_ILIMPK=402K ohm , Iocp=28/phase
MAX8736AGTL-GP-U
MAX8552ETB-1-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC-DC VCCCPUCORE
Size A3
Document Number
Pamirs-Discrete
Rev SA
Date: Wednesday, December 13, 2006
Sheet 35 of 47



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V_S3/3D3V_S5

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Friday, December 08, 2006 Sheet 36 of 47

Iocp=7.0 2 = 14A*
Rds,on=17m ohm
*Vcs1=Iocp*Rds,on=238mV*
VILIM=Vcs1/0.1=2.38V

*Iocp=7.0*2 = 14A*
Rds,on=17m ohm
*Vcs2=Iocp*Rds,on=28mV*
VILIM2=Vcs2/0.1=2.38V

1D8V / 7.0A
OCP>=14A

1D05V_S0/5A
OCP>=10A

5V_S5 R215 DUMMY-R2 5V_MAX8743_VCC
5V_S3 R217
0R3-0-U-GP

1D8V_S3 1D8V_PWR
G63 G62 G66 G65 G64 G67 G61 G68 GAP-CLOSE-PWR

DCBATOUT
C359 SC10U25V6KX-1GP
EC72 SCD1U25V3ZY-1GP
U33 AO4468-GP

NEC
Irms=7.5A(Isat=10.4A)
DCR=13mohm
12*12*5.5
1102 SA
L26
EC113 SE220U2D5VDM-3GP
TC11 SE220U2D5VDM-3GP
C339 SCD1U25V3ZY-1GP
DY SCD1U25V3ZY-2GP

U34 AO4712-GP
Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

Panasonic 220uF/2D5V
ESR=15m ohm
Iripple=2.7 A

R224 8K2R3F-GP
R225 9K53R2F-GP
Voutsetting=1.820V

5V_MAX8743_VCC
C341 SCD1U10V2MX-3GP
C340 SC1U10V3ZY-6GP
C353 SCD1U10V2MX-3GP
C349 SC1U25V5ZY-4GP
DCBATOUT

D17 BAW56-3-GP
R218
MAX8743_BST2
MAX8743_VCC
R429 R212
C350 SC1U10V3ZY-6GP
R221 0R3-0-U-GP
R432 90K9R3F-GP
R208 90K9R3F-GP
R456 0R3-0-U-GP
C352 SCD1U25V3ZY-1GP
C338 SCD1U25V3ZY-1GP

U29 MAX8743EEI-1-GP
74.08743.A79
UVP VCC VDD V+
ILIM1 BST1 DH1 LX1 DL1 CS1
ILIM2 BST2 DH2 LX2 DL2 CS2
OUT1 FB1 ON1 TON REF SKIP#
OUT2 FB2 ON2 PGOOD OVP GND

MAX8743_ILIM1 MAX8743_BST1R MAX8743_DH1 MAX8743_LX1 MAX8743_DL1
MAX8743_ILIM2 MAX8743_BST2R MAX8743_DH2 MAX8743_LX2 MAX8743_DL2
MAX8743_ON1 MAX8743_TON MAX8743_VREF MAX8743_ON2 MAX8743_PGOOD
MAX8743_FB1 MAX8743_FB2

C590 C589 SCD47U10V3KX-3GP
DY SCD1U25V3ZY-1GP

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm
U37 AO4468-GP
U36 AO4712-GP

NEC
Irms=7.5A(Isat=10.4A)
DCR=13mohm
12*12*5.5

EC77 SCD1U25V3ZY-1GP
C358
C356 SC10U25V6KX-1GP
SC10U25V6KX-1GP

1D05V_PWR 1D05V_S0
G34 G32 G33 G36 G35 GAP-CLOSE-PWR
L27
DY C336 SCD1U25V3ZY-1GP
TC10 SE220U2VDM-8GP

Panasonic 220uF/2V
ESR=15m ohm
Iripple=2.7 A

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

10KR2F-2-GP R205
R207 100KR3F-GP
Voutsetting=1.0511V

Vout=Vfb*(1+(R1/R2))
Where Vfb=1.0V,R2=10Kohm

17,20,28,31,36,38 PM_SLP_S4# R213 5K1R2-GP MAX8743_ON1
20,22,28,31,34,38,40 PM_SLP_S3# R210 5K1R2-GP MAX8743_ON2
DY C346 SCD1U10V2MX-3GP
DY C591 SCD1U10V2MX-3GP

5V_MAX8743_VCC
R434 0R2J-2-GP DY
MAX8743_VREF
R433 DUMMY-R2
R440 DUMMY-R2

0205
PM_SLP_S3# R211 220KR2J-L2-GP
DY R214
PM_SLP_S4# 220KR2J-L2-GP
MAX8743_SKIP#
C344 SC1000P50V3JN-GP DY
R216 0R2J-2-GP

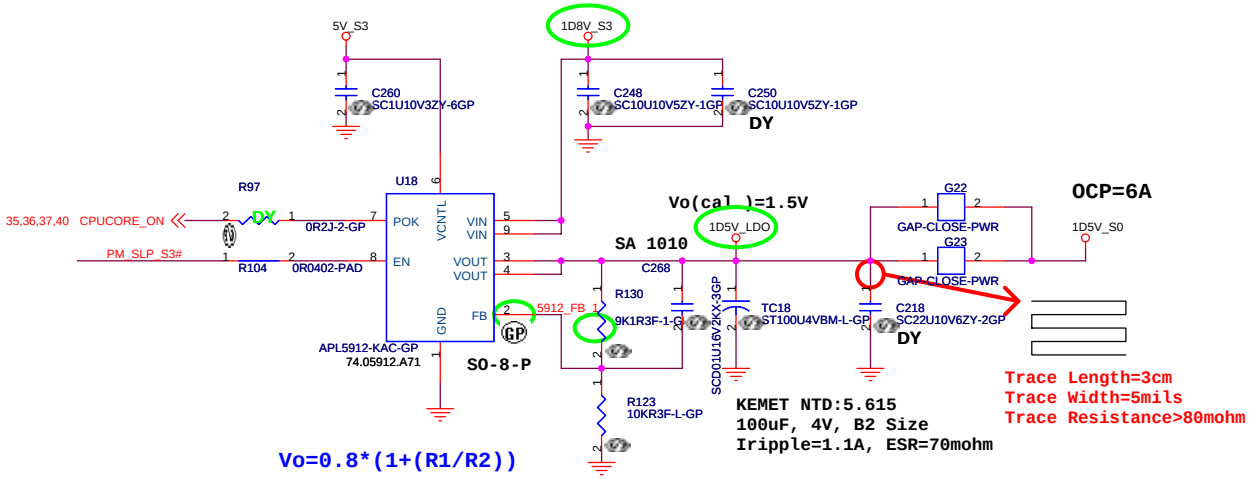
MAX8743_PGOOD
R441 0R0402-PAD
CPUCORE_ON 35,36,38,40

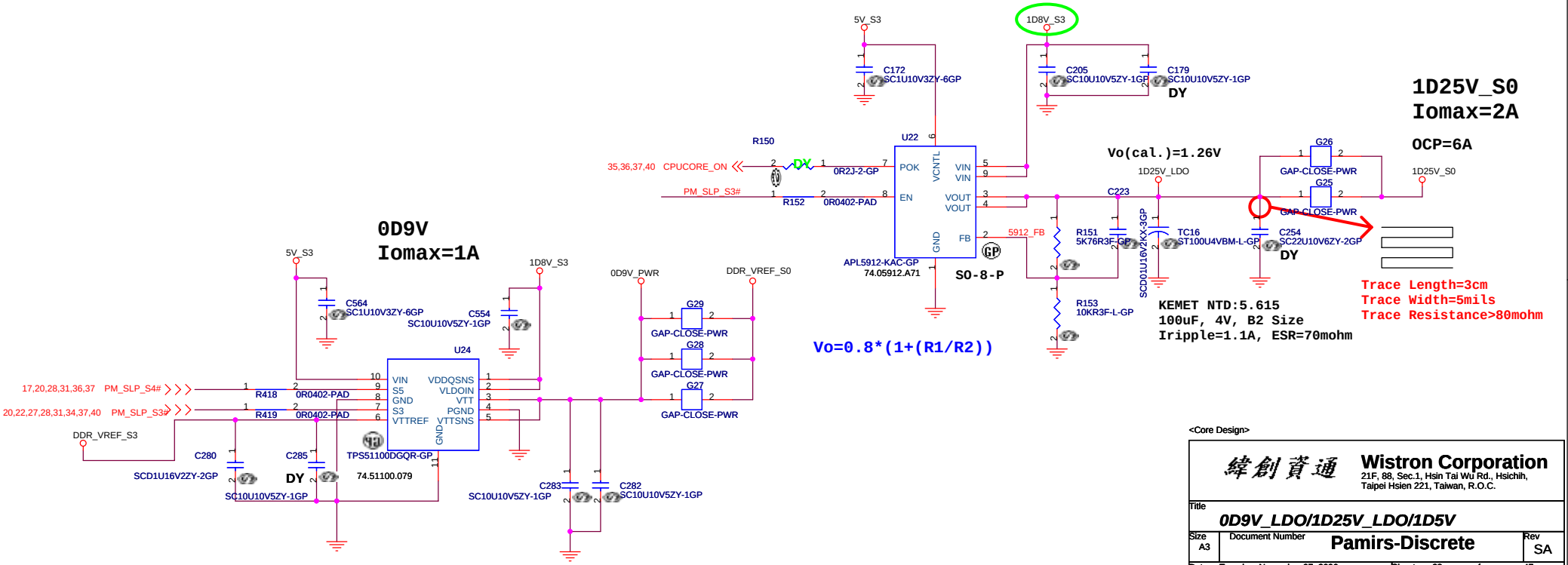
Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *1D8V_S3/1D05V_S0*
Size: A3 | Document Number: **Pamirs-Discrete** | Rev: SA
Date: Monday, December 18, 2006 | Sheet 37 of 47





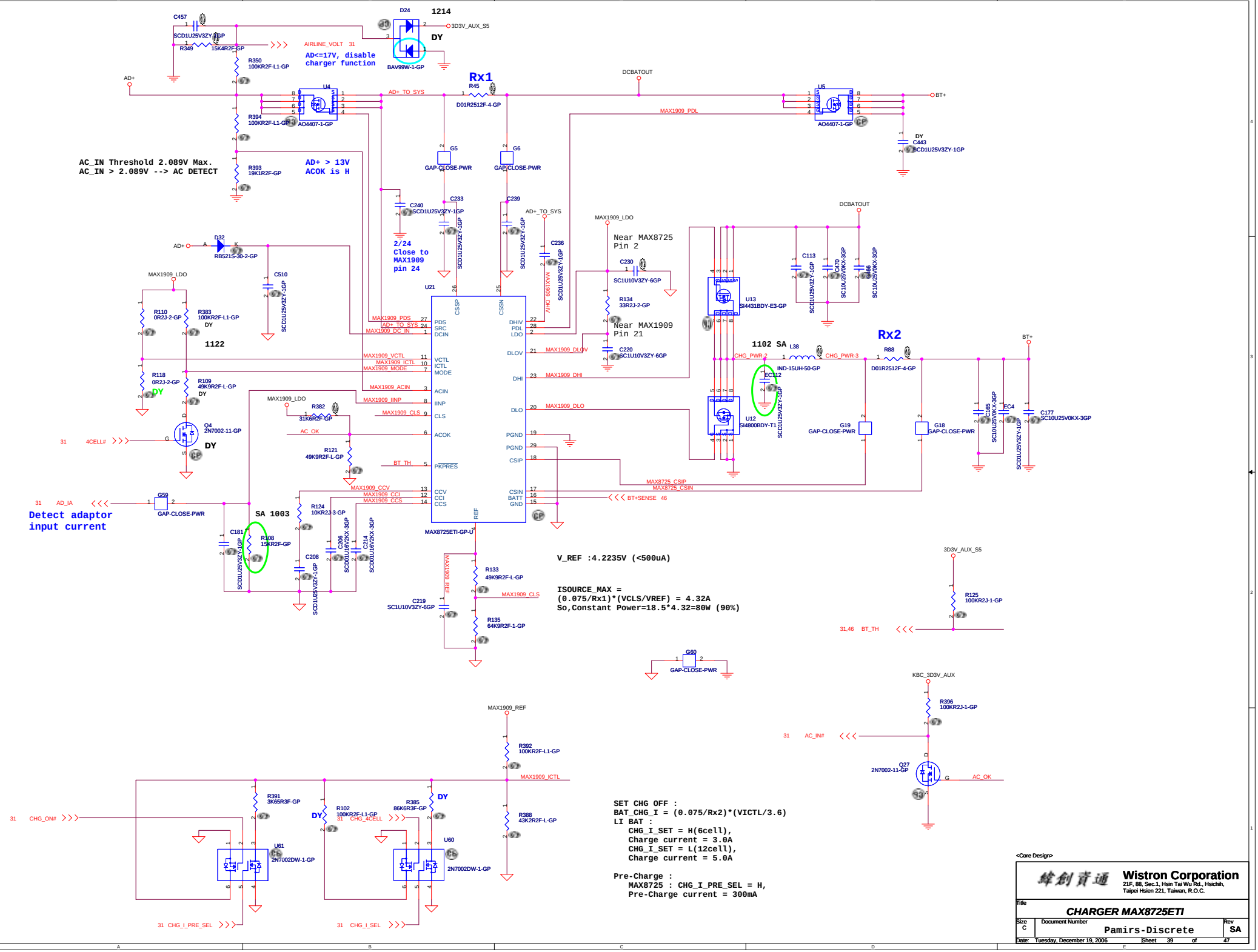
<Core Design>

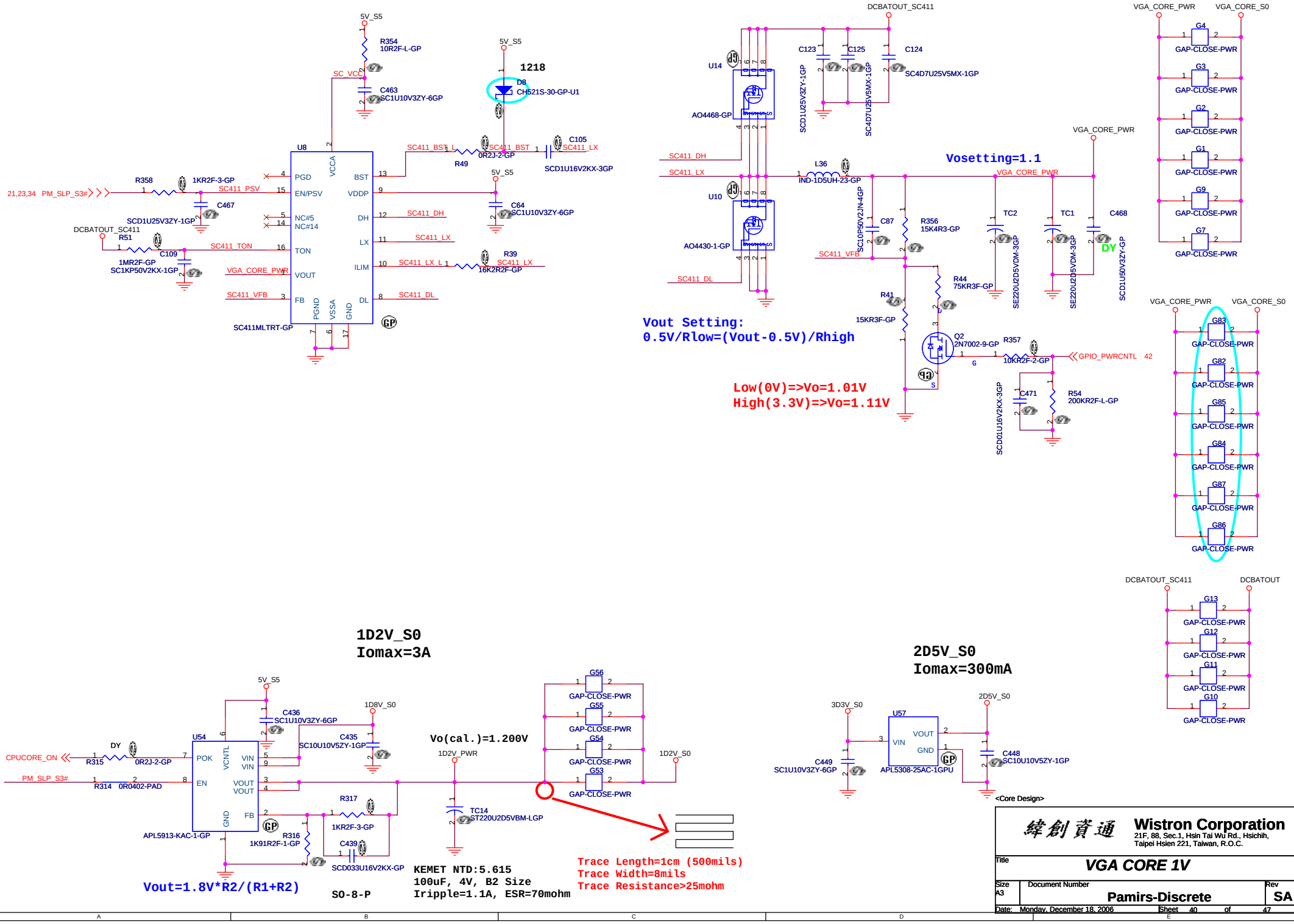
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

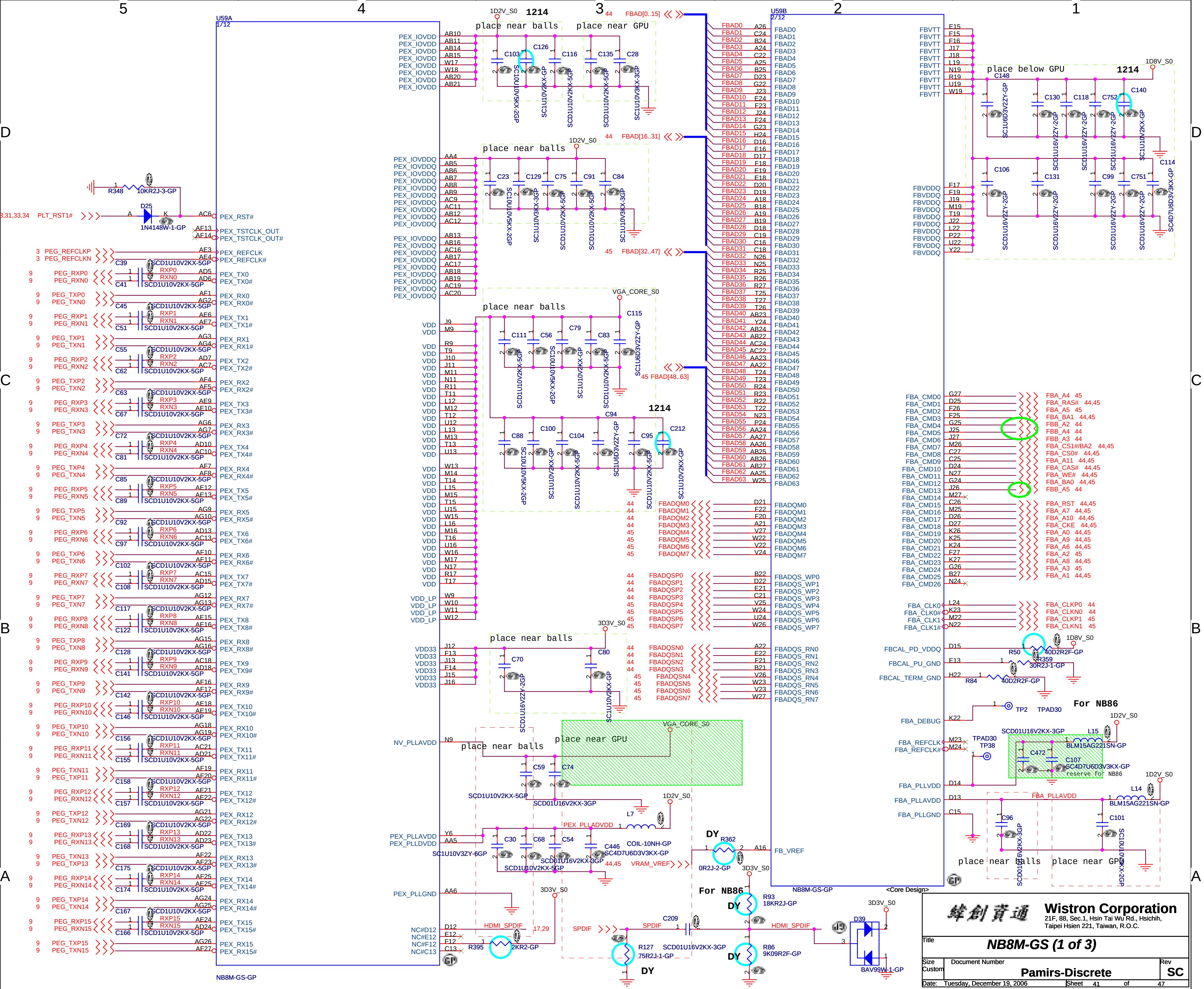
Title: 0D9V_LDO/1D25V_LDO/1D5V

Size: A3 | Document Number: Pamirs-Discrete | Rev: SA

Date: Tuesday, November 07, 2006 | Sheet 38 of 47

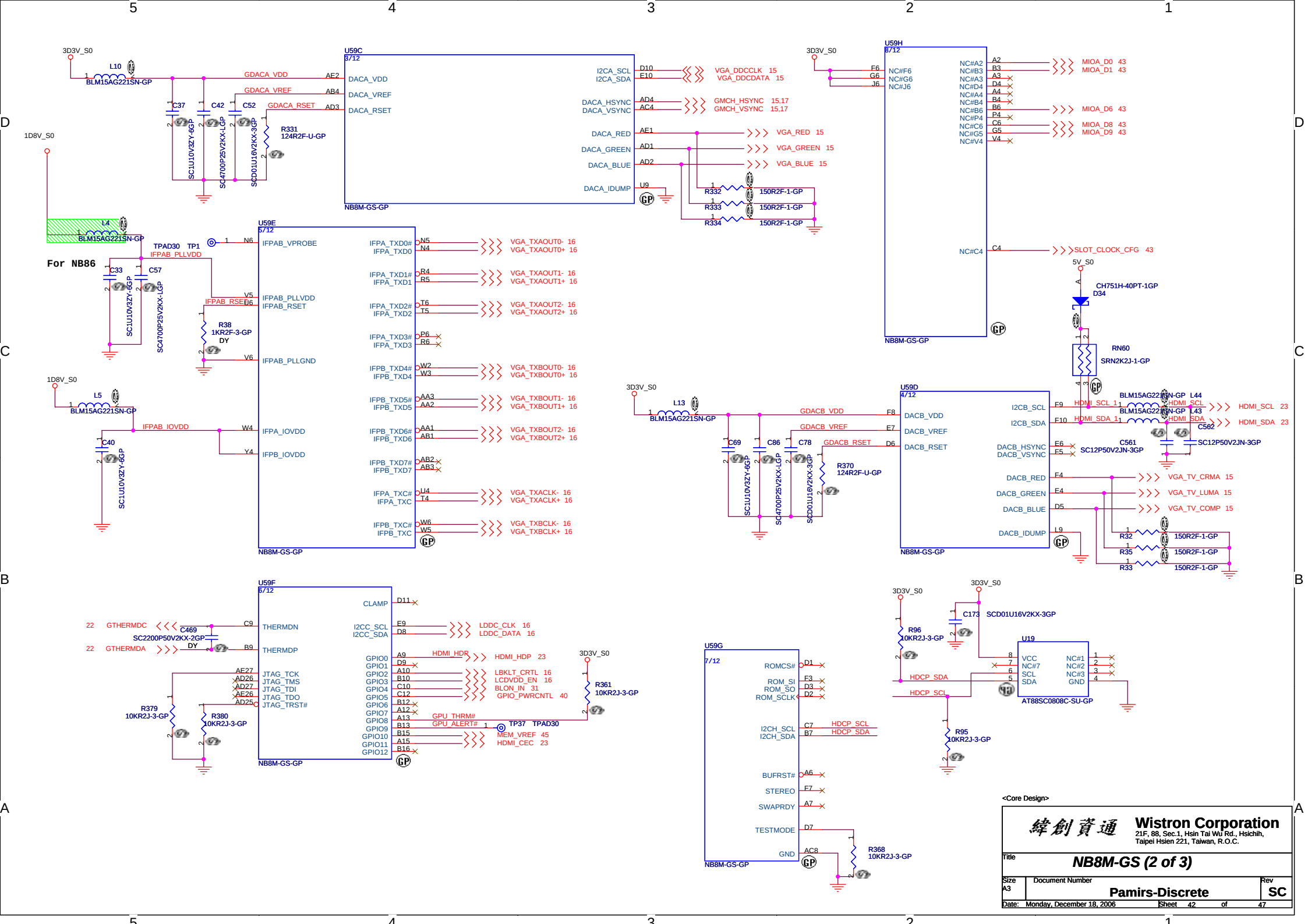

AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
AD+ > 13V
ACOK is H
AD<=17V, disable
charger function
Rx1
Rx2
1214
1122
1102 SA
SA 1003
2/24
Close to
MAX1909
pin 24
Near MAX8725
Pin 2
Near MAX1909
Pin 21
Detect adaptor
input current
V_REF :4.2235V (<500uA)
ISOURCE_MAX =
(0.075/Rx1)*(VCLS/VREF) = 4.32A
So,Constant Power=18.5*4.32=80W (90%)
SET CHG OFF :
BAT_CHG_I = (0.075/Rx2)*(VICTL/3.6)
LI BAT :
CHG_I_SET = H(6cell),
Charge current = 3.0A
CHG_I_SET = L(12cell),
Charge current = 5.0A
Pre-Charge :
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 300mA
MAX8725ETI-GP-U
AD+
DCBATOUT
BT+
3D3V_AUX_S5
KBC_3D3V_AUX
MAX1909_LDO
MAX1909_REF
AO4407-1-GP
D01R2512F-4-GP
IND-15UH-50-GP
SI4431BDY-E3-GP
SI4800BDY-T1
2N7002-11-GP
2N7002DW-1-GP
BAV99W-1-GP
RB521S-30-2-GP
GAP-CLOSE-PWR
SC1U10V3ZY-6GP
SCD1U25V3ZY-1GP
SC10U25V0KX-3GP
SCD1U25V2ZY-1GP
SCD1U16V2KX-3GP
AD_IA
4CELL#
AC_OK
AC_IN#
CHG_ON#
CHG_4CELL
CHG_I_PRE_SEL
CHG_I_SEL
BT+SENSE 46
BT_TH 31,46
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8725ETI
Pamirs-Discrete
Tuesday, December 19, 2006
Sheet 39 of 47


5V_S5
R354
10R2F-L-GP
SC_VCC
C463
SC1U10V3ZY-6GP
1218
D8
CH521S-30-GP-U1
U8
PGD
EN/PSV
NC#5
NC#14
TON
VOUT
FB
VCCA
PGND
VSSA
GND
BST
VDDP
DH
LX
ILIM
DL
SC411MLTRT-GP
SC411_BST_L
R49
0R2J-2-GP
SC411_BST
C105
SC411_LX
SCD1U16V2KX-3GP
R358
1KR2F-3-GP
21,23,34 PM_SLP_S3#
SC411_PSV
C467
SCD1U25V3ZY-1GP
DCBATOUT_SC411
R51
C109
1MR2F-GP
SC1KP50V2KX-1GP
SC411_TON
VGA_CORE_PWR
SC411_VFB
SC411_DH
SC411_LX
SC411_LX_L
R39
16K2R2F-GP
SC411_DL
C64
SC1U10V3ZY-6GP
DCBATOUT_SC411
U14
AO4468-GP
U10
AO4430-1-GP
C123
C125
C124
SC4D7U25V5MX-1GP
SCD1U25V3ZY-1GP
SC4D7U25V5MX-1GP
SC411_DH
SC411_LX
SC411_DL
L36
IND-1D5UH-23-GP
VGA_CORE_PWR
Vosetting=1.1
C87
SC10P50V2JN-4GP
R356
15K4R3-GP
SC411_VFB
R41
15KR3F-GP
R44
75KR3F-GP
TC2
TC1
C468
DY
SE220U2D5VDM-3GP
SE220U2D5VDM-3GP
SCD1U50V3ZY-GP
Q2
2N7002-9-GP
R357
10KR2F-2-GP
GPIO_PWRCNTL 42
C471
R54
200KR2F-L-GP
SCD01U16V2KX-3GP
Vout Setting:
0.5V/Rlow=(Vout-0.5V)/Rhigh
Low(0V)=>Vo=1.01V
High(3.3V)=>Vo=1.11V
VGA_CORE_PWR
VGA_CORE_S0
G4
G3
G2
G1
G9
G7
GAP-CLOSE-PWR
G83
G82
G85
G84
G87
G86
DCBATOUT_SC411
DCBATOUT
G13
G12
G11
G10
1D2V_S0
Iomax=3A
5V_S5
C436
SC1U10V3ZY-6GP
C435
SC10U10V5ZY-1GP
1D8V_S0
U54
DY
35,36,37,38 CPUCORE_ON
R315
0R2J-2-GP
PM_SLP_S3#
R314
0R0402-PAD
POK
EN
VCNTL
VIN
VOUT
GND
FB
APL5913-KAC-1-GP
R317
1KR2F-3-GP
R316
1K91R2F-1-GP
C439
SCD033U16V2KX-GP
Vo(cal.)=1.200V
1D2V_PWR
TC14
ST220U2D5VBM-LGP
1D2V_S0
G56
G55
G54
G53
GAP-CLOSE-PWR
Vout=1.8V*R2/(R1+R2)
SO-8-P
KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm
Trace Length=1cm (500mils)
Trace Width=8mils
Trace Resistance>25mohm
2D5V_S0
Iomax=300mA
3D3V_S0
U57
VIN
VOUT
GND
APL5308-25AC-1GPU
C449
SC1U10V3ZY-6GP
2D5V_S0
C448
SC10U10V5ZY-1GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA CORE 1V
Size
A3
Document Number
Pamirs-Discrete
Rev
SA
Date: Monday, December 18, 2006
Sheet 40 of 47



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	NB8M-GS (1 of 3)	
Size: Custom	Document Number: Pamirs-Discrete	Rev: SC
Date: Tuesday, December 19, 2006	Sheet 41 of 47	


U59C
3/12
NB8M-GS-GP
GDACA_VDD
GDACA_VREF
GDACA_RSET
DACA_VDD
DACA_VREF
DACA_RSET
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_IDUMP
I2CA_SCL
I2CA_SDA
VGA_DDCCLK 15
VGA_DDCDATA 15
GMCH_HSYNC 15,17
GMCH_VSYNC 15,17
VGA_RED 15
VGA_GREEN 15
VGA_BLUE 15
U59H
8/12
U59E
5/12
IFPAB_VPROBE
IFPAB_PLLVDD
IFPAB_RSET
IFPAB_PLLGND
IFPA_IOVDD
IFPB_IOVDD
IFPA_TXD0#
IFPA_TXD0
IFPA_TXD1#
IFPA_TXD1
IFPA_TXD2#
IFPA_TXD2
IFPA_TXD3#
IFPA_TXD3
IFPB_TXD4#
IFPB_TXD4
IFPB_TXD5#
IFPB_TXD5
IFPB_TXD6#
IFPB_TXD6
IFPB_TXD7#
IFPB_TXD7
IFPA_TXC#
IFPA_TXC
IFPB_TXC#
IFPB_TXC
VGA_TXAOUT0- 16
VGA_TXAOUT0+ 16
VGA_TXAOUT1- 16
VGA_TXAOUT1+ 16
VGA_TXAOUT2- 16
VGA_TXAOUT2+ 16
VGA_TXBOUT0- 16
VGA_TXBOUT0+ 16
VGA_TXBOUT1- 16
VGA_TXBOUT1+ 16
VGA_TXBOUT2- 16
VGA_TXBOUT2+ 16
VGA_TXACLK- 16
VGA_TXACLK+ 16
VGA_TXBCLK- 16
VGA_TXBCLK+ 16
For NB86
U59D
4/12
DACB_VDD
DACB_VREF
DACB_RSET
DACB_HSYNC
DACB_VSYNC
DACB_RED
DACB_GREEN
DACB_BLUE
DACB_IDUMP
I2CB_SCL
I2CB_SDA
HDMI_SCL 23
HDMI_SDA 23
VGA_TV_CRMA 15
VGA_TV_LUMA 15
VGA_TV_COMP 15
U59F
6/12
THERMDN
THERMDP
CLAMP
I2CC_SCL
I2CC_SDA
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST#
HDMI_HDR
LDDC_CLK 16
LDDC_DATA 16
HDMI_HDP 23
LBKLT_CRTL 16
LCDVDD_EN 16
BLON_IN 31
GPIO_PWRCNTL 40
GPU_THRM#
GPU_ALERT#
MEM_VREF 45
HDMI_CEC 23
U59G
7/12
ROMCS#
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST#
STEREO
SWAPRDY
TESTMODE
GND
HDCP_SCL
HDCP_SDA
U19
AT88SC0808C-SU-GP
SLOT_CLOCK_CFG 43
MIOA_D0 43
MIOA_D1 43
MIOA_D6 43
MIOA_D8 43
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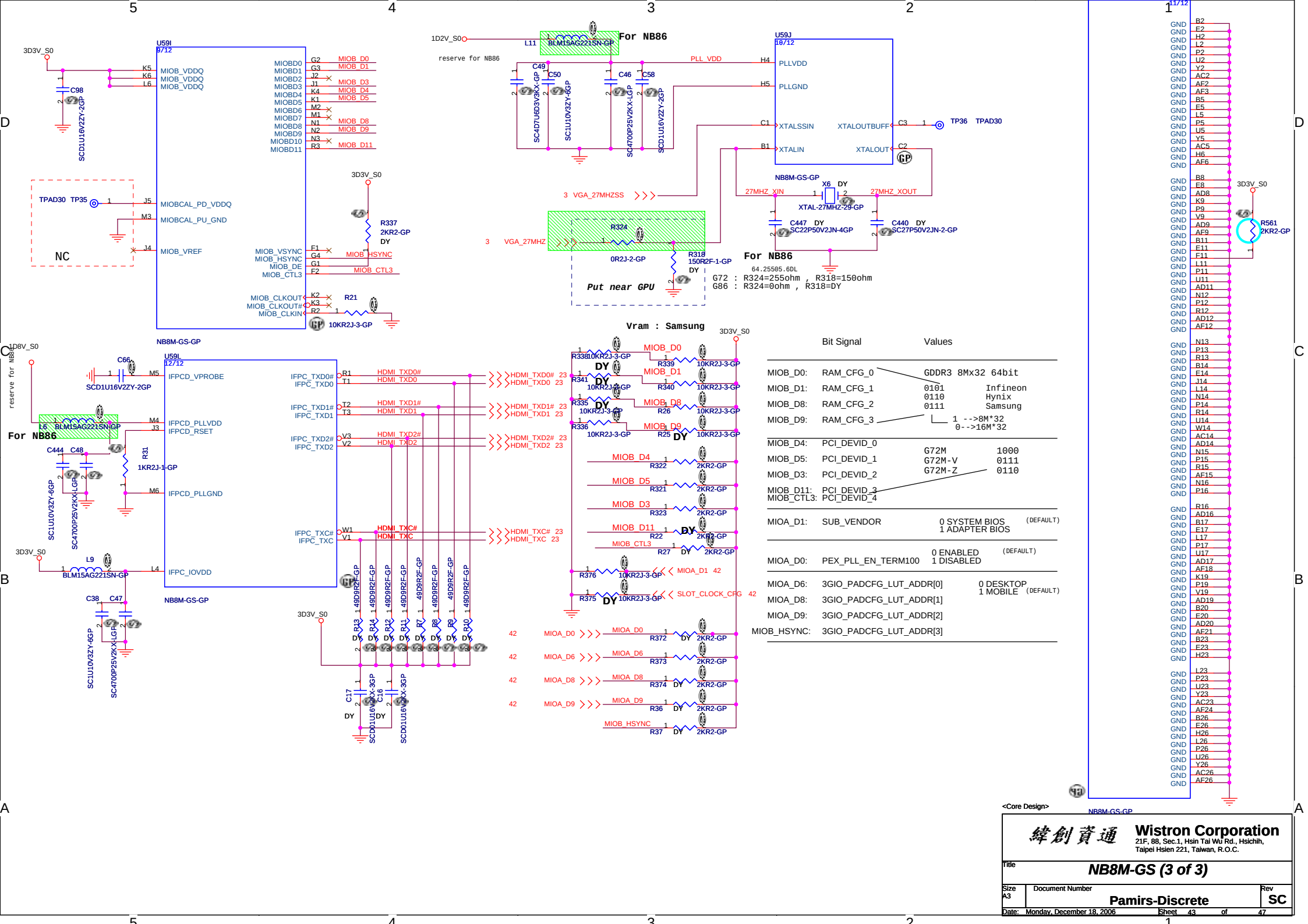

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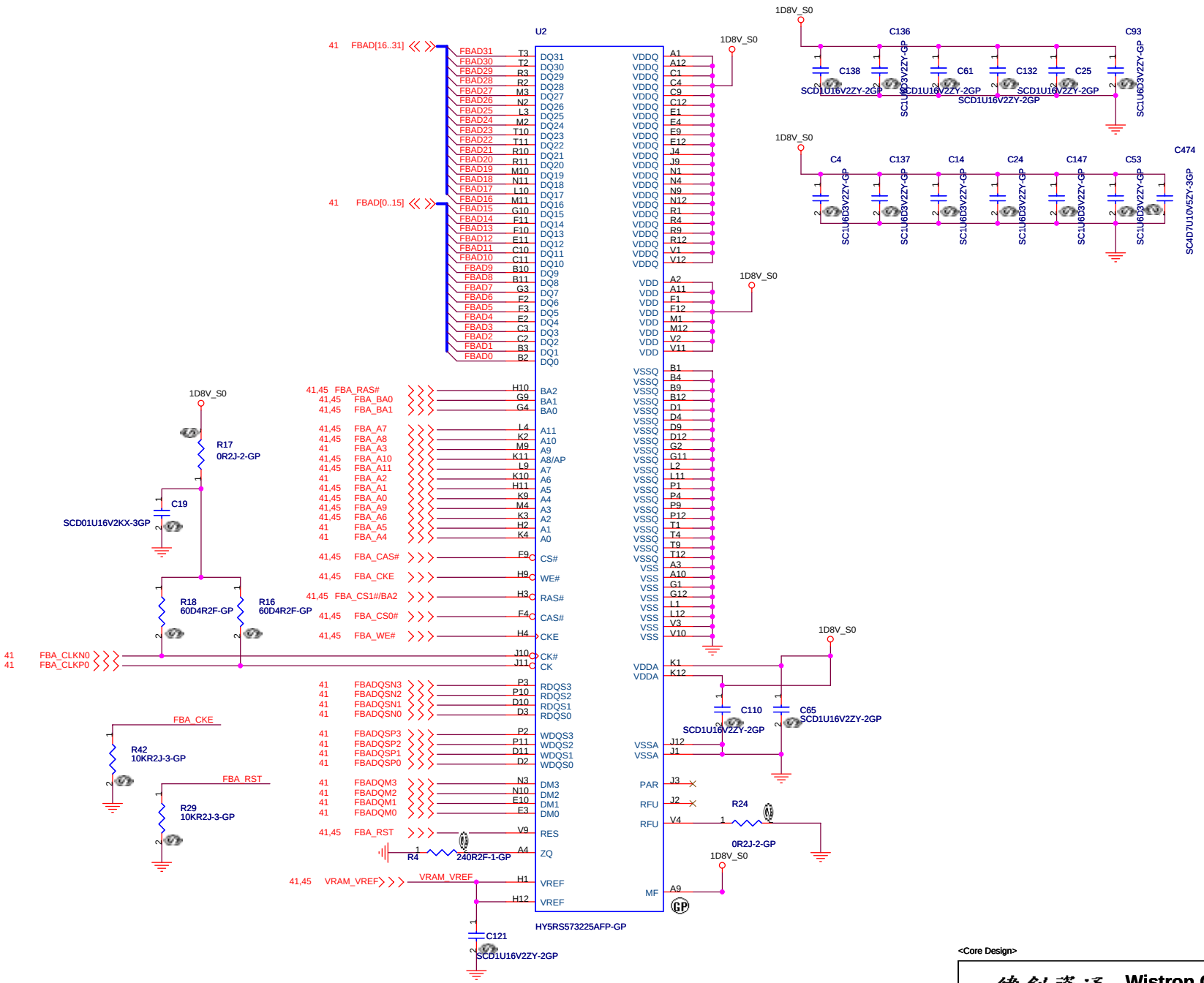

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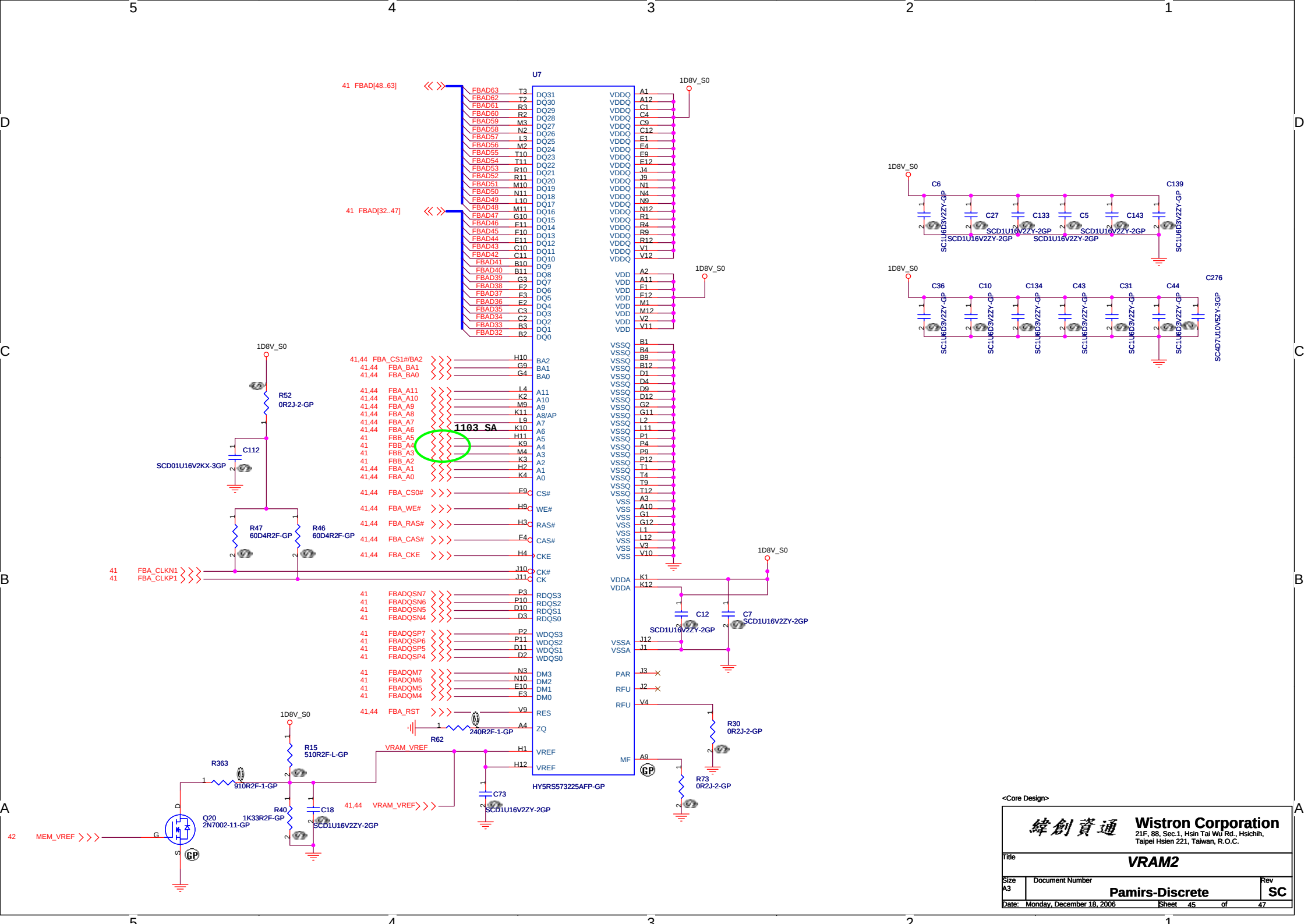
U7
HY5RS573225AFP-GP
1103 SA
1D8V_S0
R52
0R2J-2-GP
C112
SCD01U16V2KX-3GP
R47
60D4R2F-GP
R46
60D4R2F-GP
R62
240R2F-1-GP
R15
510R2F-L-GP
R363
910R2F-1-GP
R40
1K33R2F-GP
C18
SCD1U16V2ZY-2GP
Q20
2N7002-11-GP
C73
SCD1U16V2ZY-2GP
C12
C7
SCD1U16V2ZY-2GP
R30
0R2J-2-GP
R73
0R2J-2-GP
C6
C139
C27
C133
C5
C143
SC1U6D3V2ZY-GP
SCD1U16V2ZY-2GP
C36
C10
C134
C43
C31
C44
C276
SC4D7U10V5ZY-3GP
VRAM_VREF
MEM_VREF
FBAD[48..63]
FBAD[32..47]
FBA_CLKN1
FBA_CLKP1
FBA_RST
FBA_CS0#
FBA_WE#
FBA_RAS#
FBA_CAS#
FBA_CKE
FBA_CS1#/BA2
FBA_BA1
FBA_BA0
FBA_A11
FBA_A10
FBA_A9
FBA_A8
FBA_A7
FBA_A6
FBB_A5
FBB_A4
FBB_A3
FBB_A2
FBA_A1
FBA_A0
FBADQSN7
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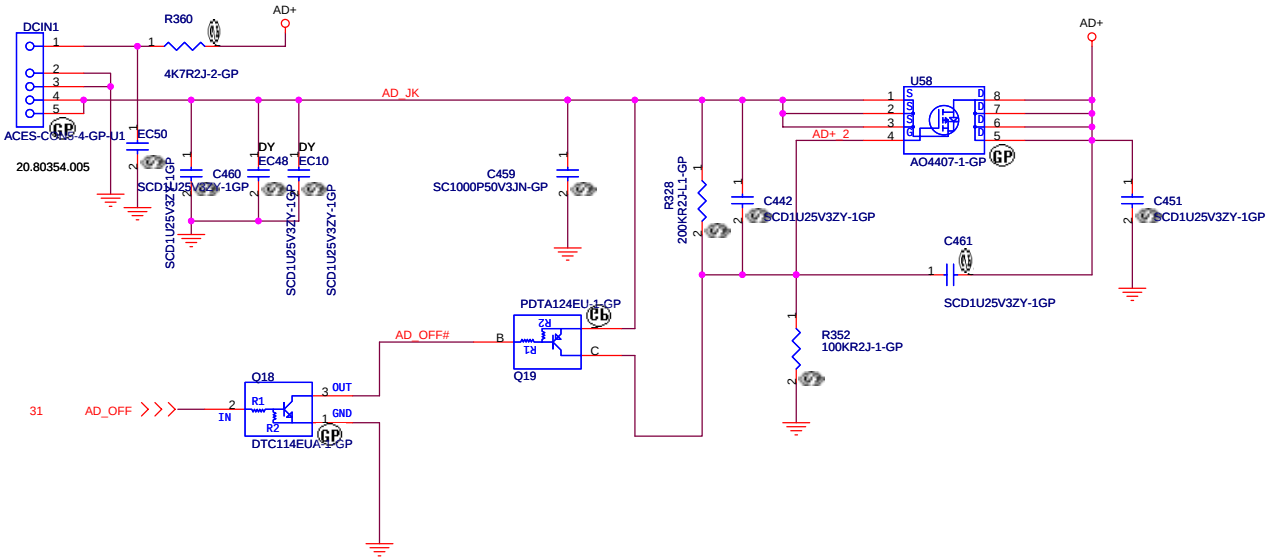
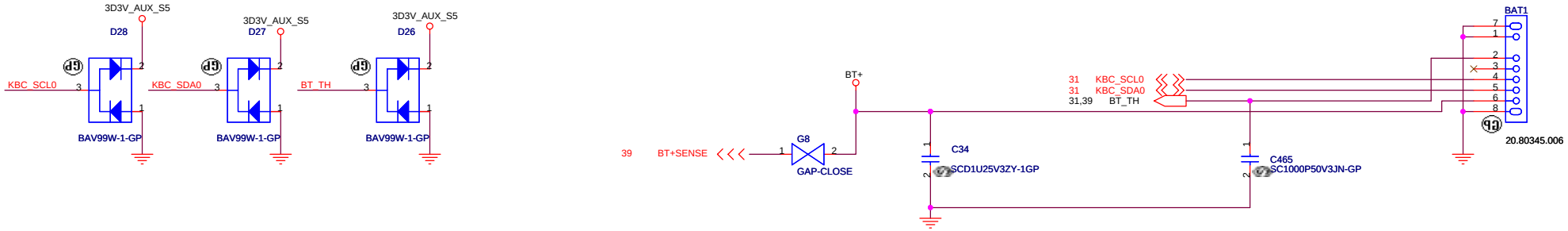
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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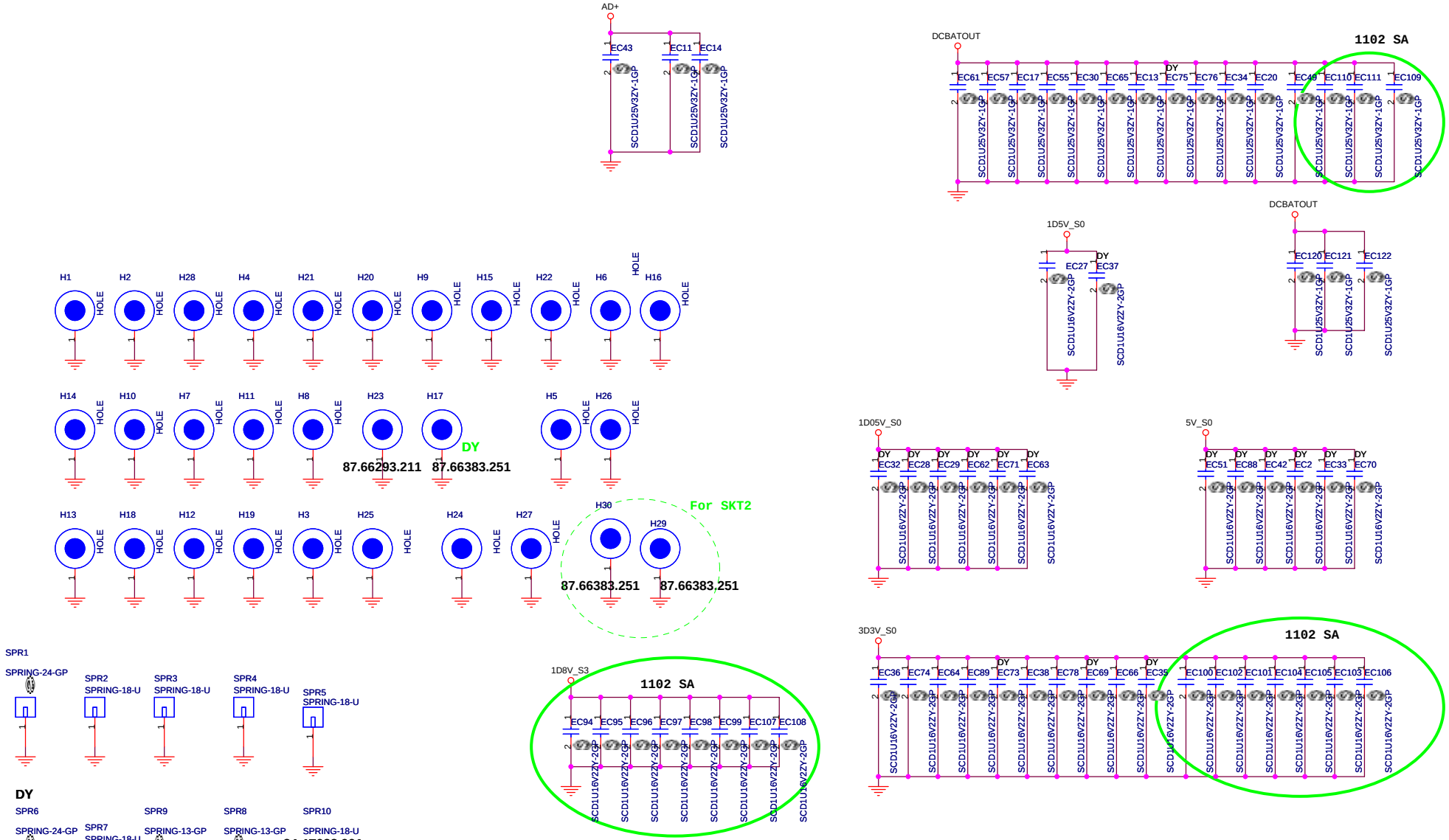

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