MODEL	REV	CHANGE LIST
CT3/5 MB 31CT3MB0015 31CT3MB0031	1A	PAGE 2 --- Enable CLK48M from clokc generator for the PLL circuit of 7411, and disable the ocsillator circuit of PCI7411 PLL. PAGE 3 --- Remove H/W shutdown circuit that supported ADM1032. PAGE 4 --- Use X7R type to replace Y5V type for CPU Decoupling/Bypass capacitor. PAGE 10 --- Add a terminal resistor R706 for -CODE_RST# to improve signal quality. PAGE 11 --- 1. Add a 10K pull-up resistor on MCH_SYNC# for booting. 2. Change the power plane of PCIE_WAKE# from 3VSUS to 3V_S5 to solve system can't turn off issue. 3. Change the power plane of ICH_THRM# and SCI_# from 3VSUS to +3V to reduce leakage. PAGE 12 --- We can also use 5VSUS to instead of 5V_S5 to save cost of MOSFET(A06402). PAGE 15 --- Add a level-shift cicuit for EDID interface. PAGE 17 --- 1. Add a off-page and a EMI solution for CLK48M. 2. Remove the reserve resistors (R693~R695) of parallel interface for PCI1510. PAGE 18 --- Remove R696, connect controller and power switch directly . PAGE 19 --- Change R682&R683 value from 56 ohms to 0 ohm cause of BOM error at A-test. PAGE 22 --- 1. Change MC3 type from Y5V to X7R to improve singal quality. 2. Connect H1/H3 to AGND via a 0 ohm resistor by Conexant's comment. PAGE 23 --- 1. Add a terminal resistor R707 for RTL8100/8110 id selection. 2. Add a 0.1uF to make Q40 turn on slowly to aviod 3VPCU drop issue. PAGE 24 --- Modified transformer circuit cause of CT can't connect each other on 10/100M application. PAGE 26 --- Add a flashrom as PLCC32 type for BIOS debugging. PAGE 27 --- 1. Change R352 value from 120K ohms to 20M ohms. 2. Add a LPC debug port for software team to debug convenient. PAGE 30 --- Add GMT fan controller for B-test to costdown. PAGE 31 --- 1. Add ESD protection circuit for S-VIDEO signal to Docking. 2. Add R713 to enable the mux in the Tampa-2 cable PAGE 33 --- Change PR143 value from 100K to 10K to solve display abnormal issue. PAGE 35 --- 1. Move 5V_S5 circuit to Page 36. 2. De-popuplate PQ129 and PR182. 3. Change PR178 value from 22 ohm to 47 ohm. PAGE 36 --- Remove PC170 and PQ127 but reserve 5V_S5 power circuit.

Model / Page	CT3/5 MB BOARD	
	FROM	TO
1	1A	
2	1A	2A
3	1A	2A
4	1A	2A
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	2A
11	1A	2A
12	1A	2A
13	1A	
14	1A	
15	1A	2A
16	1A	
17	1A	2A
18	1A	2A
19	1A	2A
20	1A	
21	1A	
22	1A	2A
23	1A	2A
24	1A	2A
25	1A	
26	1A	2A
27	1A	2A
28	1A	
29	1A	
30	1A	2A
31	1A	2A
32	1A	
33	1A	2A
34	1A	
35	1A	2A
36	1A	2A
37	1A	
38	1A	
39	1A	

MODEL	REV	CHANGE LIST
CT3/5 MB 31CT3MB0015 31CT3MB0031	2A	PAGE 2 --- 1. Add C1048 for CLK48M to get better EMI performance. PAGE 3 --- 1. Add R733 as pull-up resistor for PREQ#. PAGE 11 --- 1. Add RF_OFF# and BT_OFF# PAGE 17 --- 1. Populate R704 and C1046 to get better EMI performance. 2. Remove R701 & R702 for unused PCI1510RVGF circuit. PAGE 18 --- 1. Disconnect SM_PHYS_WP on controller side. 2. Tie SM_EL_WP with SM_PHYS_WP on conn side to allow for normal operation of SD and SM. 3. Add a discharge circuit for media card power. 4. Add R718 to solve cross-talk issue of MS-Pro card. 5. Add R717 to solve SM card can't write protect issue. 6. Add R719~R736 as terminal on all multi-function pins. 7. Add pull-up circuit. PAGE 27 --- 1. Reserve 0R for RF_OFF# and BT_OFF# circuit. 2. Modify LPC pin name. PAGE 28 --- 1. Change HDD and ODD select definition. PAGE 30 --- Adjust Capacitors and Bead to improve CRT timing issue. 1. Change L66, L67, L68 from BK1608HM470 to 0R. 2. Remove C931, C932, C933. 3. Change C934, C935, C936 from 22P to 5.6P. 4. Change C6, C14, C350 from 10P to 5.6P. 5. Change L1, L26, L27 from BK1608HM470 to BLM18BA750SN1T. PAGE 31 --- 1. Change L5,L6,L7,C57,C58,C64,C77,C113,C121 value to improve S-video quality. 2. Reserve S-video impedance match circuit.

Model / Page	CT3/5 MB BOARD FROM	CT3/5 MB BOARD TO
1	1A	
2	2A	3A
3	2A	3A
4	2A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	2A	
11	2A	
12	1A	
13	1A	
14	1A	
15	2A	
16	1A	
17	2A	3A
18	2A	3A
19	2A	
20	1A	
21	1A	
22	2A	
23	2A	
24	2A	
25	1A	
26	2A	2A
27	2A	
28	1A	2A
29	1A	
30	2A	
31	2A	
32	1A	
33	2A	
34	2A	
35	2A	
36	2A	
37	2A	
38	2A	
39	2A	

CT3 BLOCK DIAGRAM

PENTIUM-M / ALVISO / ICH6-M

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCB THICKNESS: 1.2mm

CPU THERMAL SENSOR
MAX6657 / GMT-781
+3V PAGE: 3

Processor
Intel Pentium-M
Intel Celeron-M
478 Pins (micro FC-PGA)
VCC_CORE
VCCP
VCCA
PAGE: 3, 4

FSB
400/533 MHZ

14.318MHz

CLOCK GEN
ICS954206A
CY28411ZXC
+3V PAGE: 2

HCLK_CPU	100MHZ	33MHZ	PCLK_591
HCLK_CPU#	100MHZ	33MHZ	PCLK_7411
HCLK_MCH	100MHZ	33MHZ	PCLK_ICH
HCLK_MCH#	100MHZ	33MHZ	PCLK_MINI
SRC_MCH	100MHZ	33MHZ	PCLK_LAN
SRC_MCH#	100MHZ	48MHZ	CLK48_USB
SRC_ICH	96MHZ	14MHZ	14M_ICH
SRC_ICH#			
DREFSSCLK			
DREFSSCLK#			
DOT96			
DOT96#			

SYSTEM POWER MAX1845
2.5VSUS/1.5V_S5 PAGE: 38

CPU CORE MAX1907
POWER 1.356V PAGE: 33

SYSTEM POWER MAX1999
POWER(3V/5V/15V) PAGE: 36

SYSTEM POWER MAX1992
VCCP PAGE: 37

NS L2996
VTT_DDR PAGE: 39

BATT CHARGER
MAX1772 PAGE: 34

DISCHARGE PAGE: 35

CRT port PAGE: 30 — R.G,B
LCD Panel PAGE: 15 — LVDS
MINI-DIN PAGE: 32 — S-VIDEO

Alviso-GM
GMCH
82875GM/GME
1257 PCBGA
VCCP
2.5VSUS
+1.5V
+2.5V
+3V
PAGE: 5, 6, 7

DDR I/F 2.5V
333MHz
Single Channel

DDR-SODIMM1
2.5VSUS
SMDDR_VTERM
DDR-SODIMM2
PAGE: 13

DMI interface
100MHZ 4X

32.768KHz

USB PORT 0, 1 PAGE: 19 — USB 2.0
1st IDE - HDD PAGE: 28 — ATA 66/100
2nd IDE - CDROM PAGE: 28 — ATA 66/100

ICH6-M
82801FBM
609 BGA
+5V
5VSUS
+3V
3V_S5
3VSUS
+2.5V
+1.5V
1.5V_S5
VCCRTC
GMCH_VTT
PAGE: 8, 9, 10

33MHZ, 3.3V PCI
AC97

24.576MHz
25MHz
24.576MHz
48MHz

PWRCLKP
PWRCLKN
DIB_DATAN
DIB_DATAP

AC97
CX20468-31
MBAMC20493-010
PAGE: 20

LAN
Realtek
8100CL
LANVCC PAGE: 23

MINI-PCI
+3V
+5V
LANVCC
PAGE: 14

CARDBUS / IEEE 1394 CONTROLLER/CF
3VSUS
TI 7411
PAGE: 16, 17, 18, 19

3.3V LPC, 33MHz

32.768KHz

PC97551
TQFP 176
3VPCU
+3V
VCCRTC
PAGE: 27

SMARTDAA MODEM, MDC
PAGE: 22

WIRE

RJ11 JACK
PAGE: 24

AMP
TPA0312
PAGE: 21

JACK
HEADPHONE,
2ND HEADPHONE,
MIC
PAGE: 21

RJ45 JACK
PAGE: 24

Intel WLAN W2200 802.11b/g

5 IN 1
CARD READER
SD/MMC, SM, MS, XD
PAGE: 18

CARDBUS SLOT X1
PAGE: 16

1394 CONN
PAGE: 19

CABLE DOCK PAGE: 31
Daughter Board TV, USB, BLUE TOOTH PAGE: 32
AV BOARD PAGE: 32
Power Board PAGE: 32

FAN PAGE: 30
Touchpad PAGE: 32
Keyboard PAGE: 32
FLASH PAGE: 26

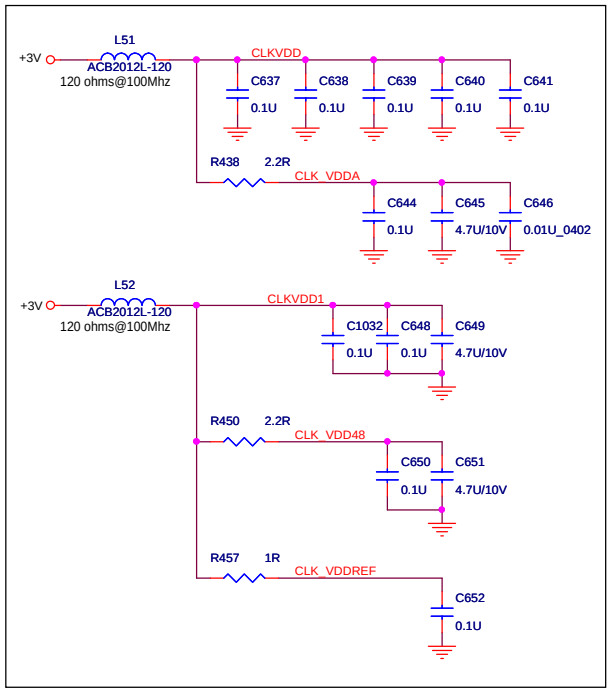
PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
GBIT ETHERNET	AD16	2	A
MINIPCI SLOT	AD22	1	C,D
CardBus/1394	AD25	0	E,F,G

PROJECT : CT3
Quanta Computer Inc.

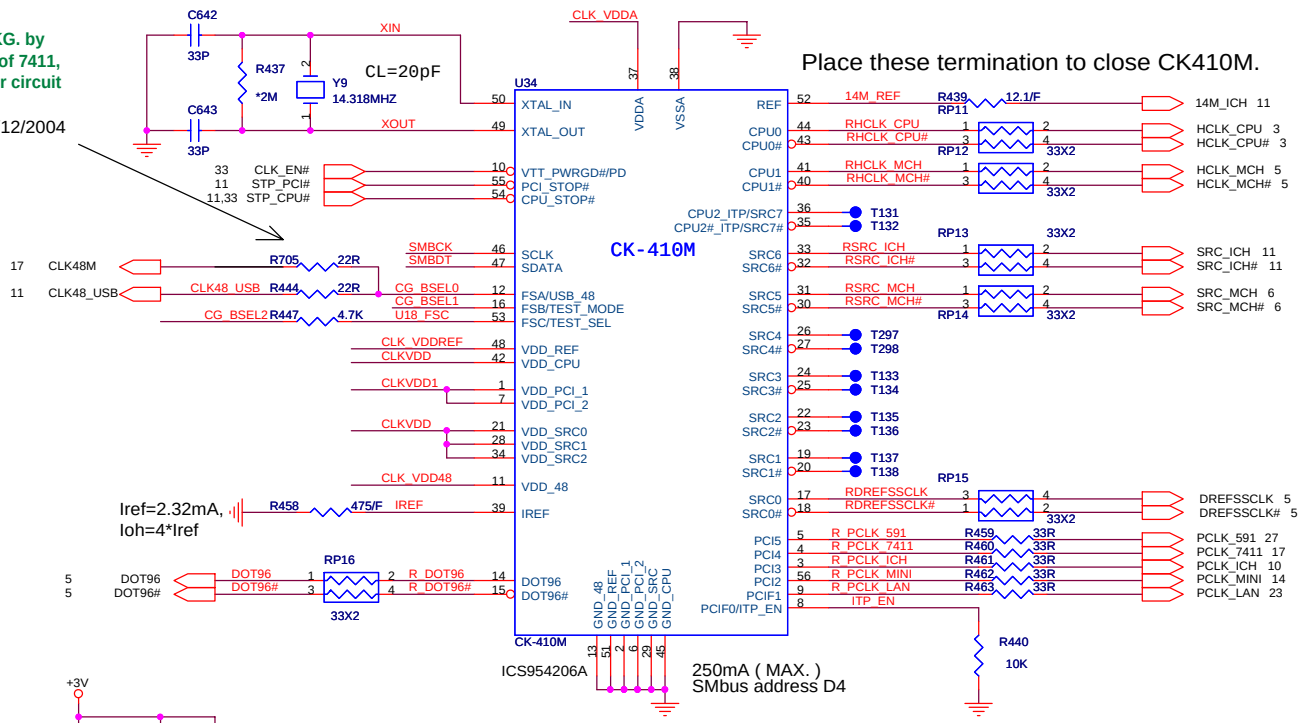
Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Monday, December 27, 2004 Sheet 1 of 39



SI stage:
Enable CLK48M from CKG. by R705 for the PLL circuit of 7411, and disable the ocsillator circuit at PCI7411 side.

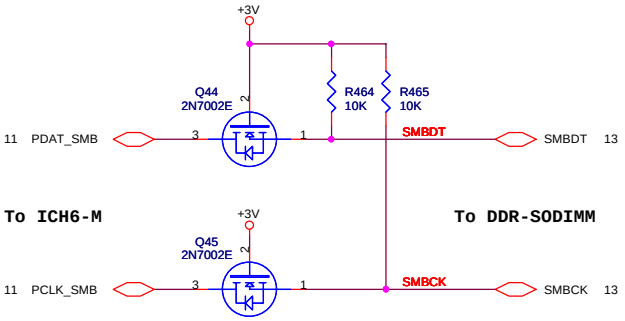
Sting 10/12/2004



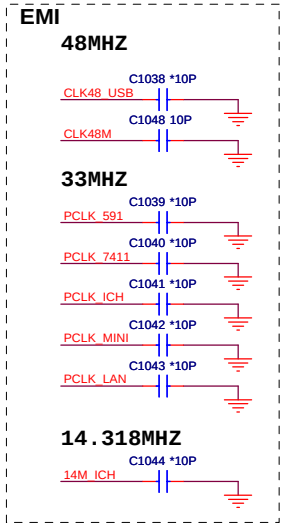
Place these termination to close CK410M.

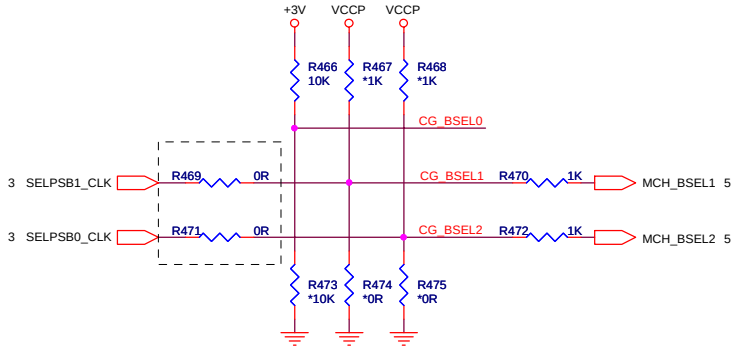
FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	DOTHAN FSB 400
0	0	1	133	100	33	DOTHAN FSB 533
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	RESERVED			

**** Frequence select by CPU auto sense.***



R_PCLK_LAN	ITP_EN
0: SRCCLK=96MHZ	0: SRC_7 Pair
1: SRCCLK=100MHZ	1: CPU_2 ITP Pair

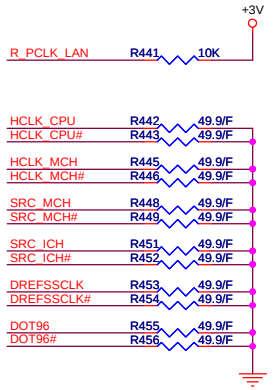




R469,R471
Dothan-A can remove so that the FSB frequency will be selected by hardware setting(R474,R475,R467,R468).
Dothan-B should be populated.

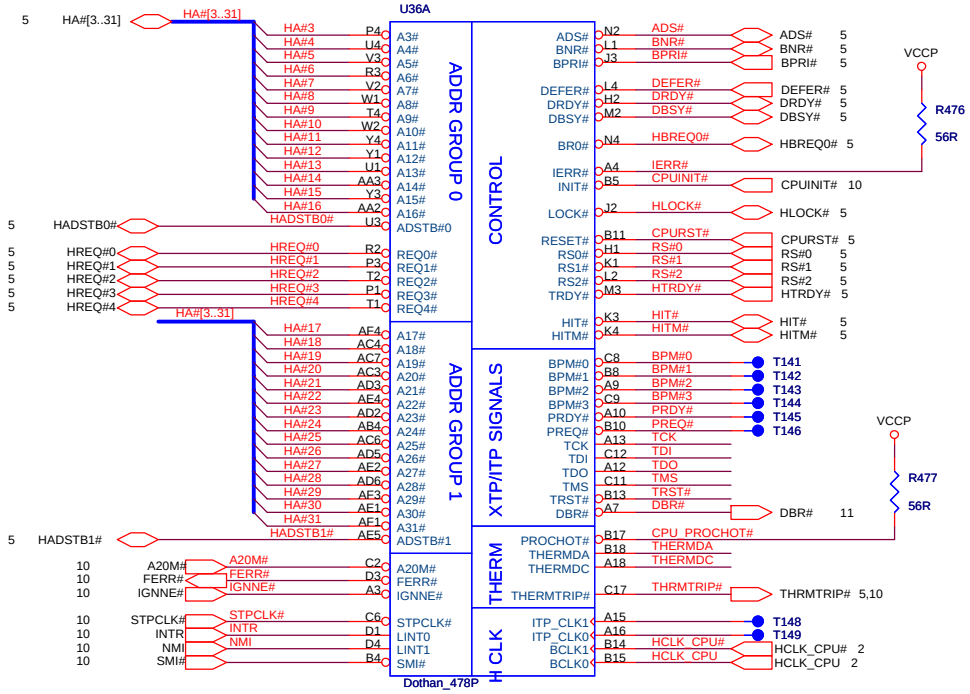
PV stage:
Add C1048 for CLK48M to get better EMI performance.

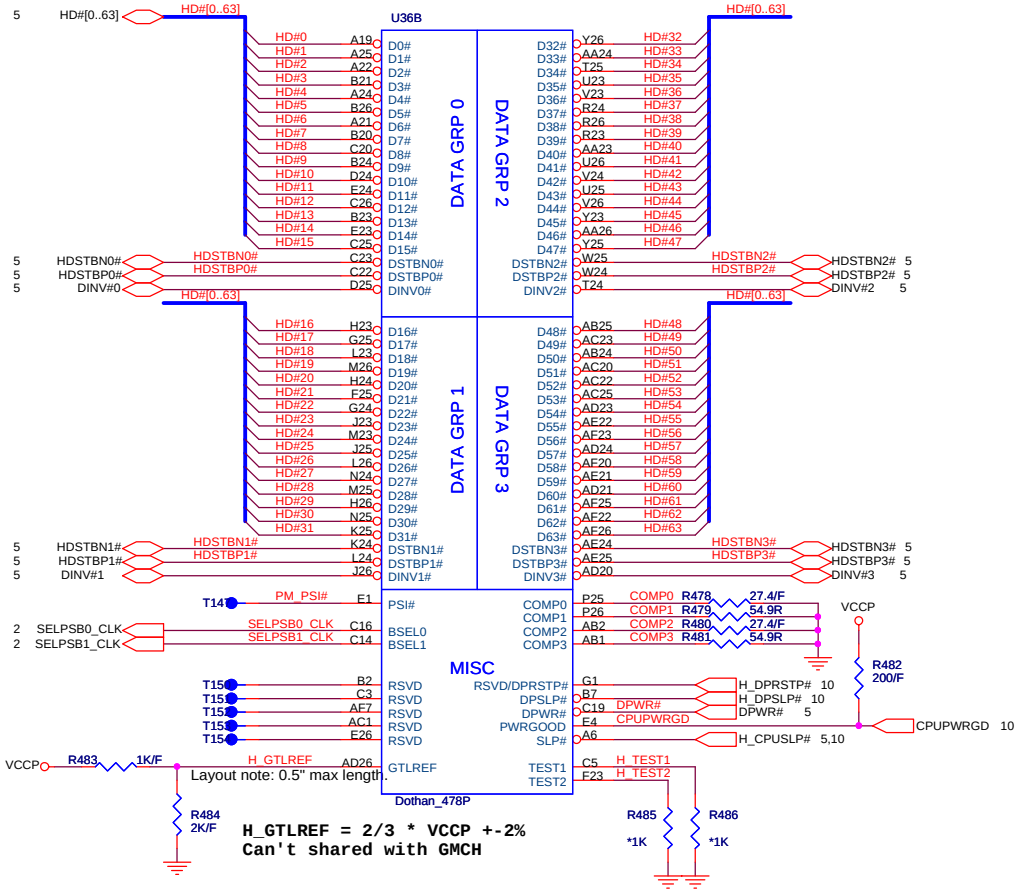
Sting 11/29/2004

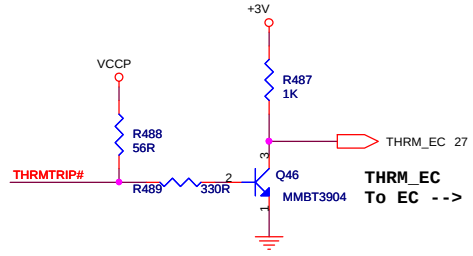


PROJECT : CT3
Quanta Computer Inc.

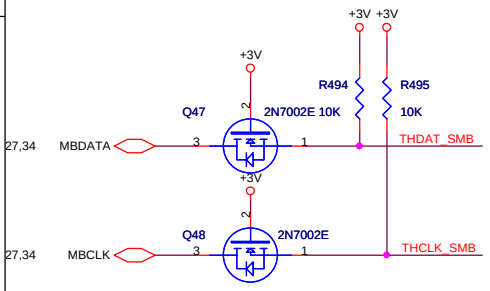
Size	Document Number	Rev
Custom	CLOCK GENERATOR	3A
Date: Monday, December 27, 2004	Sheet 2 of 39	

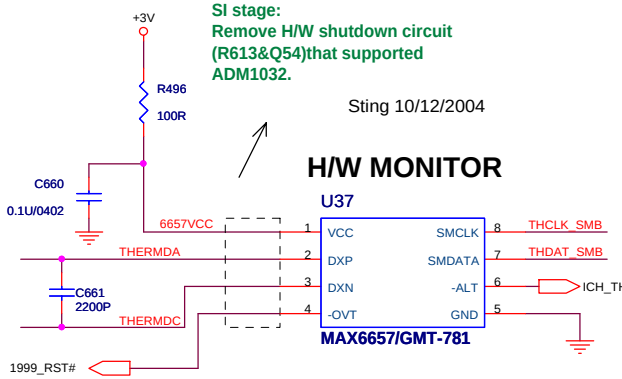






THRM_EC
To EC --> Send FANSIG to control fan.



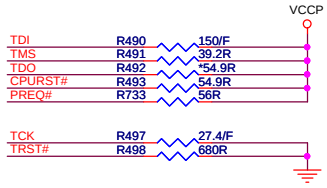


SI stage:
Remove H/W shutdown circuit (R613&Q54)that supported ADM1032.

Sting 10/12/2004

H/W MONITOR

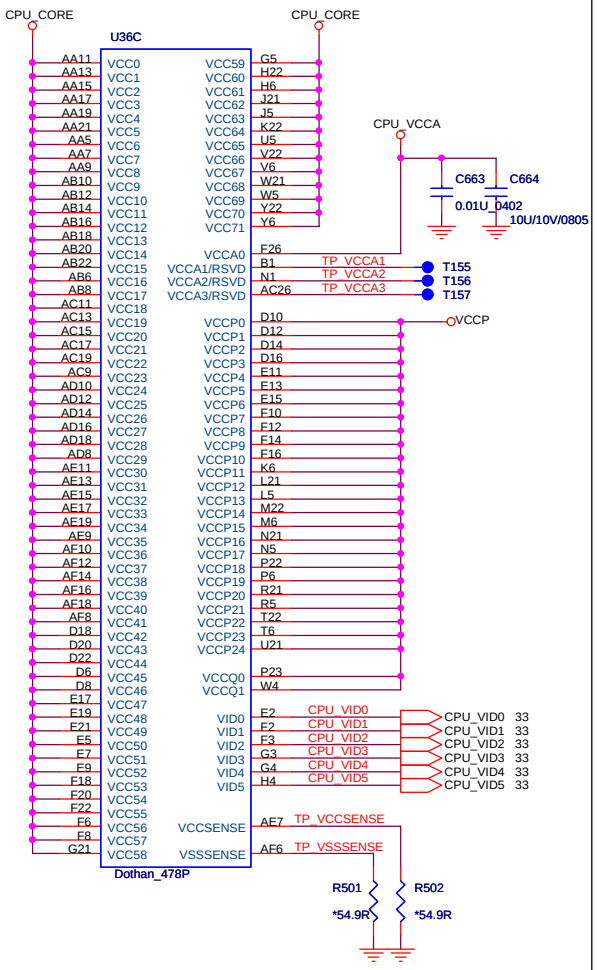
ICH_THRM#
To SB --> System throttling

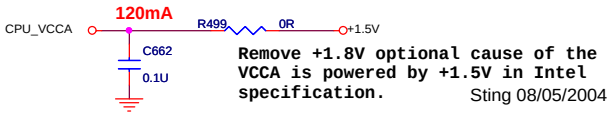


PV stage:
Add R733 as pull-up resistor for PREQ#.
Sting 11/29/2004

PROJECT : CT3
Quanta Computer Inc.

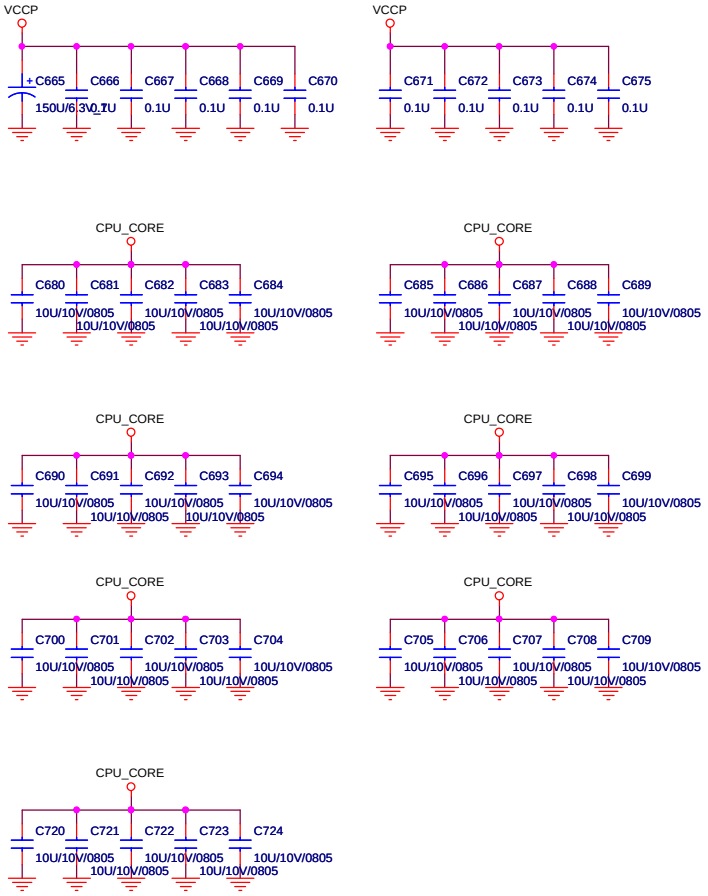
Size	Document Number	Rev
Custom	Dothan CPU (Host Bus)	3A
Date: Monday, December 27, 2004	Sheet 3 of 39	

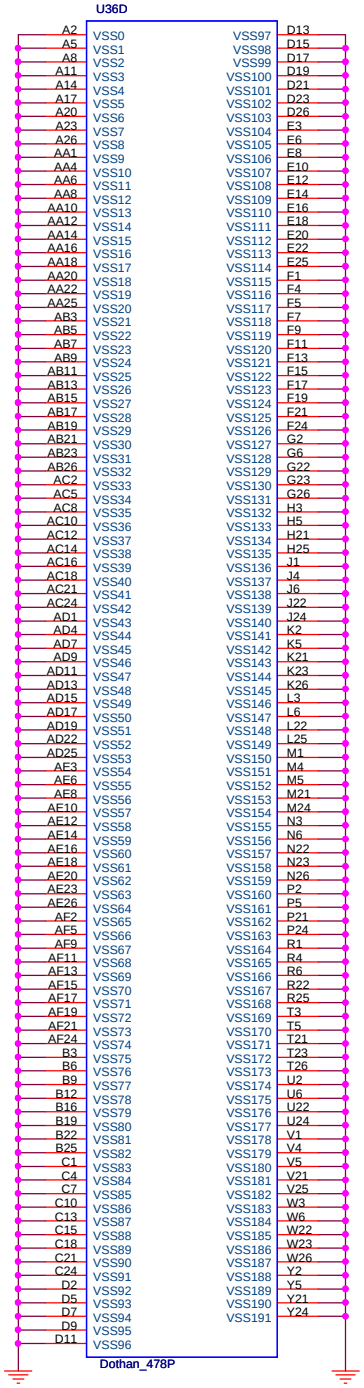




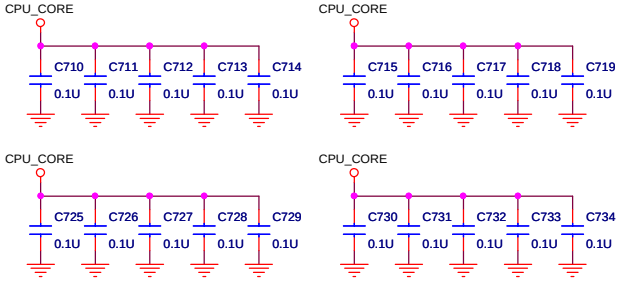
Remove +1.8V optional cause of the VCCA is powered by +1.5V in Intel specification.
Sting 08/05/2004

SI stage:
Use X7R type to replace Y5V type for Decoupling/Bypass capacitor.
Sting 10/12/2004



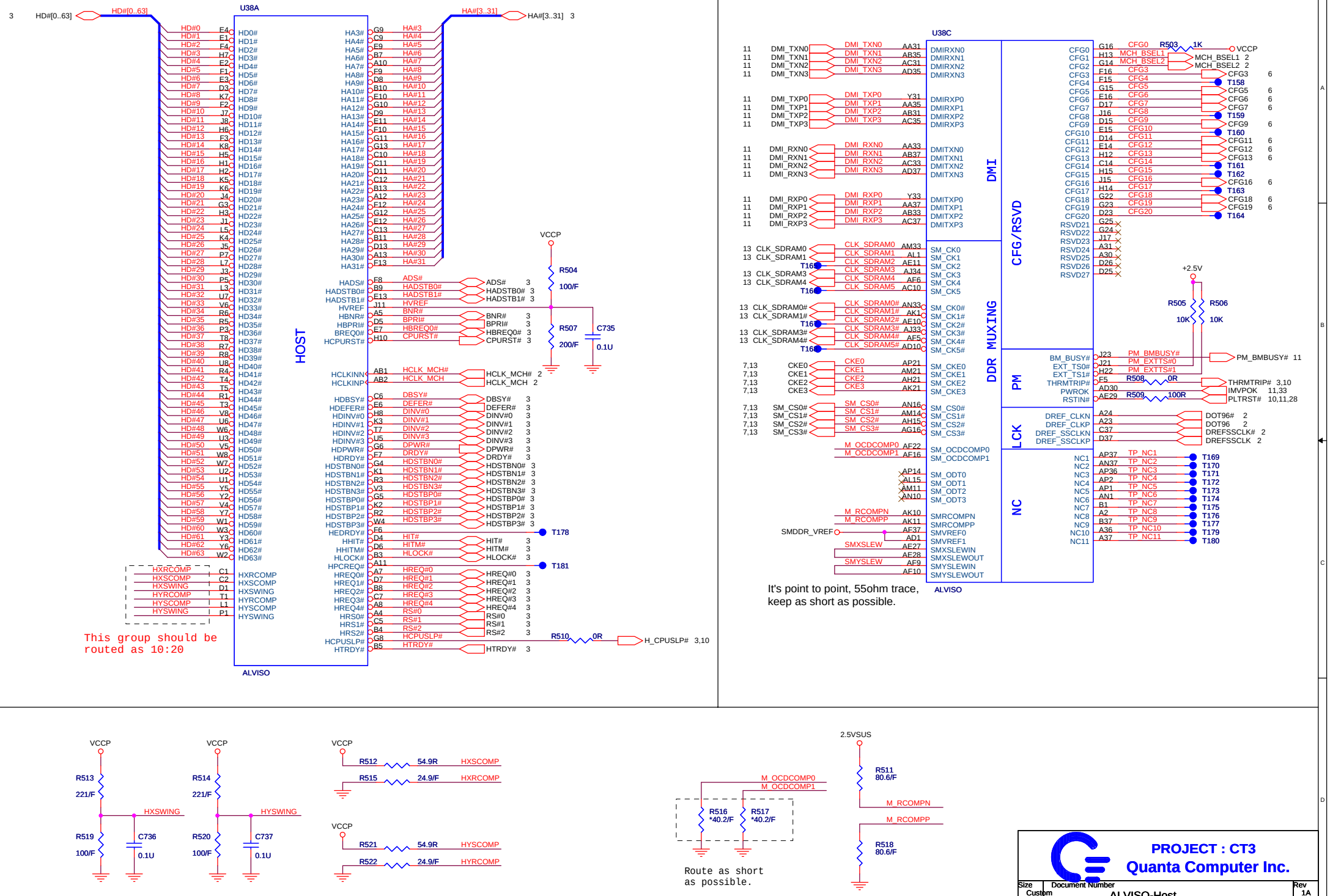


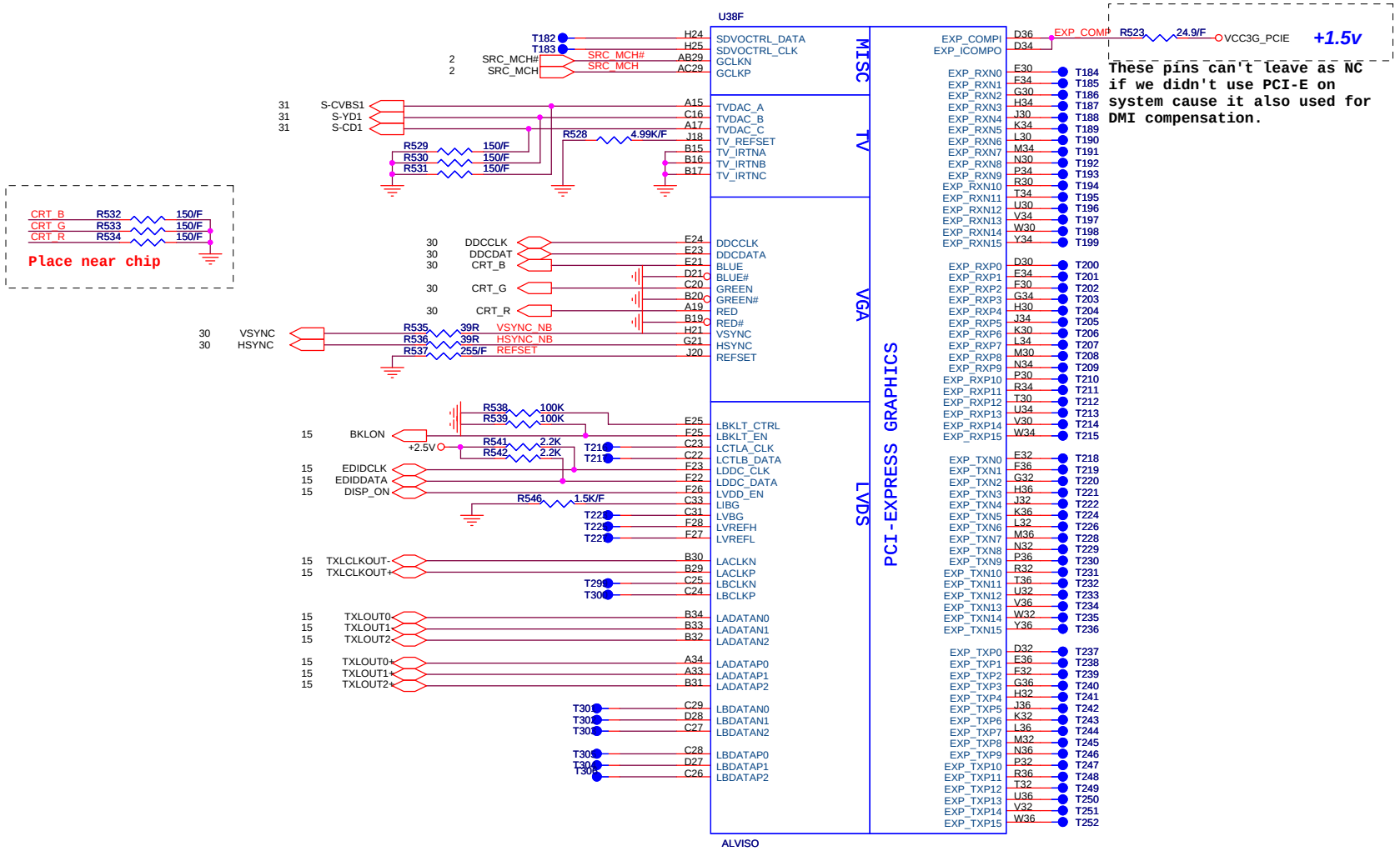
CPU de-coupling capacitor



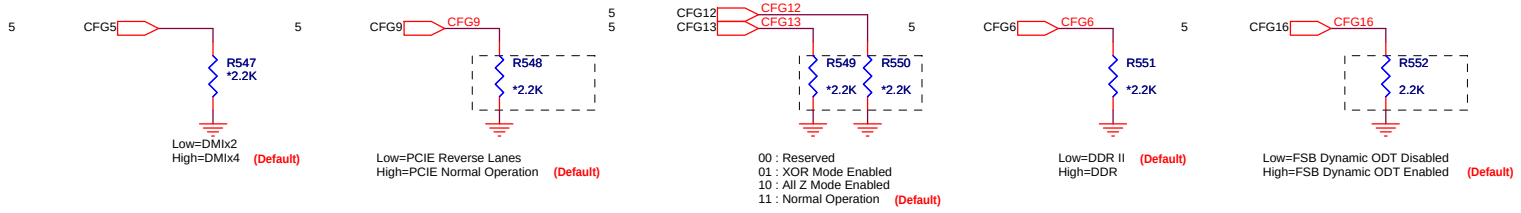
CPU Bypass capacitor

PROJECT : CT3				
Quanta Computer Inc.				
Size: Custom	Document Number: CPU POWER / GND			Rev: 2A
Date: Monday, December 27, 2004		Sheet 4	of	39


U38A
HOST
ALVISO
HD#[0..63]
HA#[3..31]
VCCP
R504
100/F
R507
200/F
C735
0.1U
R510
0R
H_CPUSLP# 3,10
This group should be routed as 10:20
U38C
DMI
DDR MUXING
CFG/RSVD
PM
LCK
NC
+2.5V
R505
10K
R506
10K
R508
0R
R509
100R
PM_BMBUSY# 11
THRMTRIP# 3,10
IMVPOK 11,33
PLTRST# 10,11,28
DOT96# 2
DOT96 2
DREFSSCLK# 2
DREFSSCLK 2
It's point to point, 55ohm trace, keep as short as possible.
R503
1K
MCH_BSEL1 2
MCH_BSEL2 2
R513
221/F
R514
221/F
HXSWING
HYSWING
R519
100/F
R520
100/F
C736
0.1U
C737
0.1U
R512
54.9R
HXSCOMP
R515
24.9/F
HXRCOMP
R521
54.9R
HYSCOMP
R522
24.9/F
HYRCOMP
R516
*40.2/F
R517
*40.2/F
Route as short as possible.
2.5VSUS
R511
80.6/F
M_RCOMPN
M_RCOMPP
R518
80.6/F
PROJECT : CT3
Quanta Computer Inc.
Size
Custom
Document Number
ALVISO-Host
Rev
1A
Date:
Monday, December 27, 2004
Sheet
5
of
39



Strapping



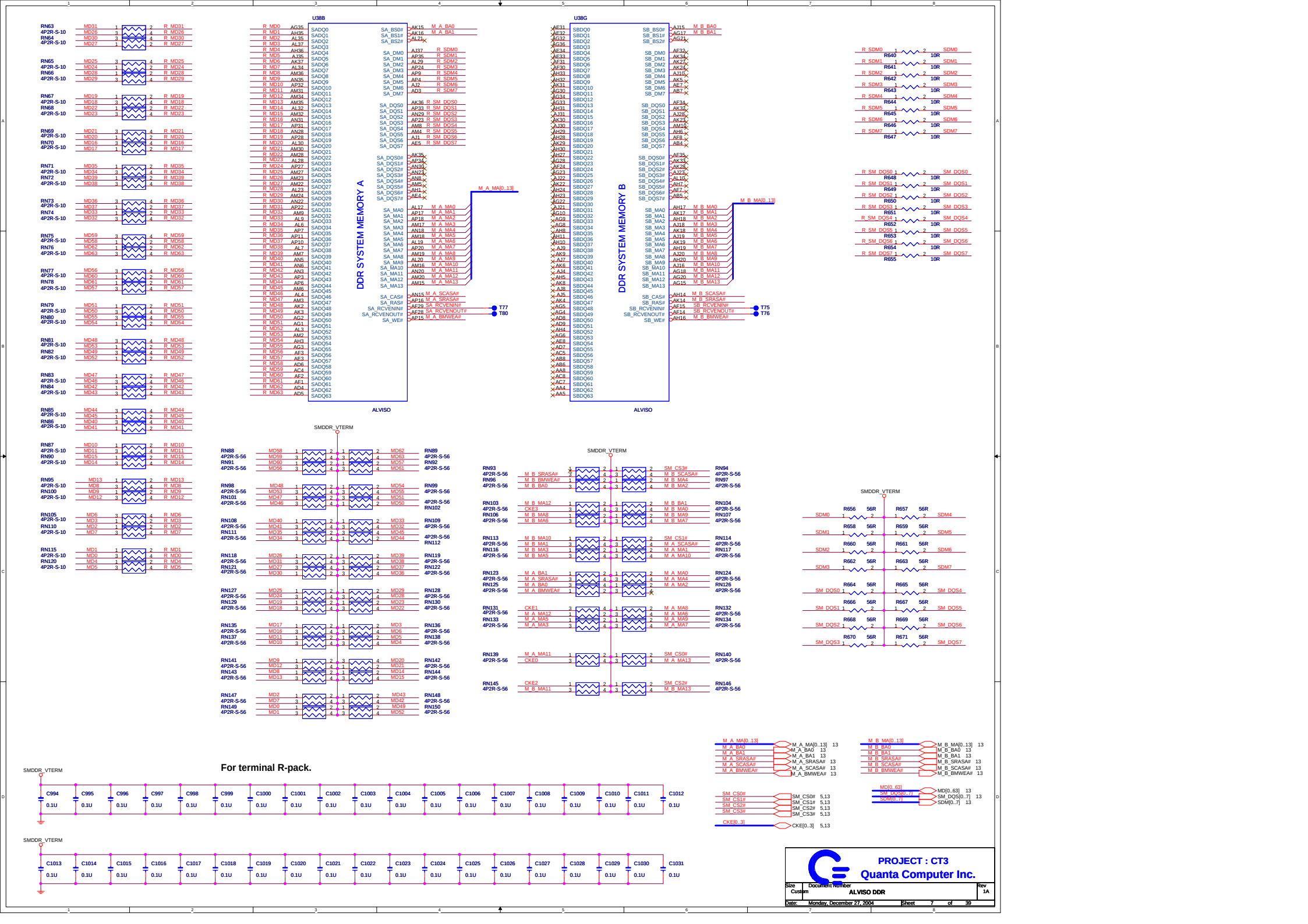
CFG[2:0]
001=533MT/S FSB
101=400MT/S FSB

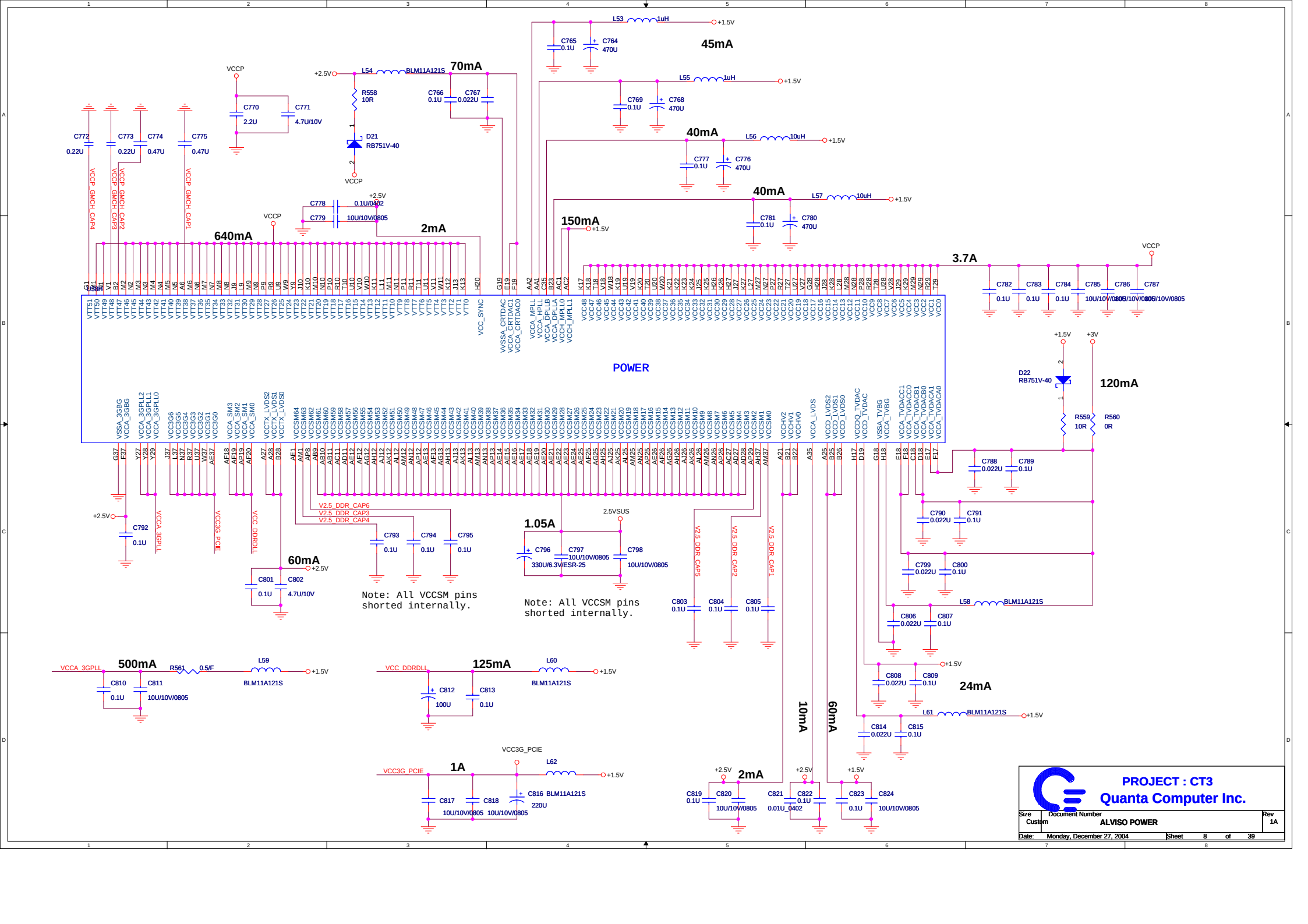
CFG[3:17] have internal pullup.

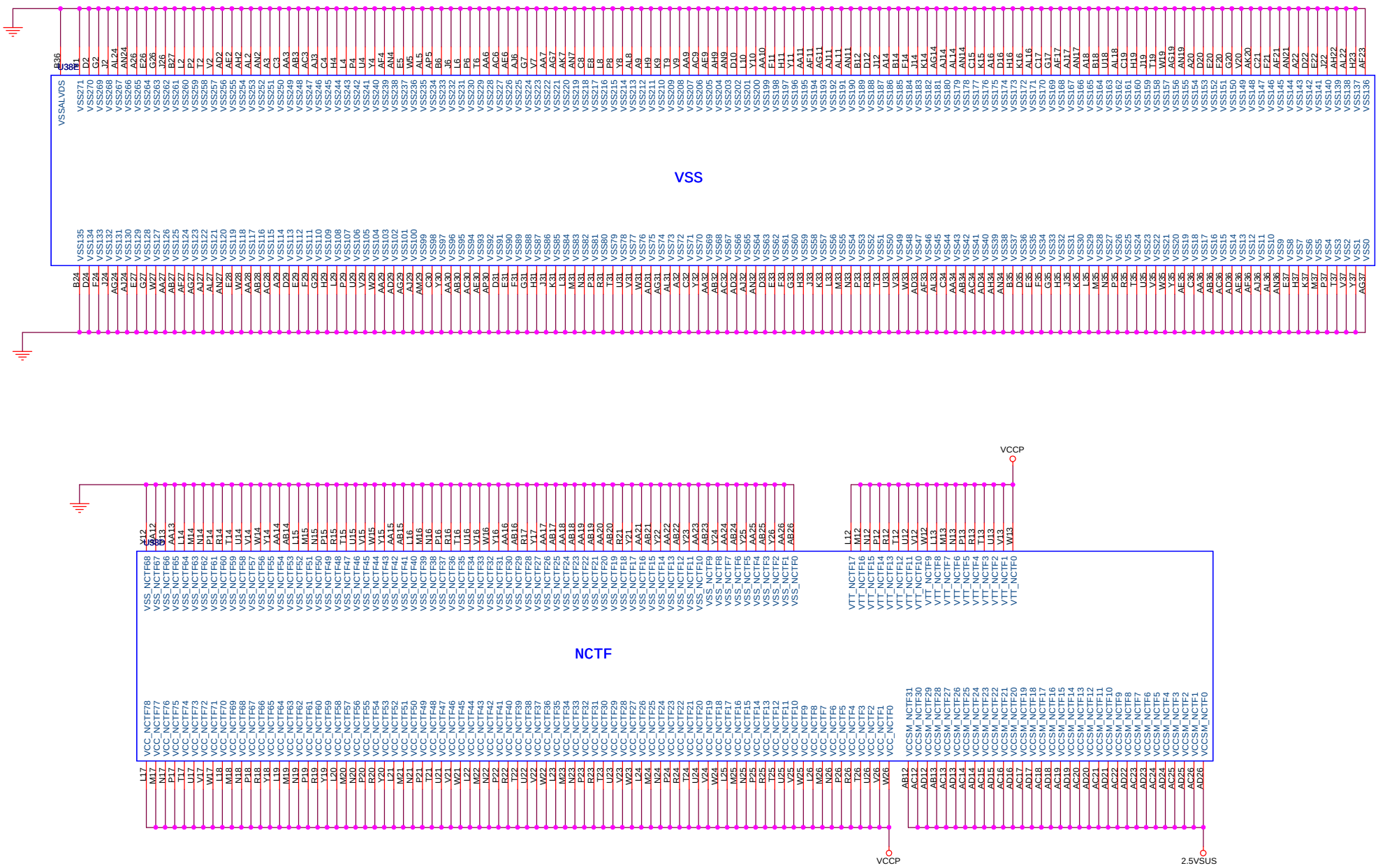
CFG[18:19] have internal pulldown.

PROJECT : CT3
Quanta Computer Inc.

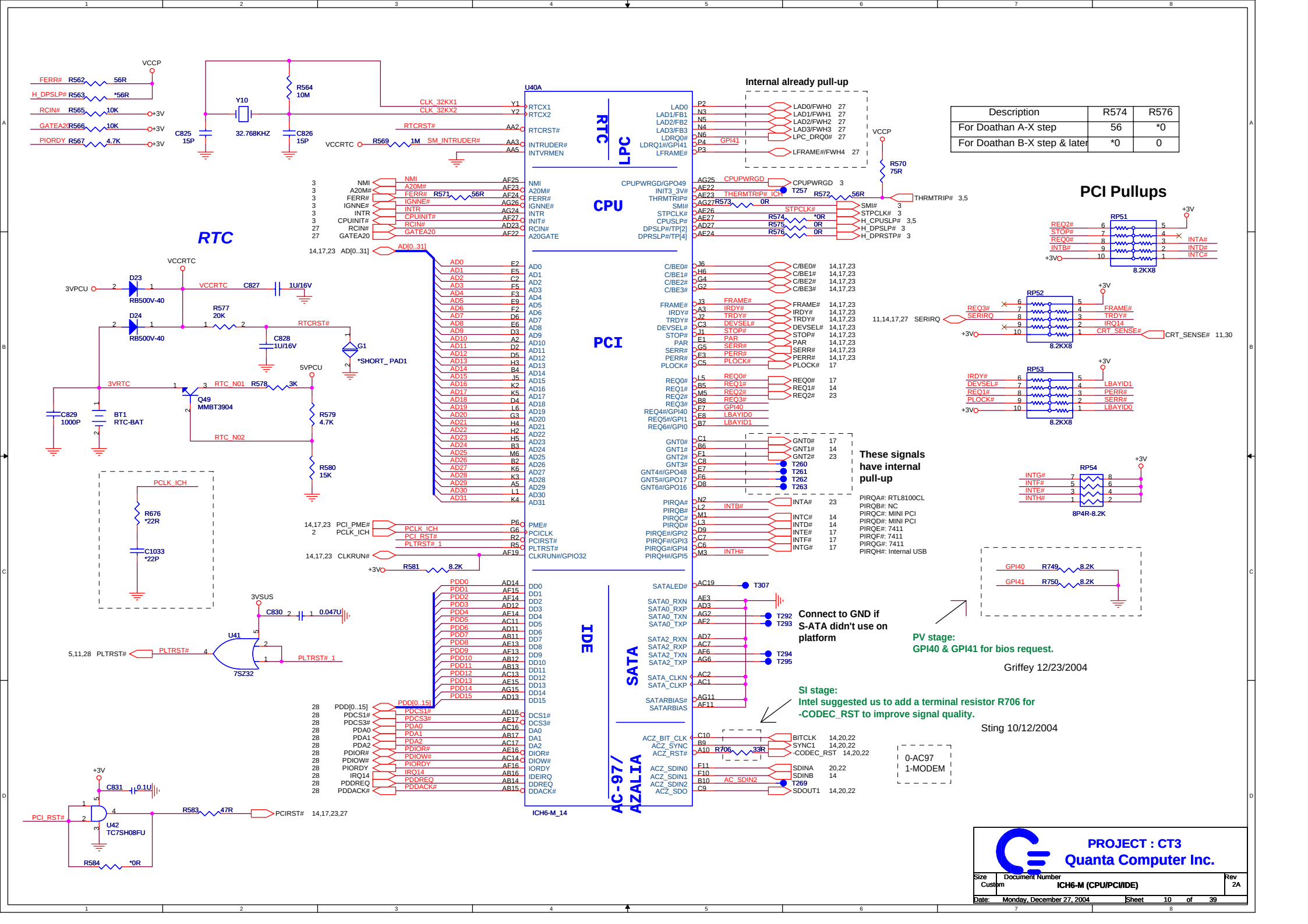
Size	Document Number	Rev
Custom	ALVISO DMI	1A
Date: Monday, December 27, 2004	Sheet 6 of 39	


U38B
DDR SYSTEM MEMORY A
ALVISO
U38G
DDR SYSTEM MEMORY B
ALVISO
M_A_MA[0..13]
M_B_MA[0..13]
SMDDR_VTERM
For terminal R-pack.
PROJECT : CT3
Quanta Computer Inc.
ALVISO DDR
Monday, December 27, 2004


POWER
640mA
2mA
150mA
45mA
70mA
40mA
40mA
3.7A
120mA
60mA
1.05A
500mA
125mA
24mA
10mA
60mA
1A
2mA
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
PROJECT : CT3
Quanta Computer Inc.
ALVISO POWER
Monday, December 27, 2004



PROJECT : CT3			
Quanta Computer Inc.			
Size: Custom	Document Number: ALVISO VSS/NCTF		Rev: 1A
Date: Monday, December 27, 2004	Sheet 9 of 39		

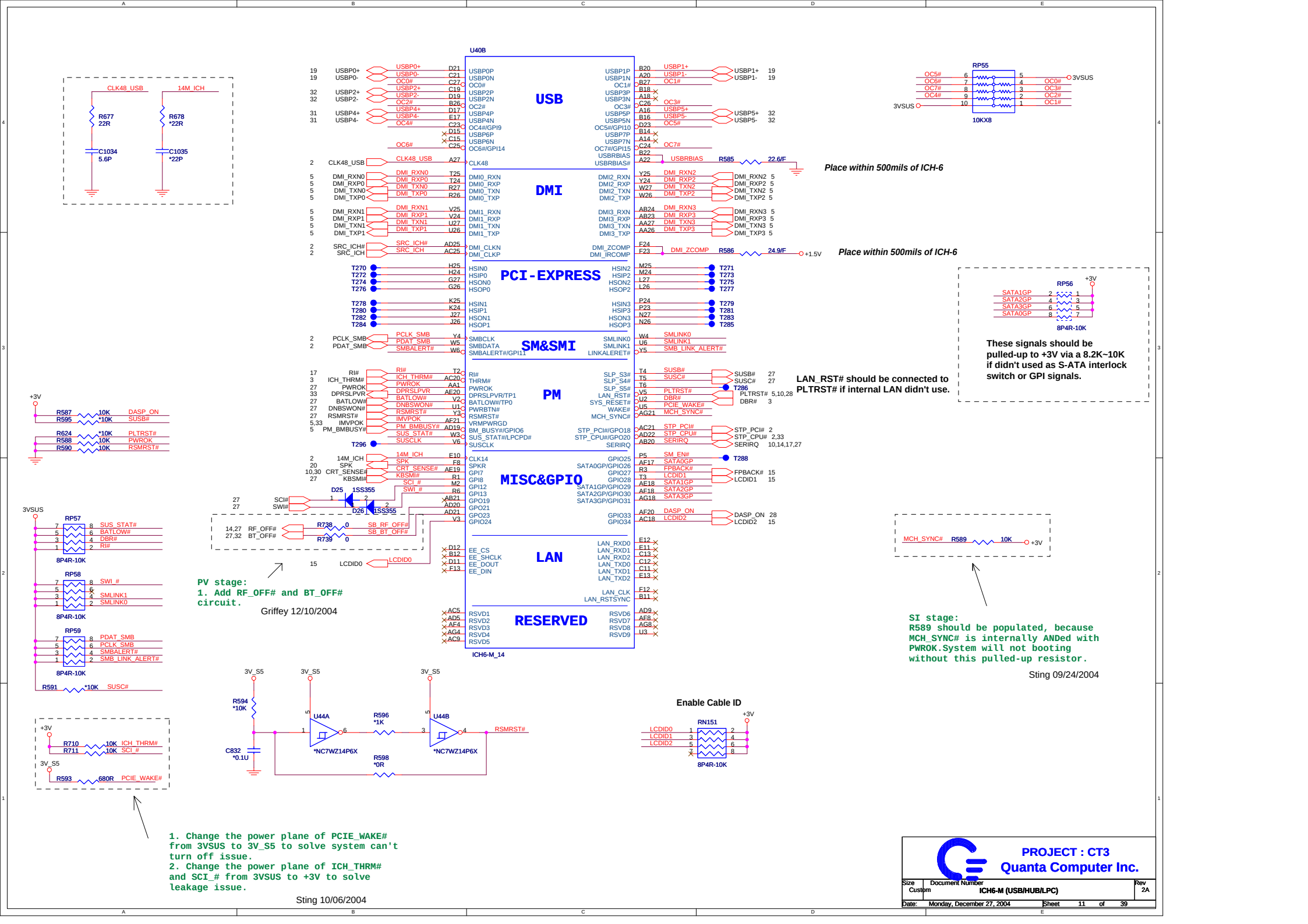


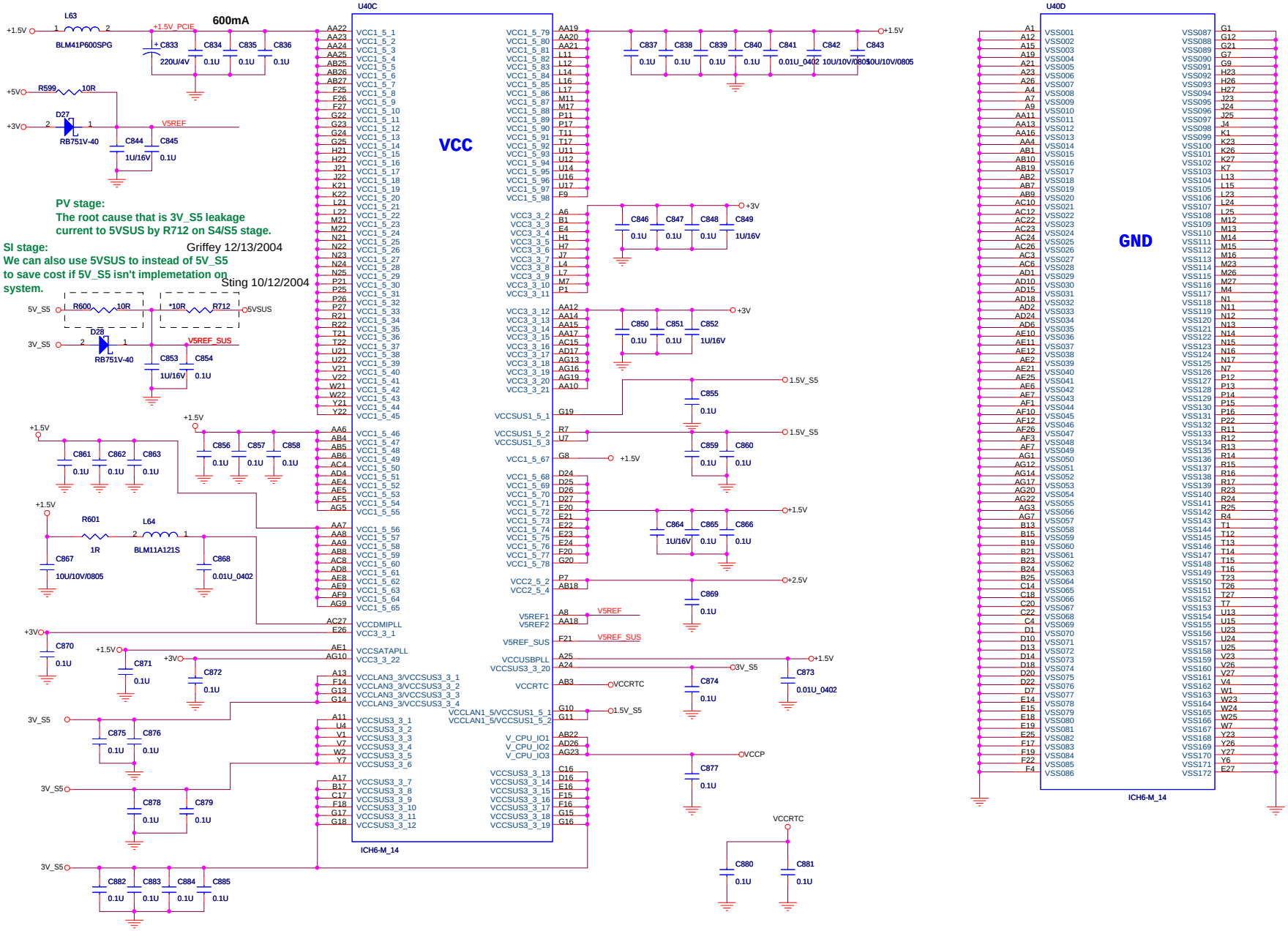
Description	R574	R576
For Doathan A-X step	56	*0
For Doathan B-X step & later	*0	0

PROJECT : CT3
Quanta Computer Inc.

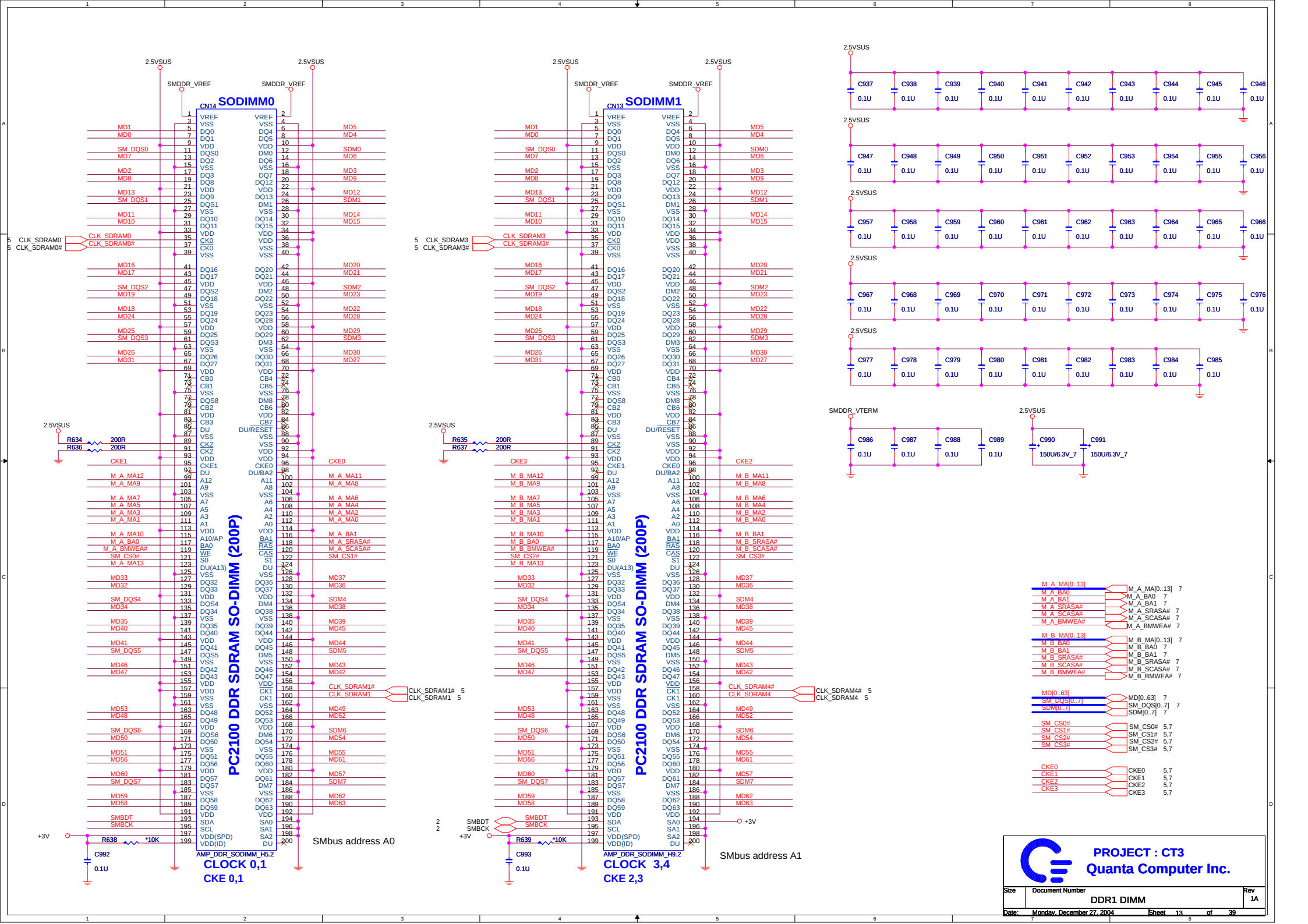
Size	Document Number	Rev
Custom	ICH6-M (CPU/PCI/IDE)	2A

Date: Monday, December 27, 2004 Sheet 10 of 39


U40B
USB
DMI
PCI-EXPRESS
SM&SMI
PM
MISC&GPIO
LAN
RESERVED
ICH6-M_14
CLK48_USB
14M_ICH
R677 22R
R678 *22R
C1034 5.6P
C1035 *22P
USBP0+
USBP0-
USBP2+
USBP2-
USBP4+
USBP4-
OC6#
CLK48_USB
DMI_RXN0
DMI_RXP0
DMI_TXN0
DMI_TXP0
DMI_RXN1
DMI_RXP1
DMI_TXN1
DMI_TXP1
SRC_ICH#
SRC_ICH
T270
T272
T274
T276
T278
T280
T282
T284
PCLK_SMB
PDAT_SMB
SMBALERT#
RI#
ICH_THRM#
PWROK
DPRSLPVR
BATLOW#
DNBSWON#
RSMRST#
IMVPOK
PM_BMBUSY#
SUS_STAT#
SUSCLK
T296
14M_ICH
SPK
CRT_SENSE#
KBSMI#
SCI_#
SWI_#
LCDID0
USBP1+
USBP1-
OC1#
OC3#
USBP5+
USBP5-
OC5#
OC7#
USBRBIAS
R585 22.6/F
Place within 500mils of ICH-6
DMI_RXN2
DMI_RXP2
DMI_TXN2
DMI_TXP2
DMI_RXN3
DMI_RXP3
DMI_TXN3
DMI_TXP3
DMI_ZCOMP
DMI_IRCOMP
R586 24.9/F
+1.5V
Place within 500mils of ICH-6
T271
T273
T275
T277
T279
T281
T283
T285
SMLINK0
SMLINK1
SMB_LINK_ALERT#
SUSB#
SUSC#
T286
PLTRST# 5,10,28
DBR# 3
LAN_RST# should be connected to PLTRST# if internal LAN didn't use.
STP_PCI#
STP_CPU#
SERIRQ
T288
SM_EN#
SATA0GP
FPBACK#
LCDID1
SATA1GP
SATA2GP
SATA3GP
DASP_ON
LCDID2
FPBACK# 15
LCDID1 15
STP_PCI# 2
STP_CPU# 2,33
SERIRQ 10,14,17,27
RP55
10KX8
OC0#
OC2#
OC3#
OC1#
3VSUS
RP56
8P4R-10K
SATA1GP
SATA2GP
SATA3GP
SATA0GP
+3V
These signals should be pulled-up to +3V via a 8.2K~10K if didn't used as S-ATA interlock switch or GPI signals.
D25 1SS355
D26 1SS355
SCI#
SWI#
RF_OFF#
BT_OFF#
R738 0
R739 0
SB_RF_OFF#
SB_BT_OFF#
PV stage:
1. Add RF_OFF# and BT_OFF# circuit.
Griffey 12/10/2004
MCH_SYNC#
R589 10K
SI stage:
R589 should be populated, because MCH_SYNC# is internally ANDed with PWROK.System will not booting without this pulled-up resistor.
Sting 09/24/2004
R587 10K DASP_ON
R595 *10K SUSB#
R624 *10K PLTRST#
R588 10K PWROK
R590 10K RSMRST#
RP57
SUS_STAT#
BATLOW#
DBR#
RI#
8P4R-10K
RP58
SWI_#
SMLINK1
SMLINK0
RP59
PDAT_SMB
PCLK_SMB
SMBALERT#
SMB_LINK_ALERT#
R591 *10K SUSC#
R710 10K ICH_THRM#
R711 10K SCI_#
R593 680R PCIE_WAKE#
1. Change the power plane of PCIE_WAKE# from 3VSUS to 3V_S5 to solve system can't turn off issue.
2. Change the power plane of ICH_THRM# and SCI_# from 3VSUS to +3V to solve leakage issue.
Sting 10/06/2004
3V_S5
R594 *10K
C832 *0.1U
U44A
U44B
*NC7WZ14P6X
R596 *1K
R598 *0R
RSMRST#
Enable Cable ID
RN151
8P4R-10K
LCDID0
LCDID1
LCDID2
PROJECT : CT3
Quanta Computer Inc.
Size Custom
Document Number ICH6-M (USB/HUB/LPC)
Rev 2A
Date: Monday, December 27, 2004
Sheet 11 of 39



PROJECT : CT3		
Quanta Computer Inc.		
Size: Custom	Document Number: ICH6-M (POWER)	Rev: 2A
Date: Monday, December 27, 2004	Sheet 12 of 39	


SODIMM0
CN14
PC2100 DDR SDRAM SO-DIMM (200P)
AMP_DDR_SODIMM_H5.2
CLOCK 0,1
CKE 0,1
SMbus address A0
SODIMM1
CN13
PC2100 DDR SDRAM SO-DIMM (200P)
AMP_DDR_SODIMM_H9.2
CLOCK 3,4
CKE 2,3
SMbus address A1
2.5VSUS
SMDDR_VREF
SMDDR_VTERM
+3V
C937 C938 C939 C940 C941 C942 C943 C944 C945 C946
C947 C948 C949 C950 C951 C952 C953 C954 C955 C956
C957 C958 C959 C960 C961 C962 C963 C964 C965 C966
C967 C968 C969 C970 C971 C972 C973 C974 C975 C976
C977 C978 C979 C980 C981 C982 C983 C984 C985
C986 C987 C988 C989
C990 150U/6.3V_7
C991 150U/6.3V_7
0.1U
R634 200R
R636 200R
R635 200R
R637 200R
R638 *10K
R639 *10K
C992 0.1U
C993 0.1U
PROJECT : CT3
Quanta Computer Inc.
DDR1 DIMM
Size
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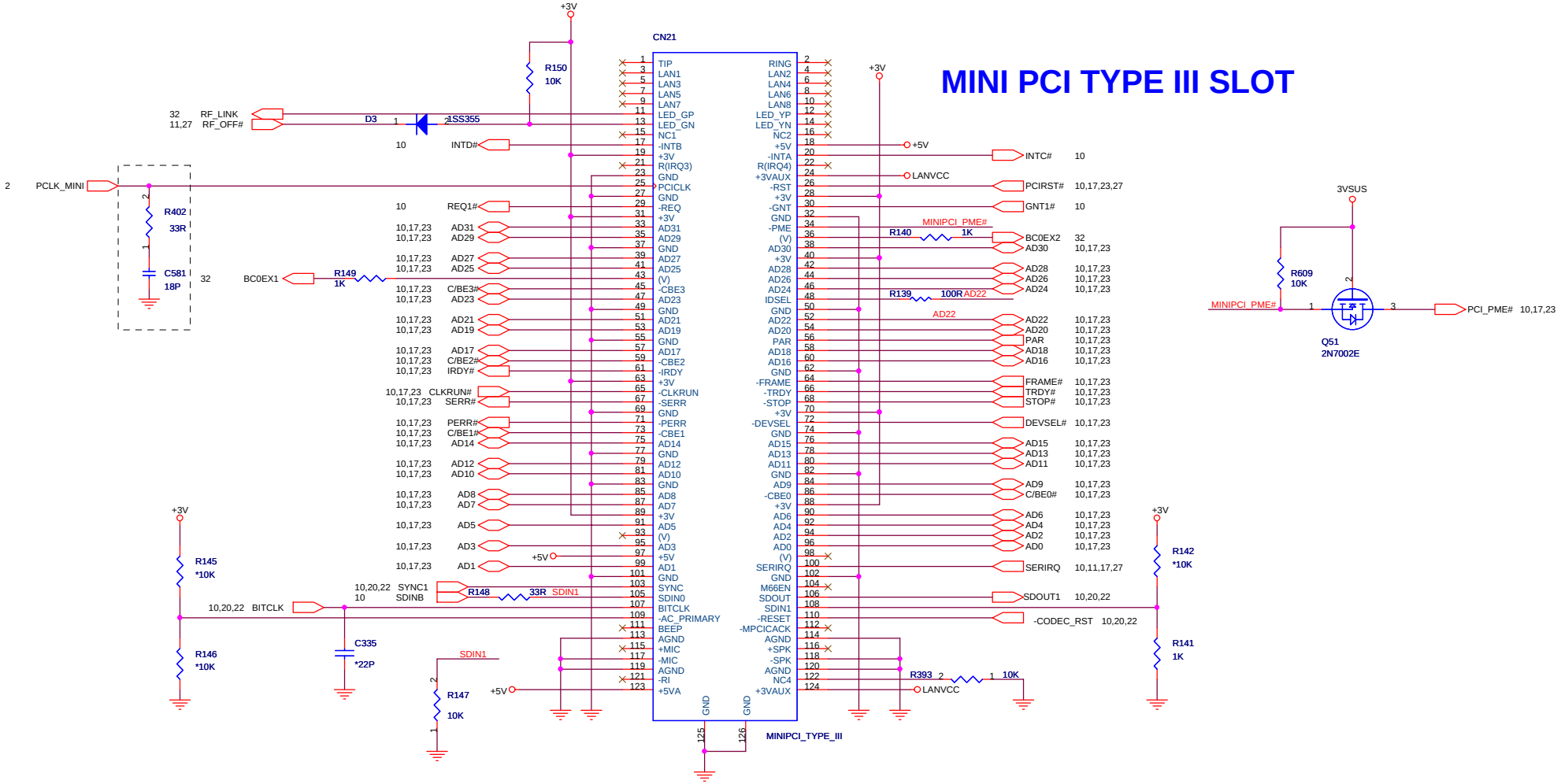
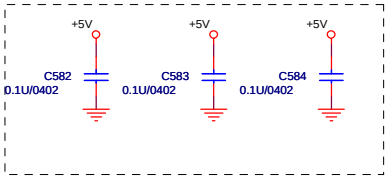
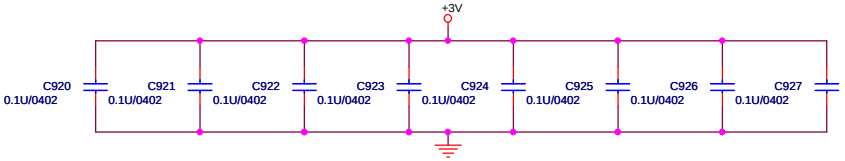
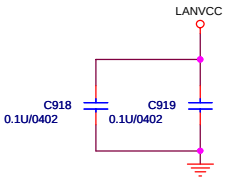
MINI PCI TYPE III SLOT

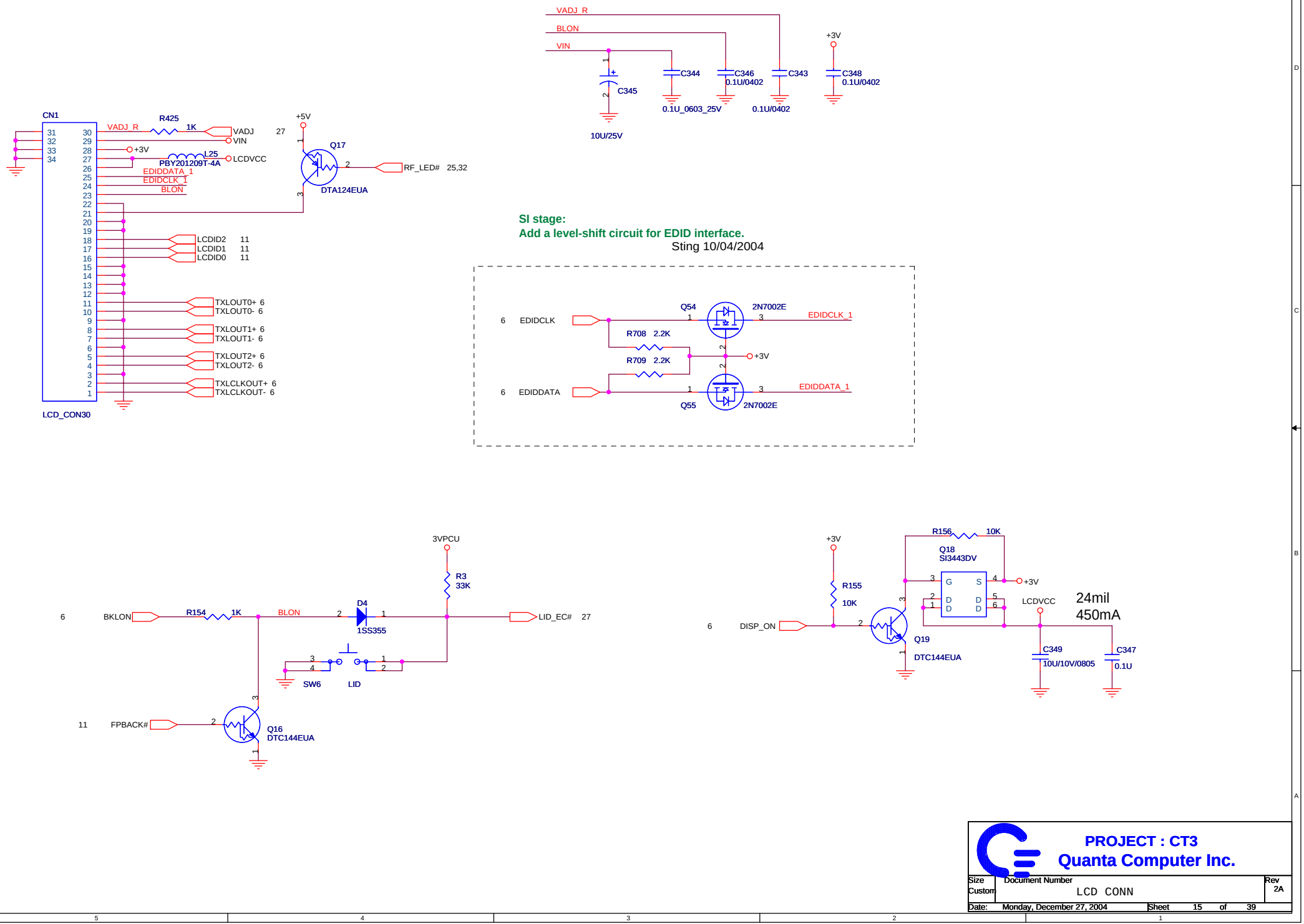








PROJECT : CT3			
Quanta Computer Inc.			
Size: Custom	Document Number: MINIPCI_TYPE_III		Rev: 1A
Date: Monday, December 27, 2004	Sheet 14 of 39		



PROJECT : CT3		
Quanta Computer Inc.		
Size: Custom	Document Number: LCD CONN	Rev: 2A
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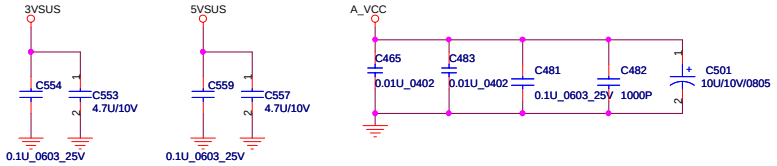
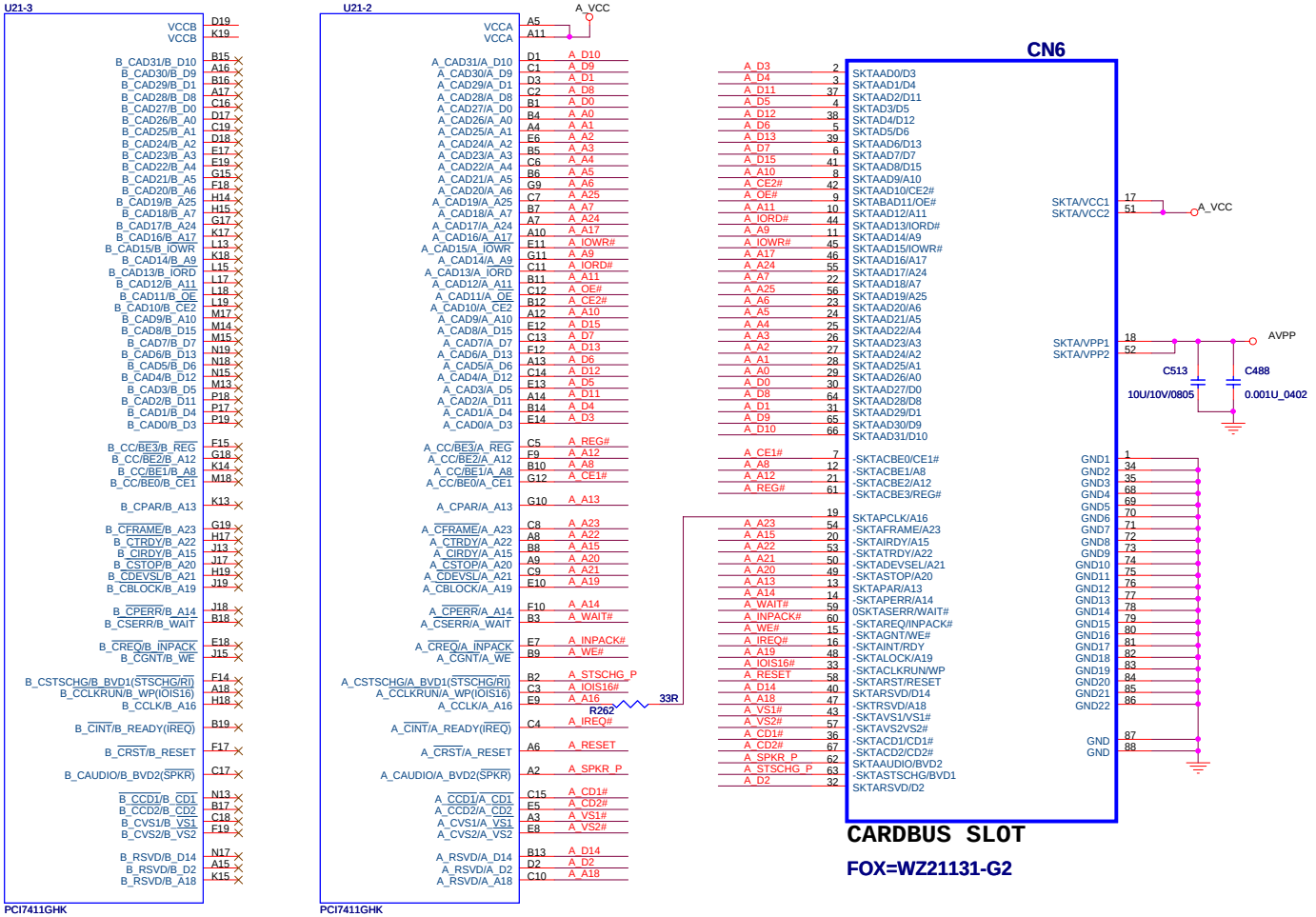
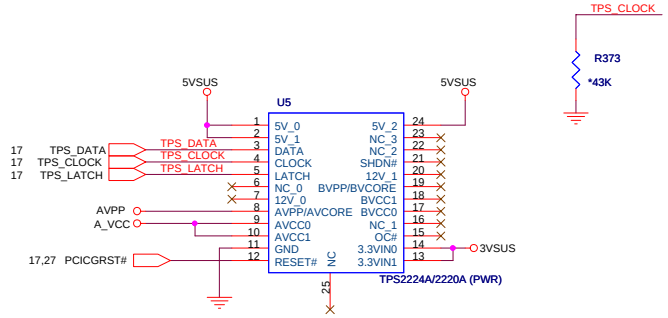
CardBus Connector





CARDBUS POWER SWITCH

For PCI7411



For PCI1510

PV stage:
Remove unused PCI1510RVGF circuit.

Griffey 12/08/2004

PROJECT : CT3			
Quanta Computer Inc.			
Size: Custom	Document Number: CardBus Connector		Rev: 1A
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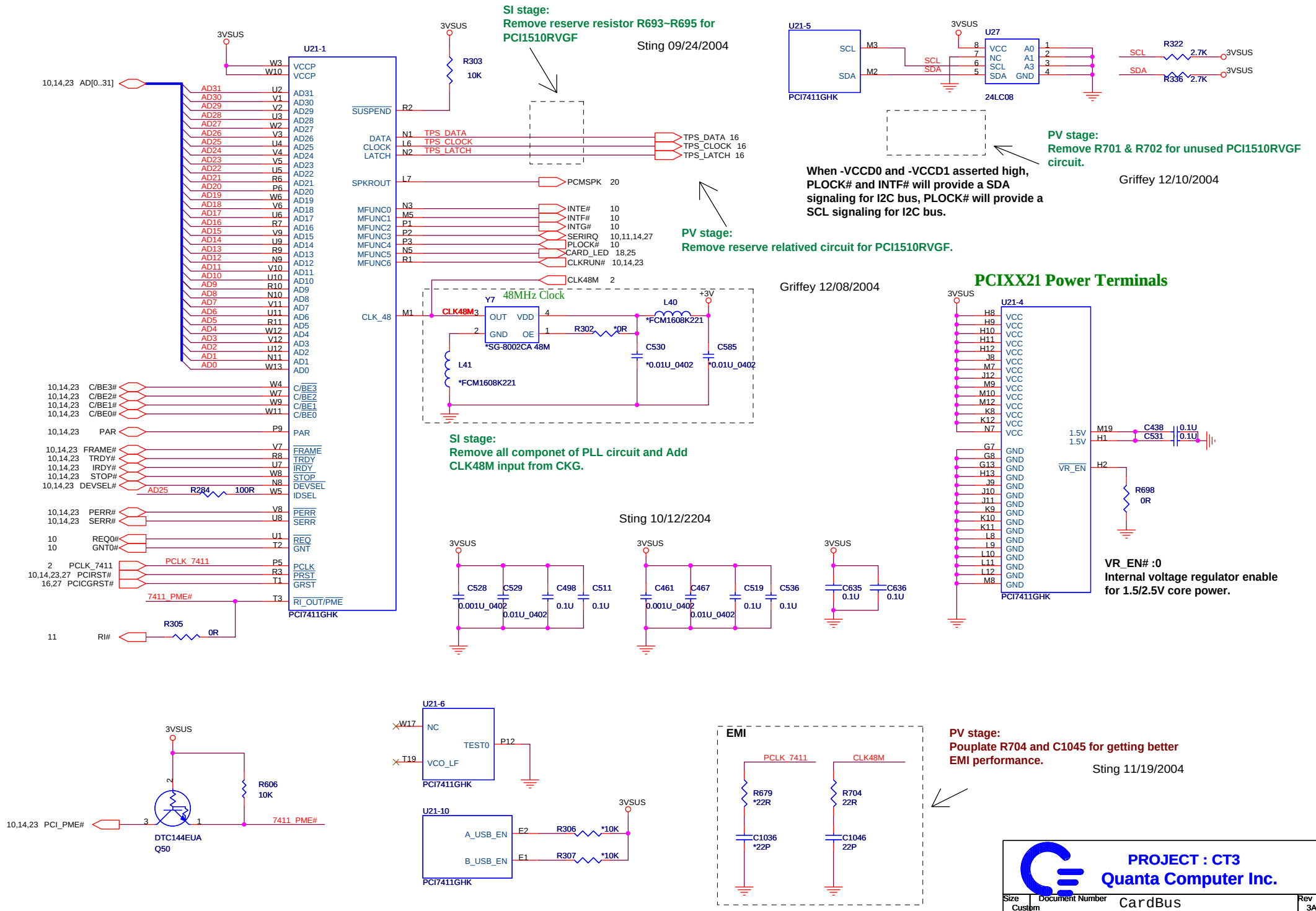
CardBus


SI stage:
Remove reserve resistor R693~R695 for PCI1510RVGF
Sting 09/24/2004
PV stage:
Remove R701 & R702 for unused PCI1510RVGF circuit.
Griffey 12/10/2004
When -VCCD0 and -VCCD1 asserted high, PLOCK# and INTF# will provide a SDA signaling for I2C bus, PLOCK# will provide a SCL signaling for I2C bus.
PV stage:
Remove reserve relatived circuit for PCI1510RVGF.
Griffey 12/08/2004
PCIXX21 Power Terminals
SI stage:
Remove all componet of PLL circuit and Add CLK48M input from CKG.
Sting 10/12/2204
VR_EN# :0
Internal voltage regulator enable for 1.5/2.5V core power.
EMI
PV stage:
Pouplate R704 and C1045 for getting better EMI performance.
Sting 11/19/2004
PROJECT : CT3
Quanta Computer Inc.
CardBus
Monday, December 27, 2004
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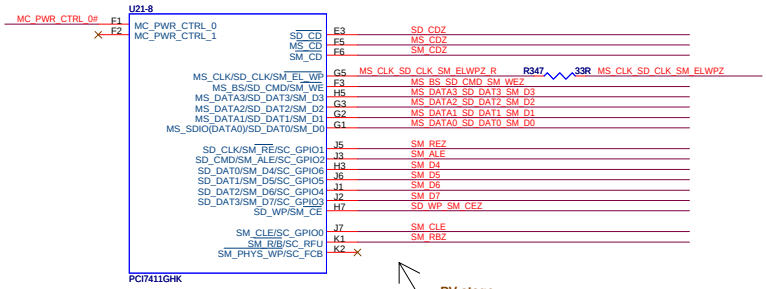
CARD POWER CONTROL

PV stage:
Remove reserve relatived circuit for PCI1510RVGF.

Griffey 12/08/2004

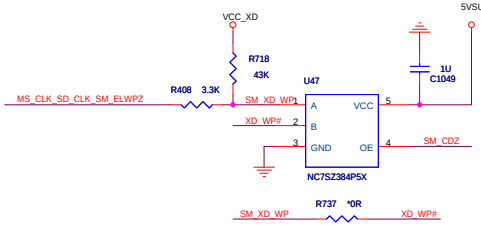
SI stage:
Remove reserve resistor R696 fro PCI1510RVGF.

Sting 10/12/2004



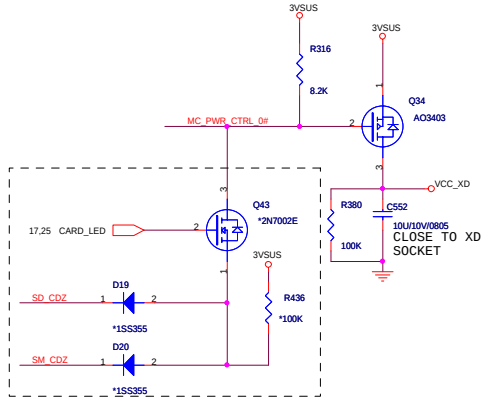
PV stage:
1. Disconnect SM_PHYS_WP.
2. Tie SM_EL_WP with SM_PHYS_WP of SM card to allow for normal operation of SD and SM.

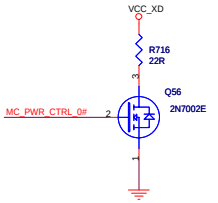
Sting 11/19/2004



PV stage:
1. Add quick switch circuit.

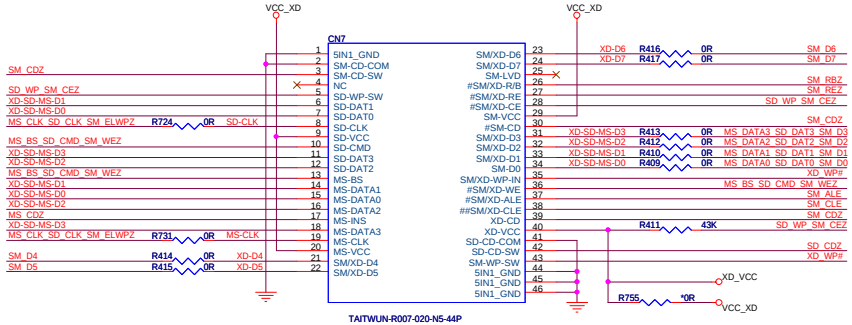
Griffey 12/10/2004

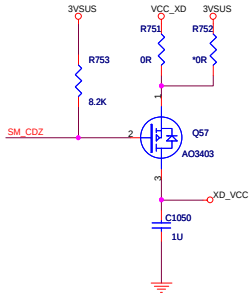




PV stage:
Add a discharge circuit for media card power.

Sting 11/19/2004

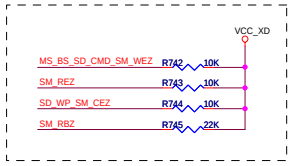




5 IN1 CARD READER

PV stage:
1. Add pull-up circuit.

Griffey 12/20/2004



PV stage:
1. Add R717 to solve SM card can't write protect issue.
2. Add R718 to solve cross-talk issue of MS-PRO card.
3. Add R719~R736 as terminal on all multi-funtion pin.

Sting 11/19/2004

PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
C	CARD READER CONN	3A

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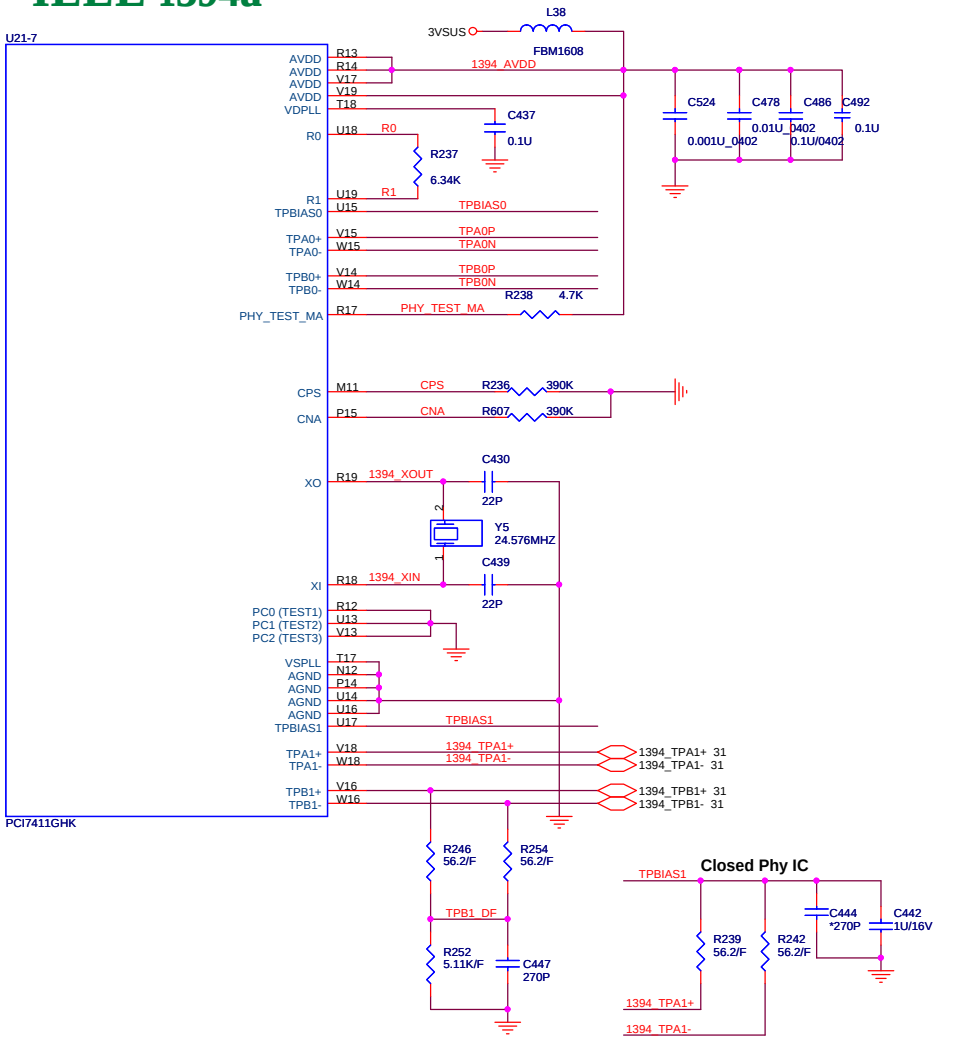
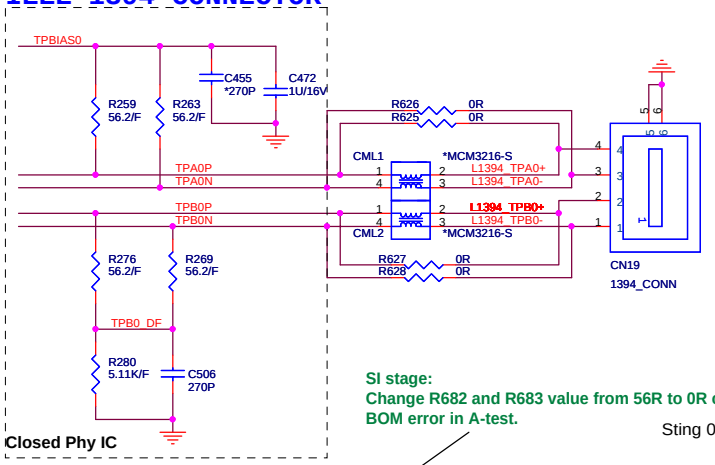
IEEE 1394a

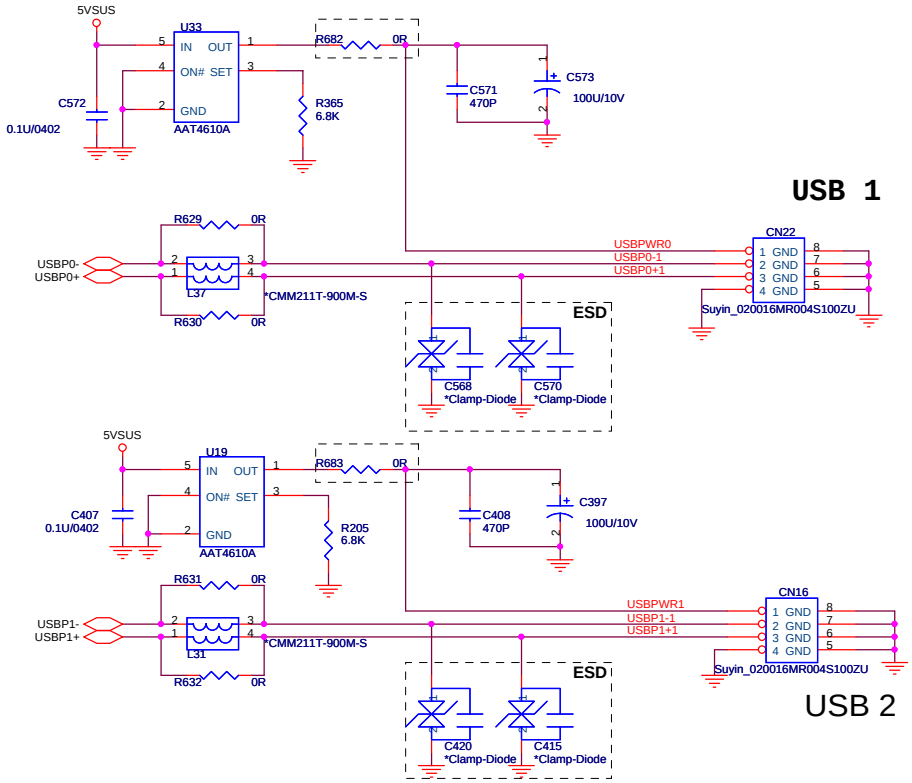


IEEE_1394_CONNECTOR



SI stage:
Change R682 and R683 value from 56R to 0R cause of BOM error in A-test.

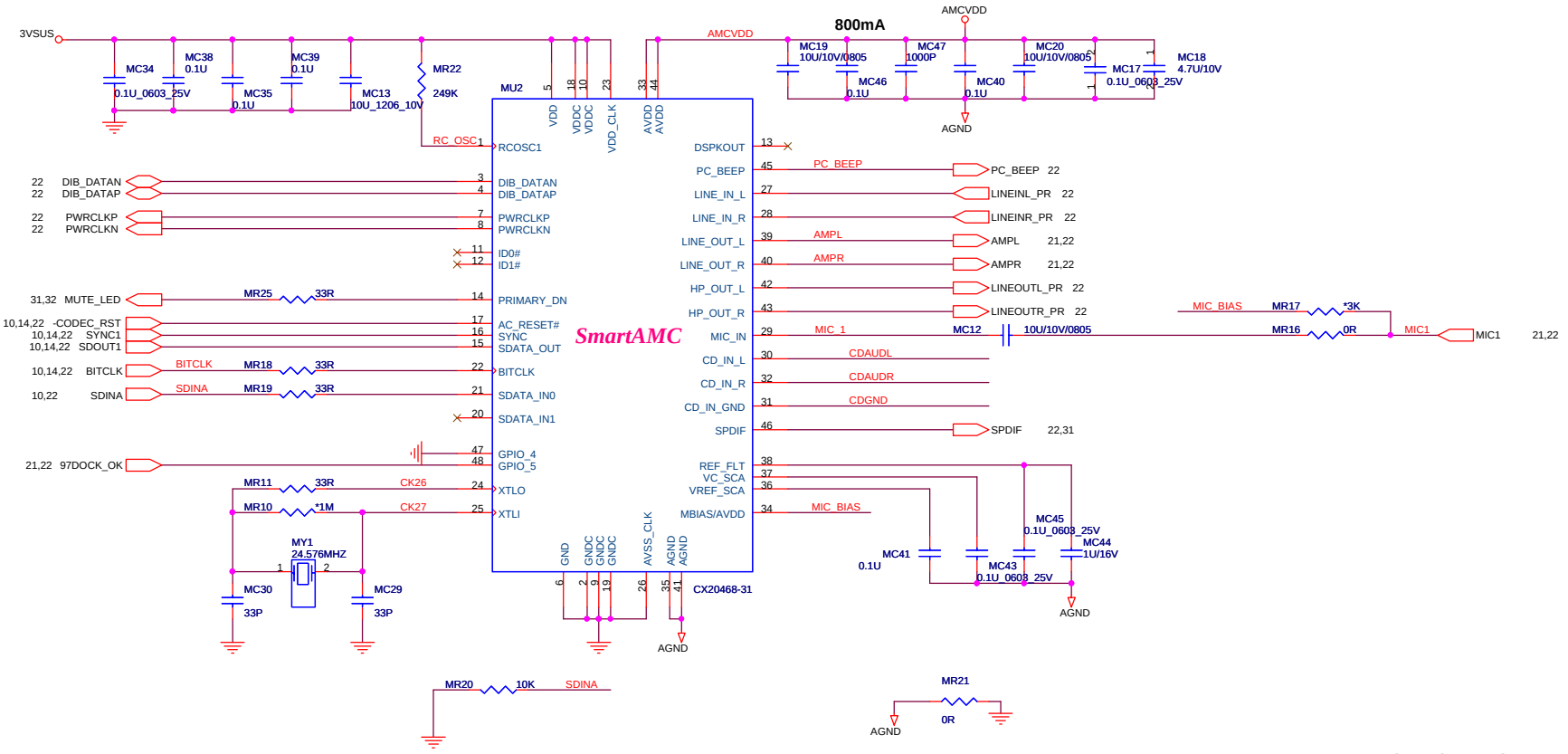
Sting 09/24/2004



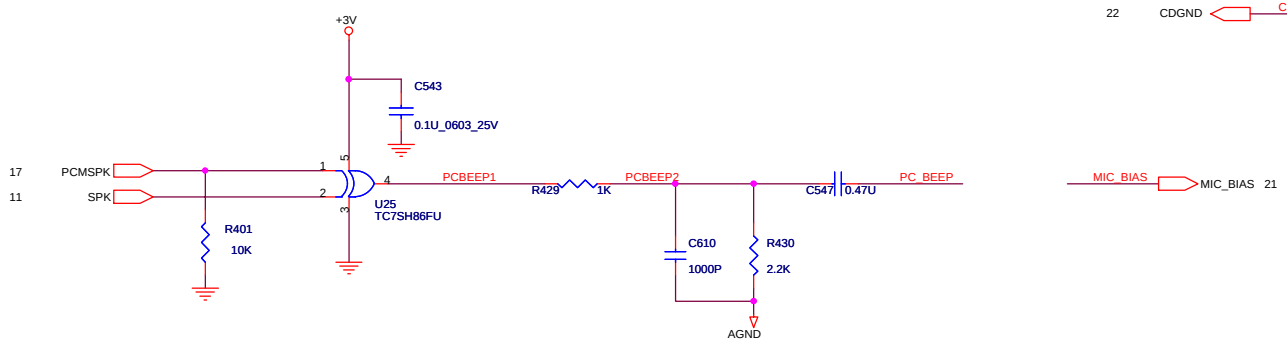
PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	IEEE 1394A, USBX2	2A
Date: Monday, December 27, 2004	Sheet 19 of 39	

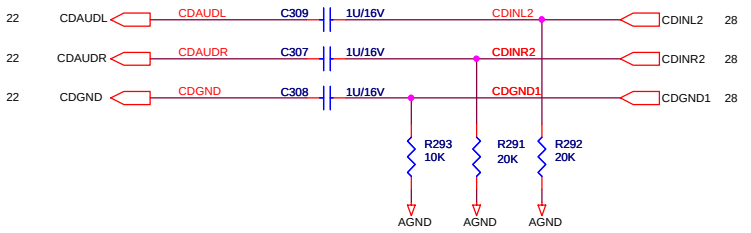
The AMC20493-001 modem is used for mother board family MBAMC20493-010.



PC SPEAKER



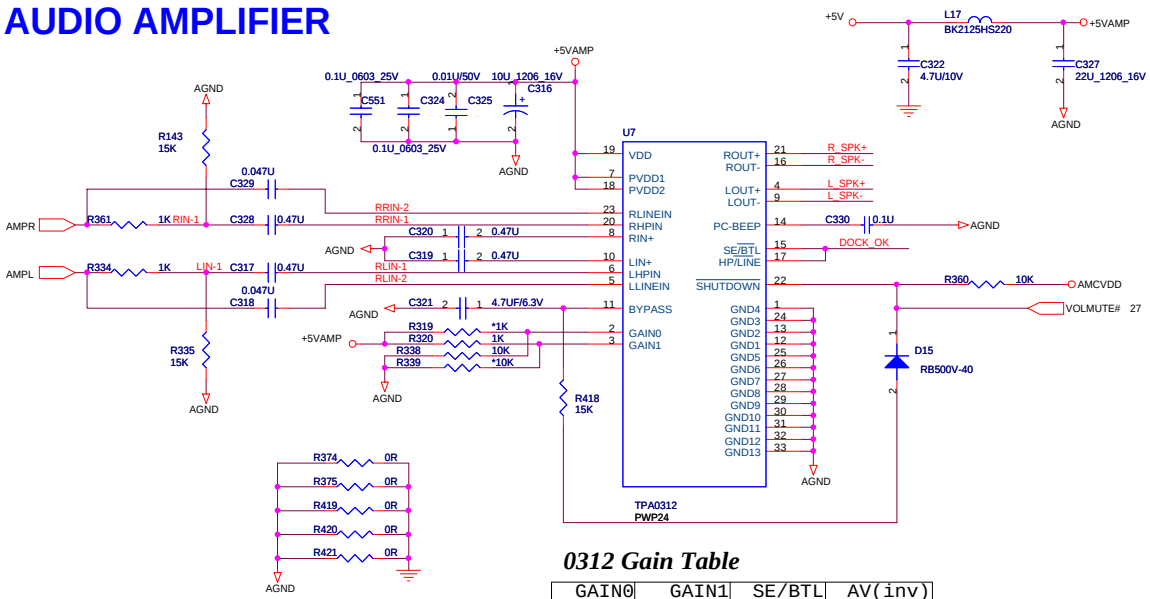
FROM CD-ROM



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
	AMC97 CODEC	1A
Date: Monday, December 27, 2004	Sheet 20 of 39	

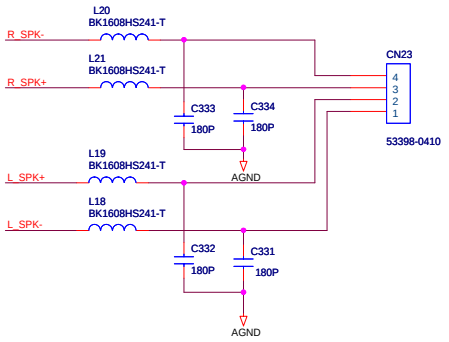
AUDIO AMPLIFIER

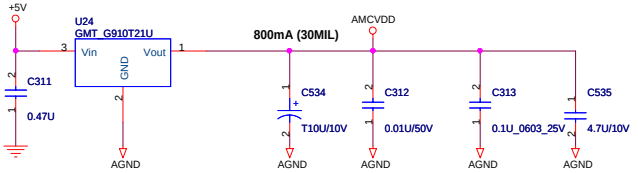


0312 Gain Table

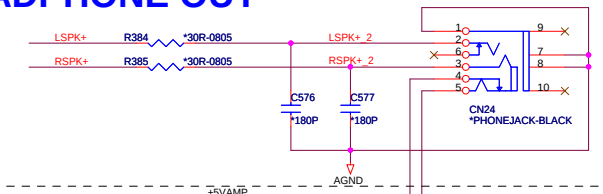
GAIN0	GAIN1	SE/BTL	AV(inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

SPEAKER OUT

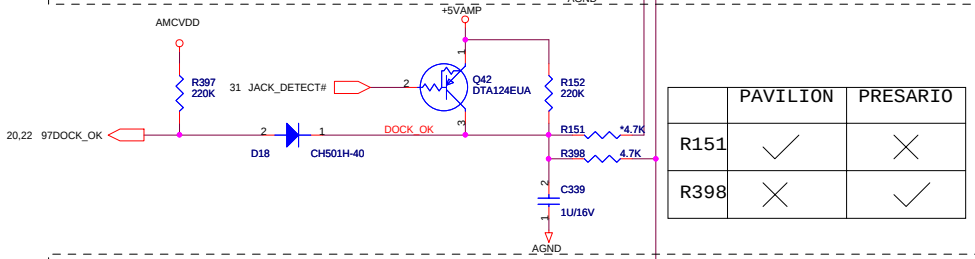




2ND HEADPHONE OUT

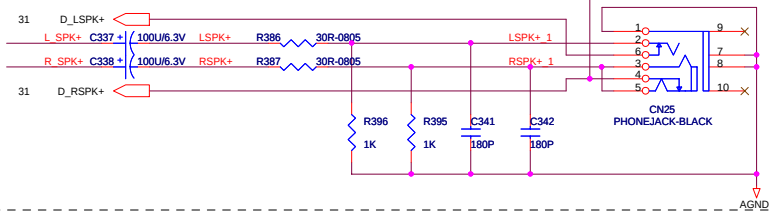


PAVILION



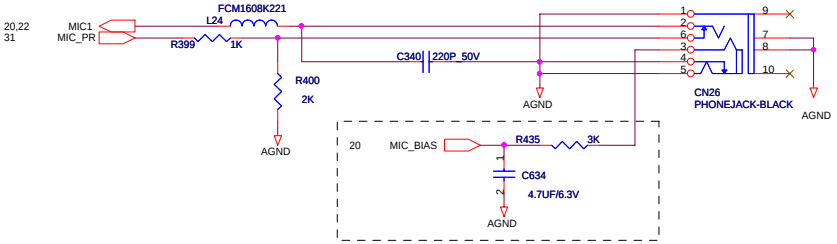
	PAVILION	PRESARIO
R151	✓	✗
R398	✗	✓

HEADPHONE OUT



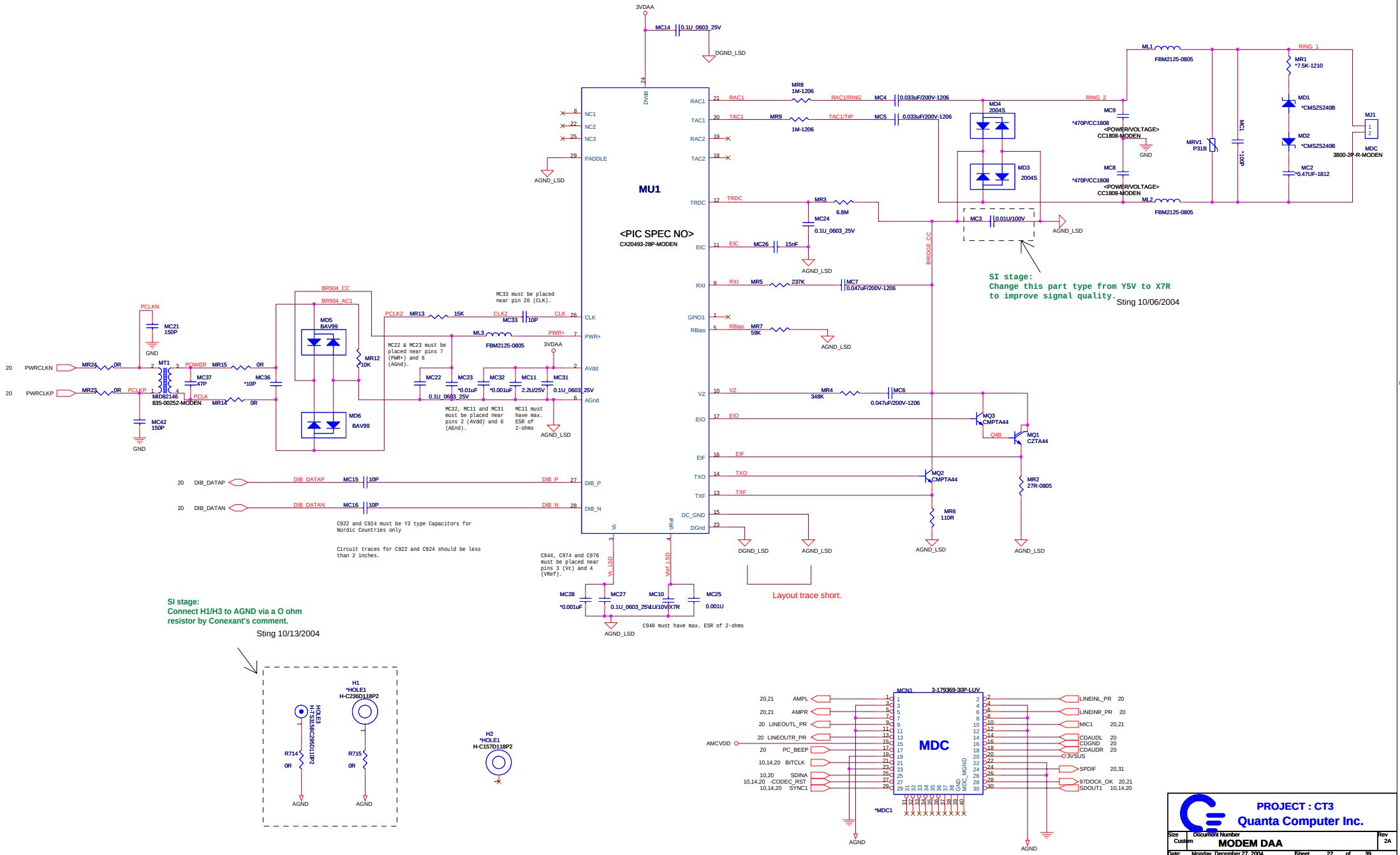
PAVILION
PRESARIO

MICROPHONE



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP_ TI-TPA0312	1A
Date: Monday, December 27, 2004	Sheet 21 of 39	


MU1
<PIC SPEC NO>
CX20493-28P-MODEN
3VDAA
DGND_LSD
AGND_LSD
SI stage:
Change this part type from Y5V to X7R
to improve signal quality.
Sting 10/06/2004
SI stage:
Connect H1/H3 to AGND via a O ohm
resistor by Conexant's comment.
Sting 10/13/2004
Layout trace short.
C922 and C924 must be Y3 type Capacitors for Nordic Countries only
Circuit traces for C922 and C924 should be less than 2 inches.
MC33 must be placed near pin 26 (CLK).
MC22 & MC23 must be placed near pins 7 (PWR+) and 6 (AGnd).
MC32, MC11 and MC31 must be placed near pins 2 (AVdd) and 6 (AGnd).
MC11 must have max. ESR of 2-ohms
C944, C974 and C976 must be placed near pins 3 (Vc) and 4 (VRef).
C940 must have max. ESR of 2-ohms
MDC
3800-2P-R-MODEN
MCN1
3-179369-30P-LUV
*MDC1
PROJECT : CT3
Quanta Computer Inc.
MODEM DAA
Size: Custom
Document Number
Rev: 2A
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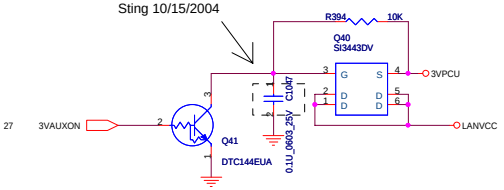
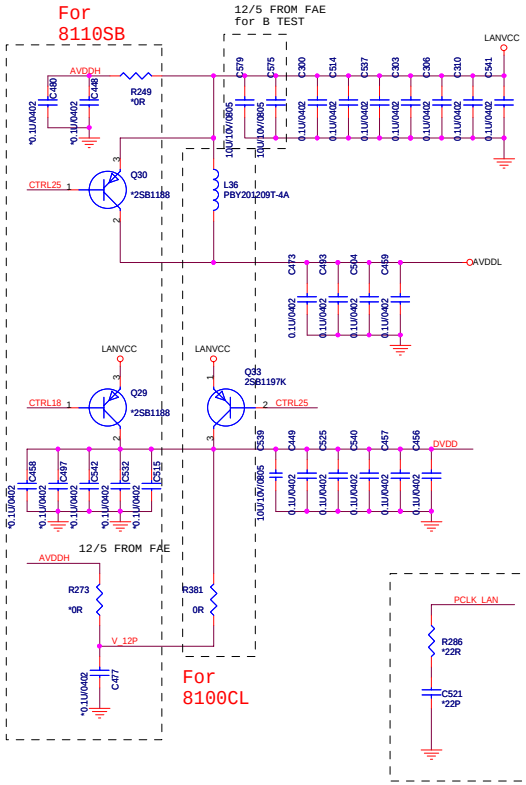
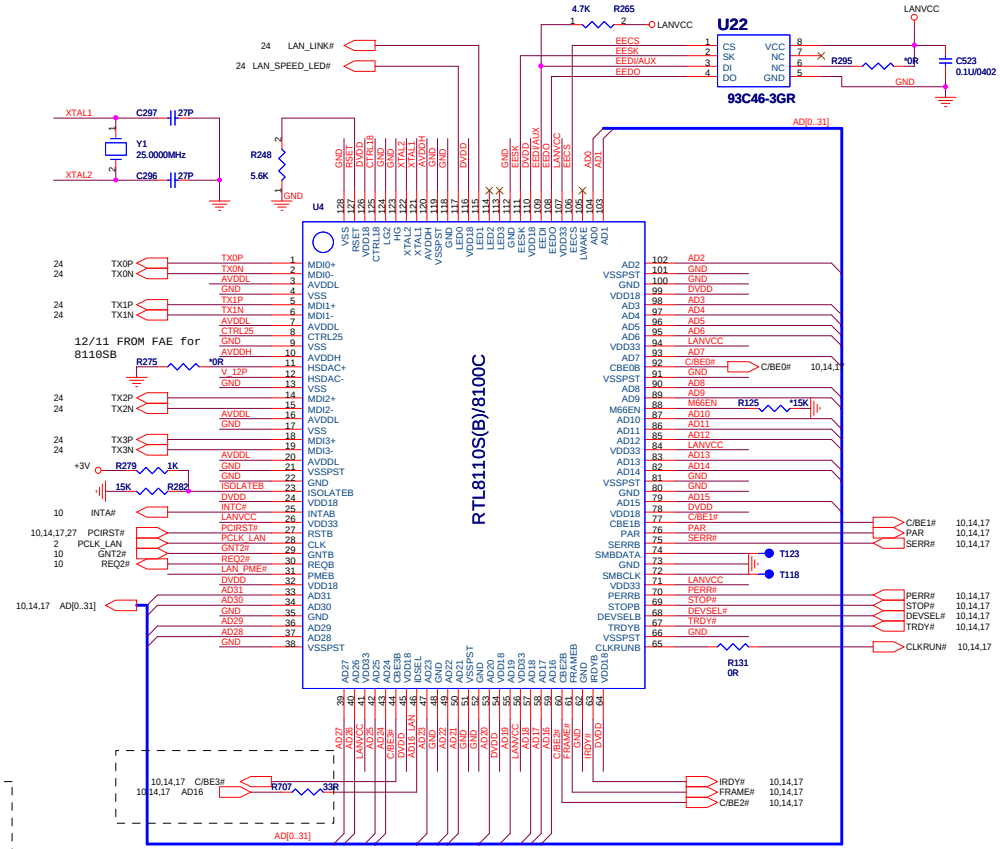
	8100CL(10/100M)	8110SB(1G)
DVDD33	3.3VD 26,41,56,71,84,94,107	3.3VD 26,41,56,71,84,94,107
AVDDL	3.3VA 3,7,20	2.5VA 3,7,20,16
DVDD	2.5VD 32,54,78,99	1.8VD 32,54,78,99,24,45,64,110,116,126
AVDD25	2.5VA 12	NC
AVDDH	NC	3.3VA 10,120

SI stage:
Add a 0.1uF to make Q40 turn on slowly, because 3VPCU will drop when LANVCC turned on quickly. it will make EC state machine crazy.

Sting 10/15/2004

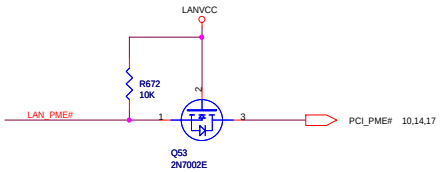






SI stage:
Add R707 for ID selection of Lan controller.

Sting 10/04/2004

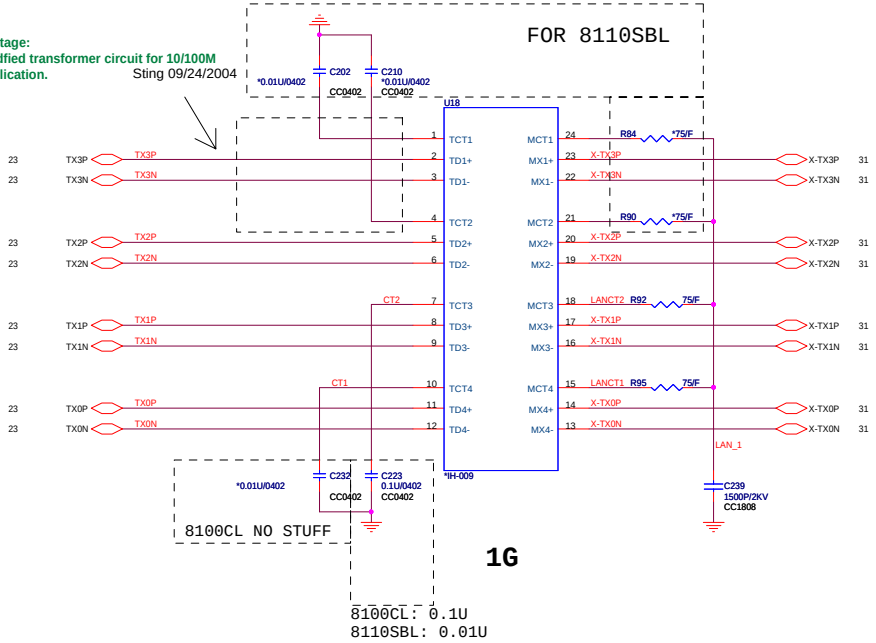


PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
C	RTL8100CL / RTL8110SB	2A
Date: Monday, December 27, 2004	Sheet 23 of 39	

SI stage:
Modfied transformer circuit for 10/100M application.
Sting 09/24/2004

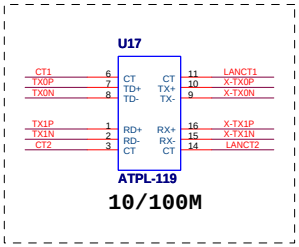
FOR 8110SBL



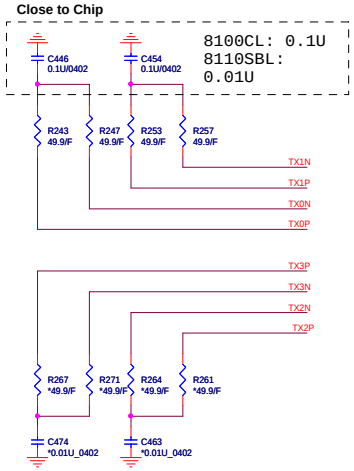
8100CL NO STUFF

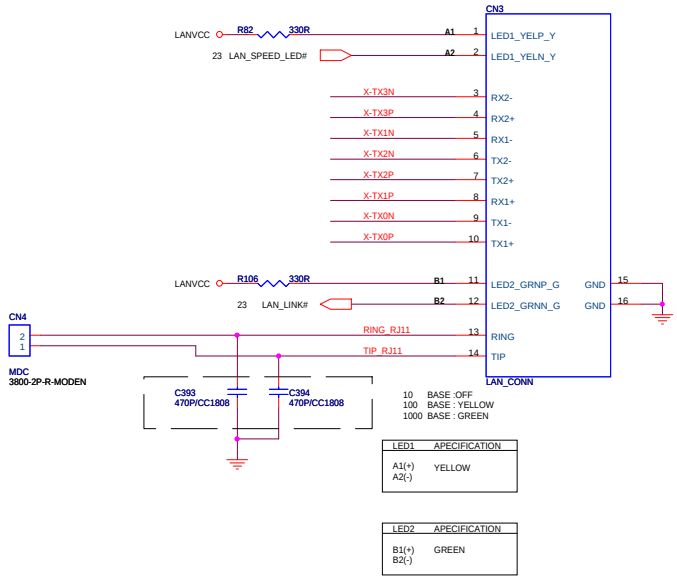
1G

8100CL: 0.1U
8110SBL: 0.01U



Close to Chip





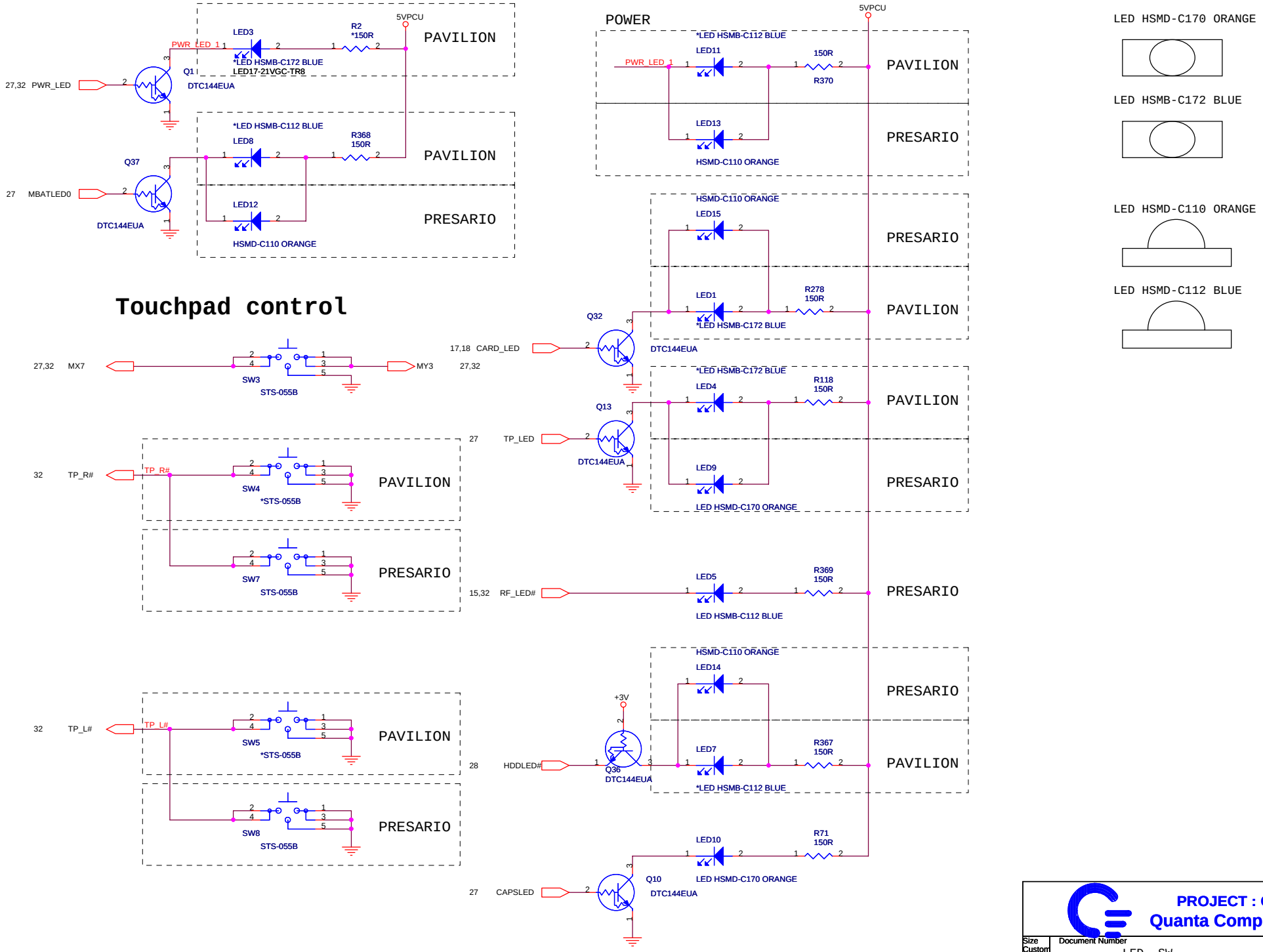
LED1	APECIFICATION
A1(+) A2(-)	YELLOW

LED2	APECIFICATION
B1(+) B2(-)	GREEN

PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
C	LAN, RJ11, RJ45	2A

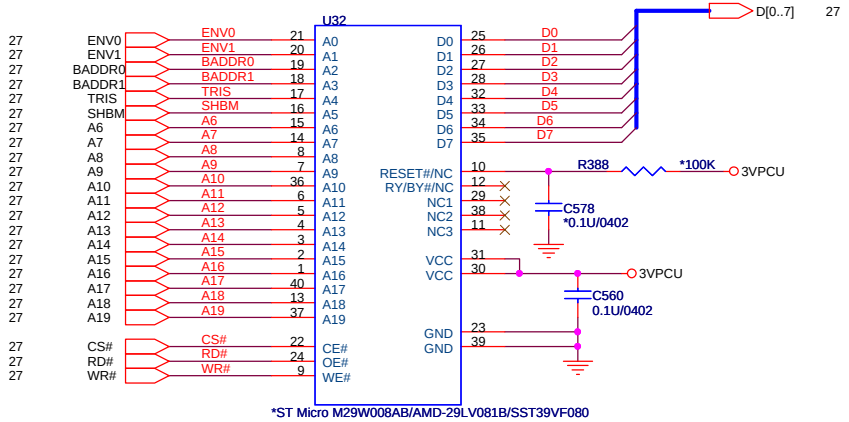
Date: Monday, December 27, 2004 Sheet 24 of 39



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED, SW	1A
Date: Monday, December 27, 2004	Sheet 25 of 39	

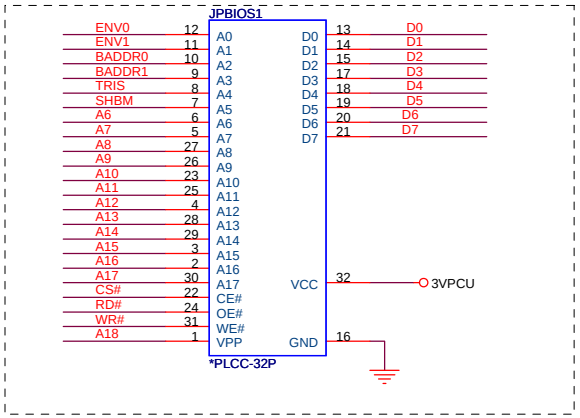
8Mbit (1M Byte), TSSOP40



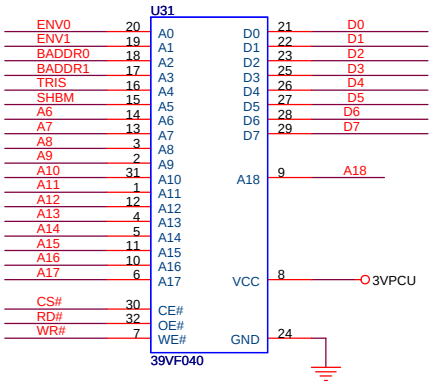
1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
2.SIO has internal 20 mS delay of VCC1_PWROK

AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

SI stage:
Add PLCC32 cause of it is convenient for Bios debugging.
Sting 10/01/2004



4Mbit (512k Byte), TSSOP32



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
B	BIOS ROM	2A
Date: Monday, December 27, 2004	Sheet 26 of 39	

KBC-NS87551L

LDRQ#(pin 8) internal is no use

U23

PC97551

RESERVE FOR 97551

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

I/O Address

BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

SHBM=1: Enable shared memory with host BIOS

CLOSE TO U23

PV stage:
1. Reserve 0R for RF_OFF# and BT_OFF# circuit.
Griffey 12/11/2004

PRESARIO

PAVILION

Pin 24 if no pull-high, will can't reboot.

SI stage:
Add LPC debug port for software team to debug convenient.
Sting 10/06/2004

PV stage:
Modify pin name.
Griffey 12/10/2004

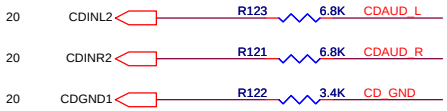
SI stage:
Change R352 value from 120K to 20M.
Sting 09/24/2004

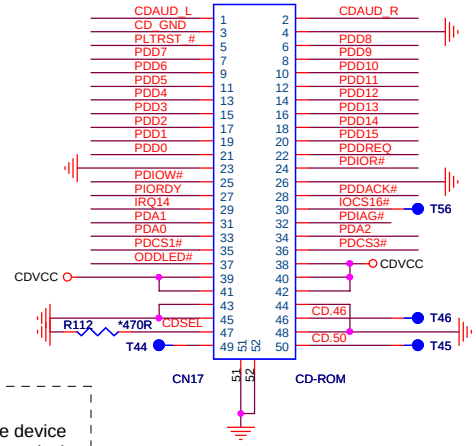
Pin 103 internal is "A19",Can't use to GPIO

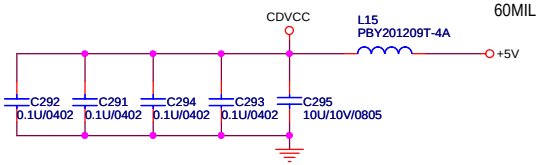
PROJECT : CT3	
Quanta Computer Inc.	
Size: C	Document Number: KBC PCU-97551
Rev: 2A	
Date: Monday, December 27, 2004	Sheet 27 of 39

HDD, CD-ROM

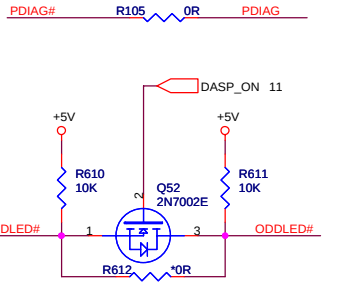
CD-ROM



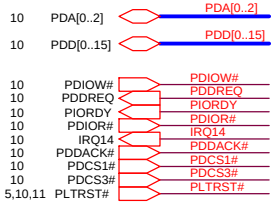


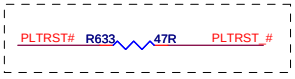


CDSEL
--> NC, Slave device
--> Low, Master device

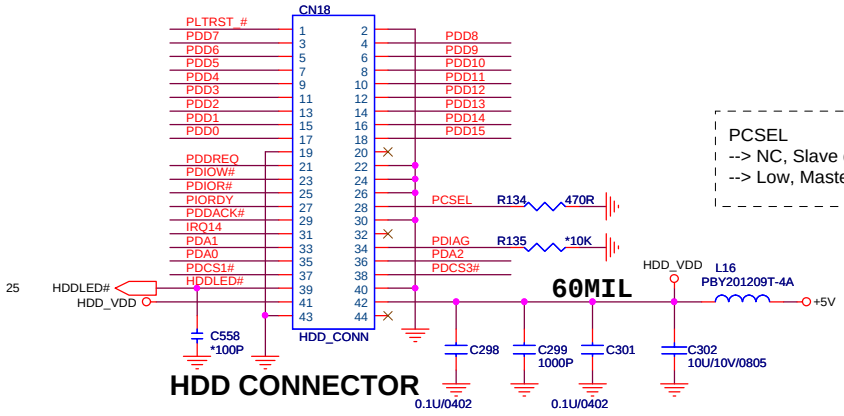


ADD DASP_ON FOR IDE CABLE SELECT



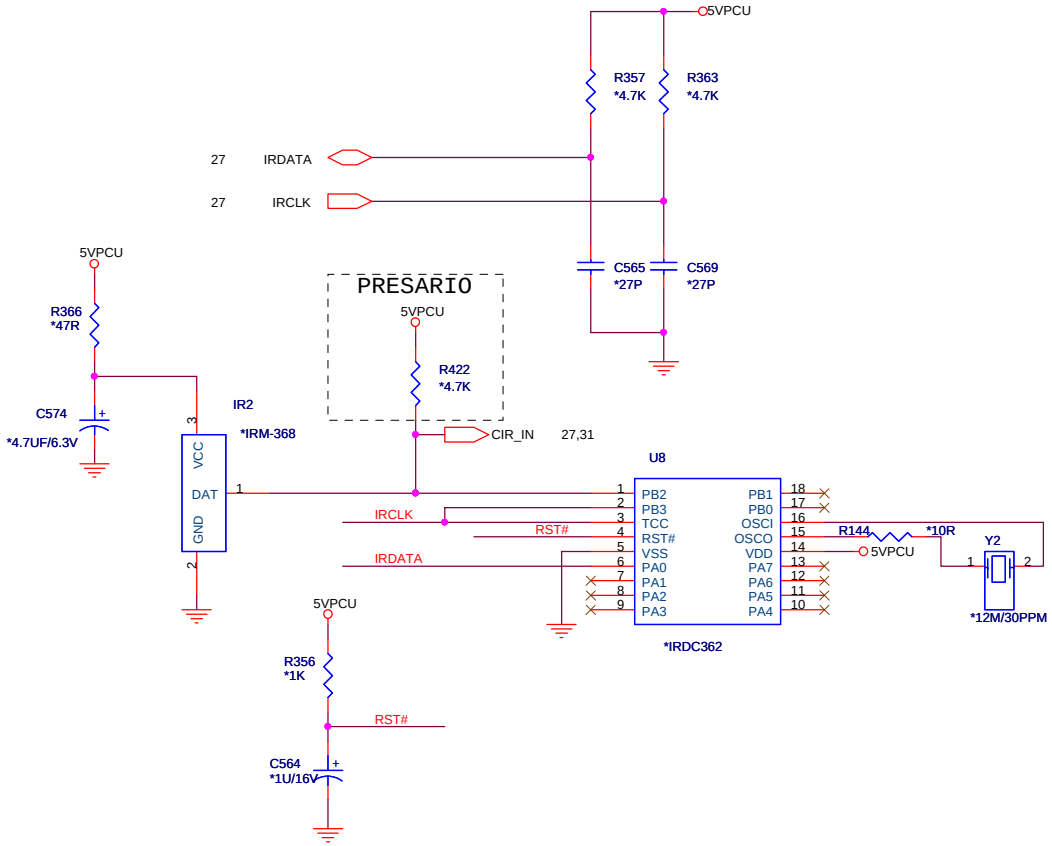


HDD CONNECTOR



PCSEL
--> NC, Slave device
--> Low, Master device

PROJECT : CT3			
Quanta Computer Inc.			
Size: Custom	Document Number: HDD&ODD CONN.		Rev: 2A
Date: Monday, December 27, 2004	Sheet 28 of 39		

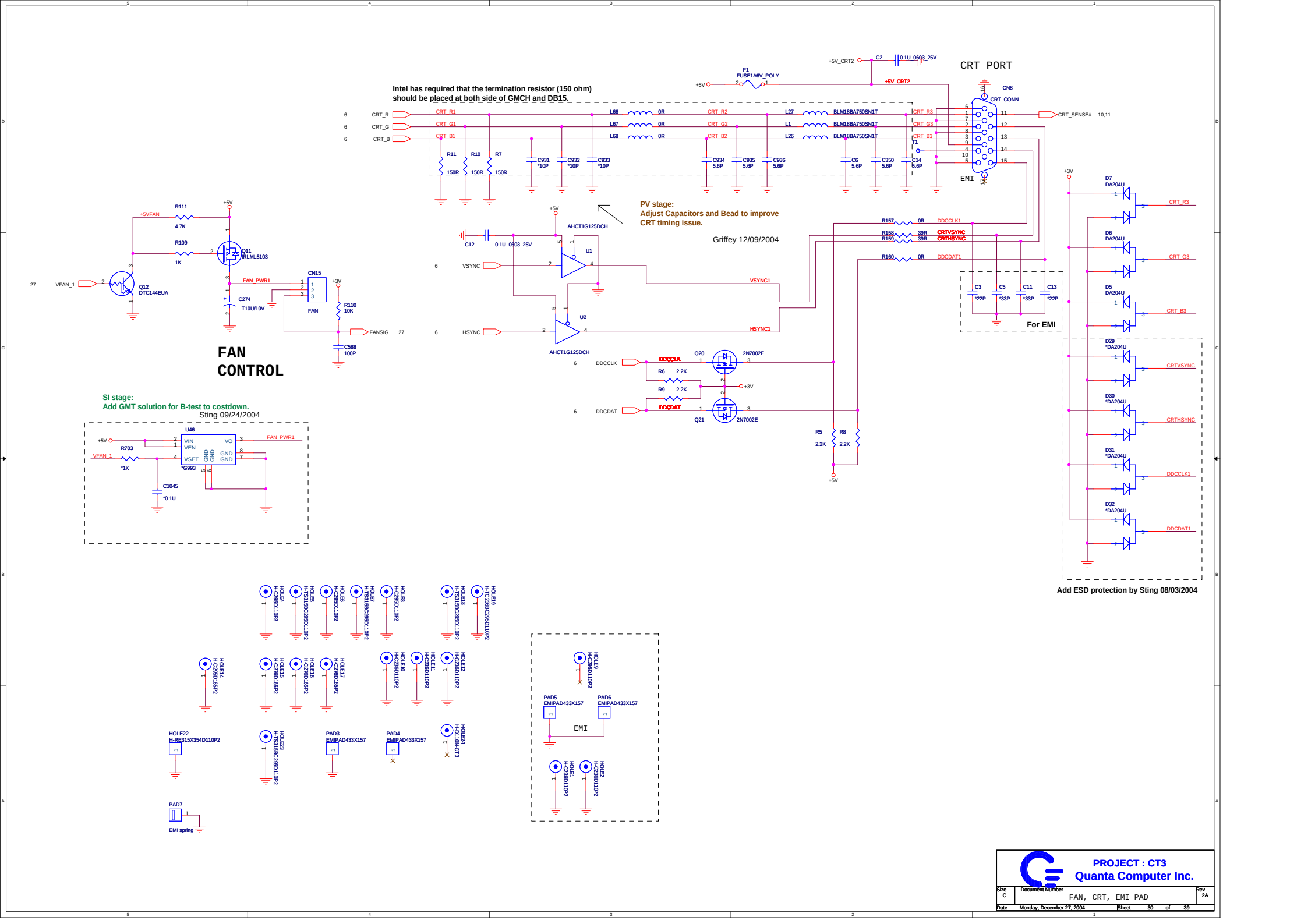


PROJECT : CT3

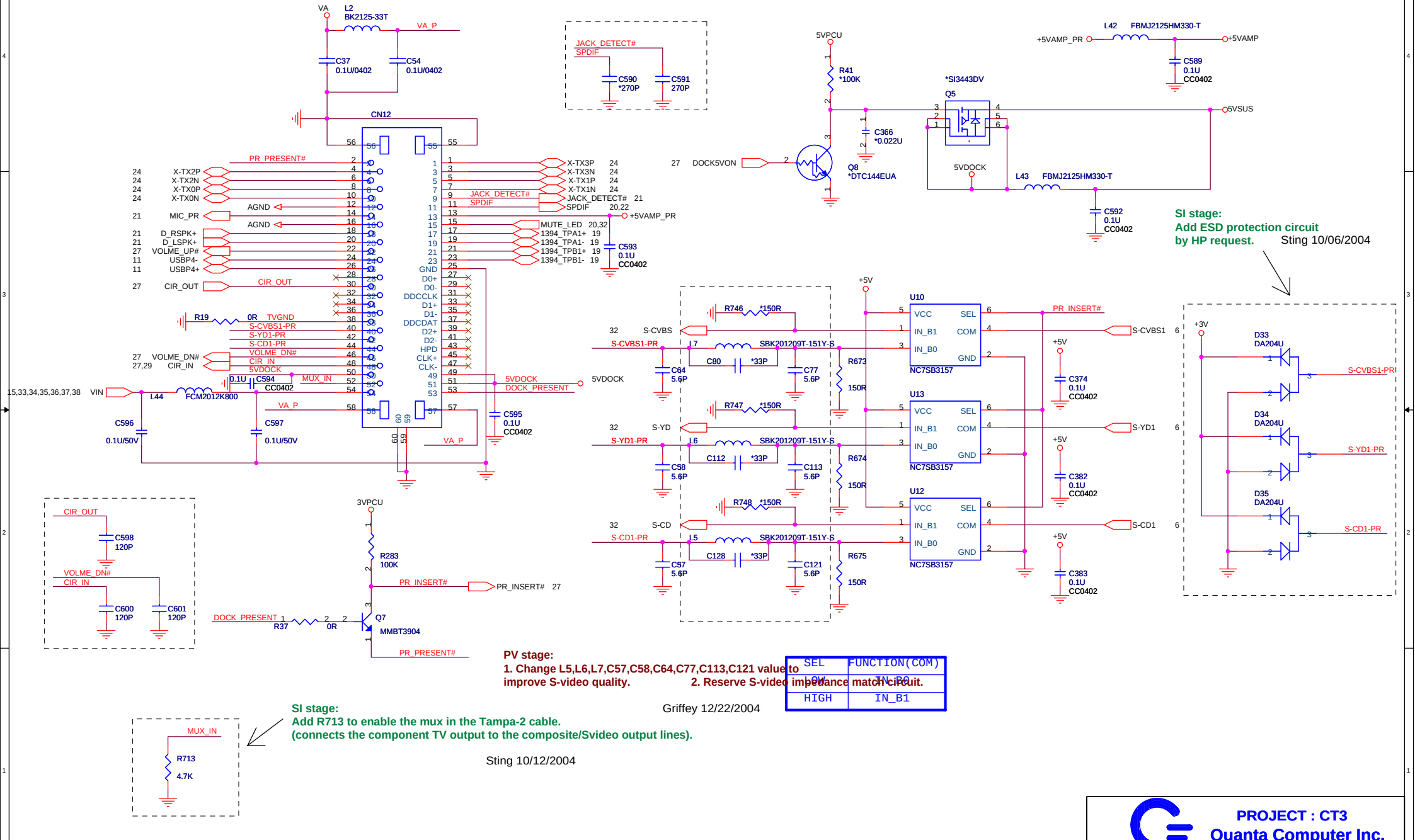
Quanta Computer Inc.

Size	Document Number	Rev
B	REMOTE IRDC362	1A

Date: Monday, December 27, 2004 Sheet 29 of 39



PROJECT : CT3			
Quanta Computer Inc.			
Size: C	Document Number: FAN, CRT, EMI PAD		Rev: 2A
Date: Monday, December 27, 2004	Sheet 30 of 39		



SI stage:
Add ESD protection circuit
by HP request. Sting 10/06/2004

PV stage:
1. Change L5,L6,L7,C57,C58,C64,C77,C113,C121 value to improve S-video quality. **2. Reserve S-video impedance match circuit.** Griffey 12/22/2004

SEL	FUNCTION(COM)
LOW	IN_B0
HIGH	IN_B1

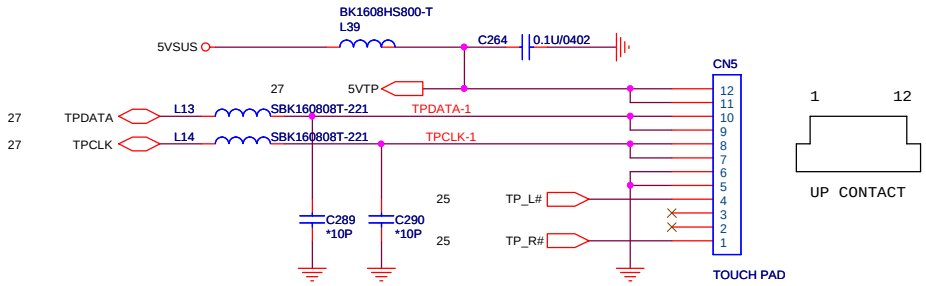
SI stage:
Add R713 to enable the mux in the Tampa-2 cable.
(connects the component TV output to the composite/Svideo output lines).

Sting 10/12/2004

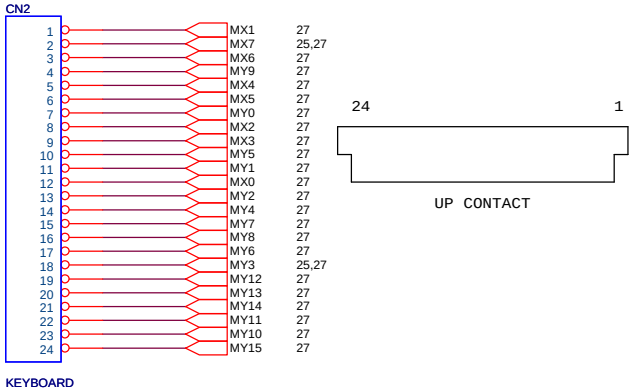
PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CABLE DOCKING	2A
Date: Monday, December 27, 2004	Sheet 31 of 39	

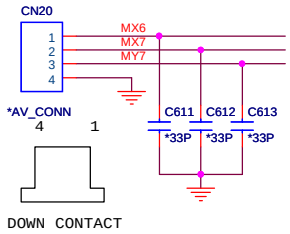
TOUCH PAD CONNECTOR



KEYBOARD CONNECTOR

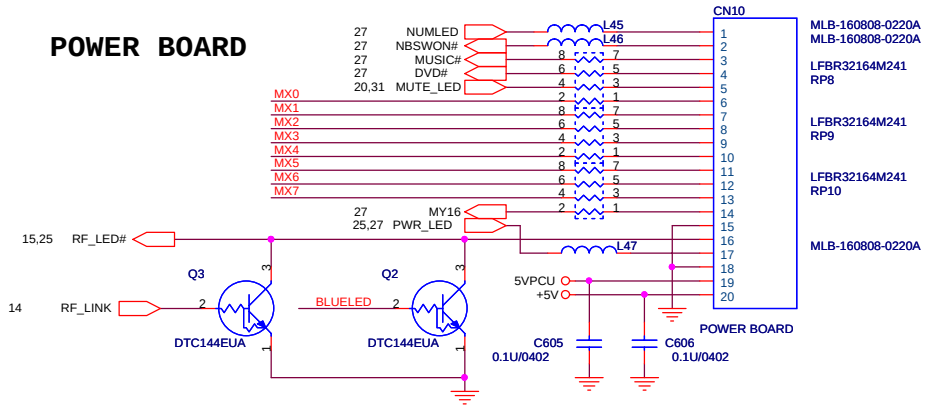


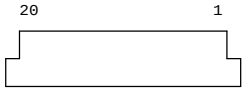
AV BOARD



MX6	MX7
ENTER	MENU

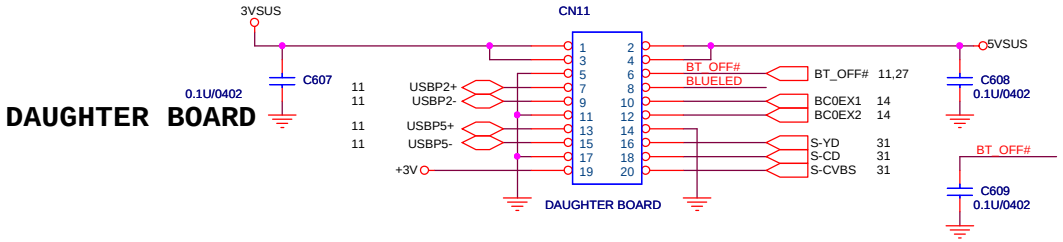
POWER BOARD

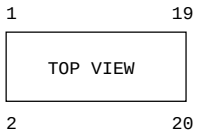




MX0	MX1	MX2	MX3	MX4	MX5	MX6	MX7
BACK	PLAY/PAUSE	FORWARE	STOP	VOL UP	MUTE	VOL DN	WIRELESS

DAUGHTER BOARD





PROJECT : CT3
Quanta Computer Inc.

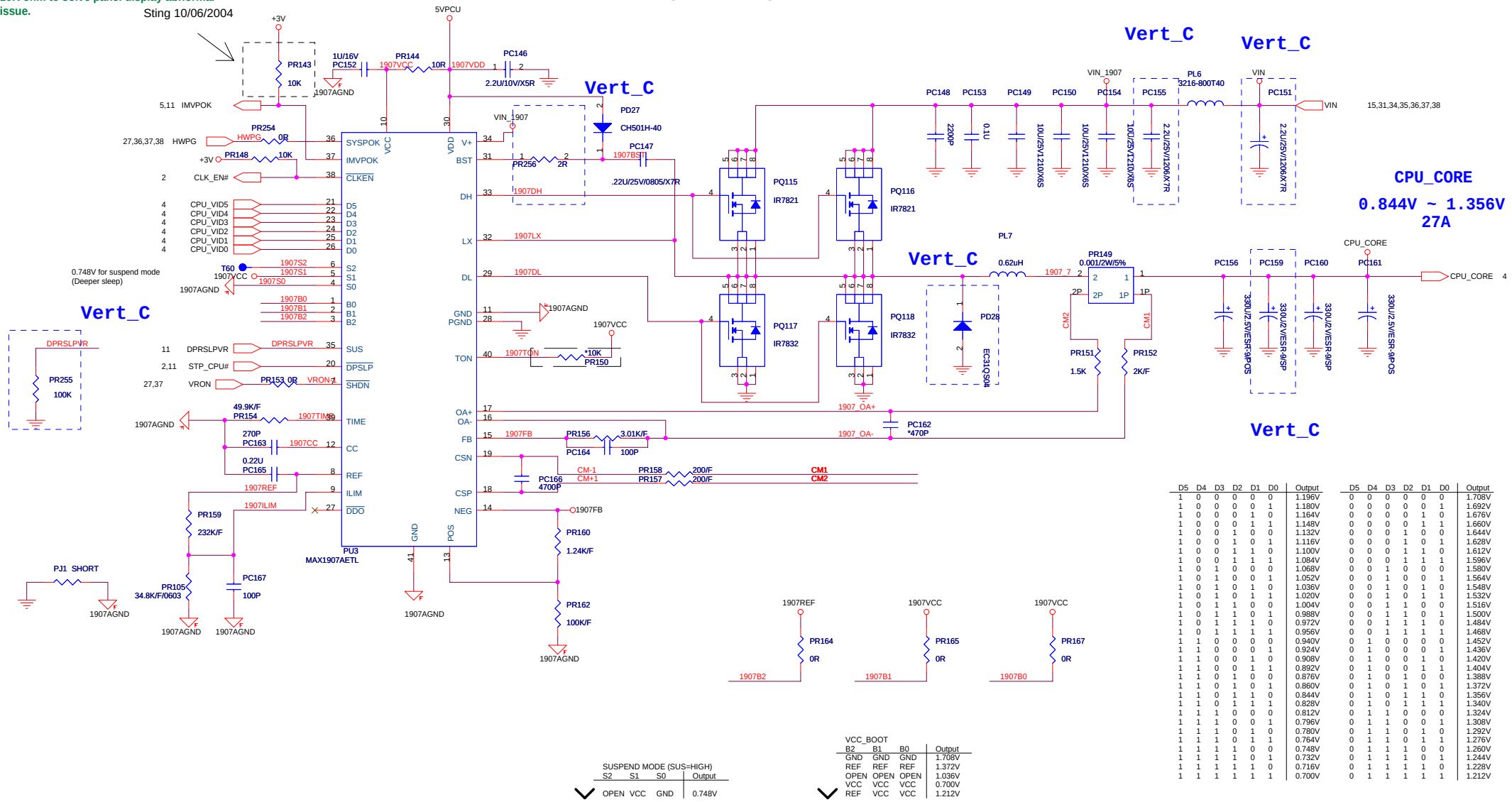
Size	Document Number	Rev
Custom	BLUETOOTH/TP/BTB	1A

Date: Monday, December 27, 2004 Sheet 32 of 39

CPU VCC_CORE (MAX1907)

SI stage:
Change PR143 value from 100K ohms to 10K ohm to solve panel display abnormal issue.

Sting 10/06/2004



SUSPEND MODE (SUS=HIGH)

S2	S1	S0	Output
OPEN	VCC	GND	0.748V

VCC_BOOT

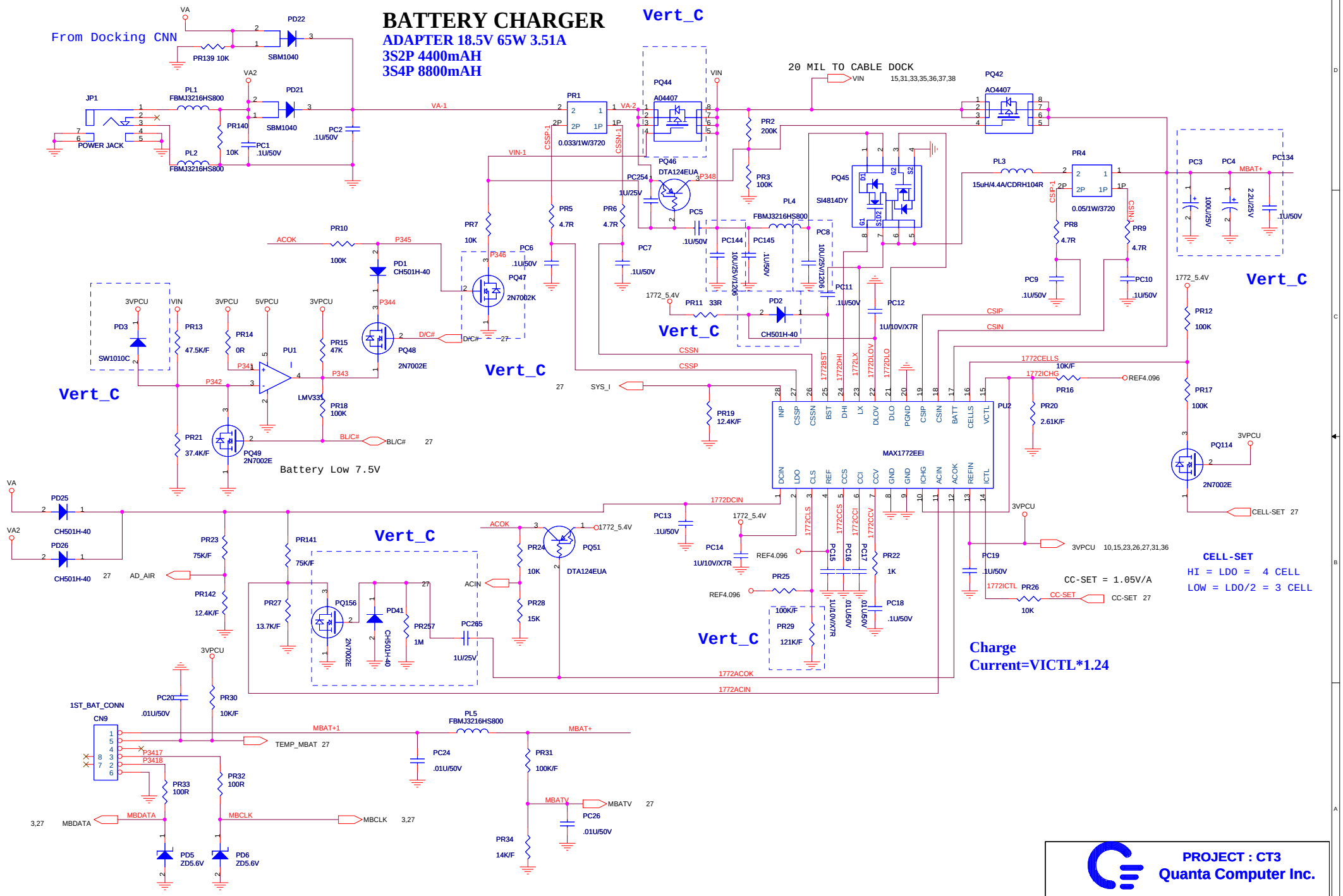
B2	B1	B0	Output
GND	GND	GND	1.708V
REF	REF	REF	1.372V
OPEN	OPEN	OPEN	1.036V
VCC	VCC	VCC	0.700V
REF	VCC	VCC	1.212V

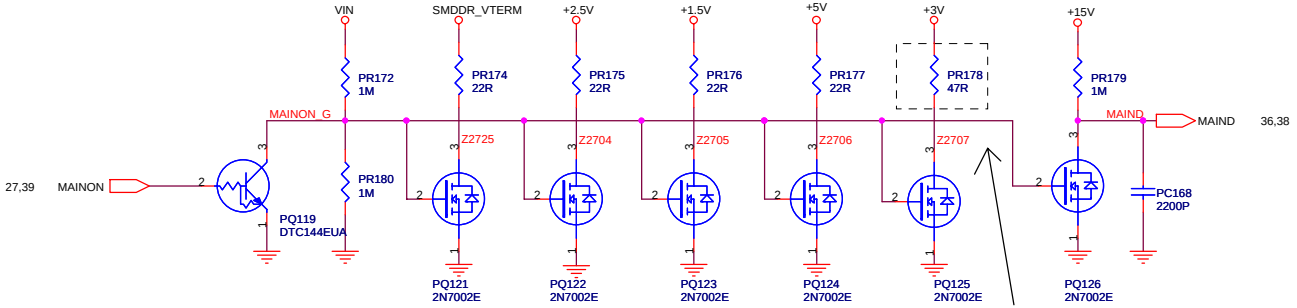
D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V
1	0	0	0	0	1	1.180V
1	0	0	0	1	0	1.164V
1	0	0	0	1	1	1.148V
1	0	0	1	0	0	1.132V
1	0	0	1	0	1	1.116V
1	0	0	1	1	0	1.100V
1	0	0	1	1	1	1.084V
1	0	1	0	0	0	1.068V
1	0	1	0	0	1	1.052V
1	0	1	0	1	0	1.036V
1	0	1	0	1	1	1.020V
1	0	1	1	0	0	1.004V
1	0	1	1	0	1	0.988V
1	0	1	1	1	0	0.972V
1	0	1	1	1	1	0.956V
1	1	0	0	0	0	0.940V
1	1	0	0	0	1	0.924V
1	1	0	0	1	0	0.908V
1	1	0	0	1	1	0.892V
1	1	0	1	0	0	0.876V
1	1	0	1	0	1	0.860V
1	1	0	1	1	0	0.844V
1	1	0	1	1	1	0.828V
1	1	1	0	0	0	0.812V
1	1	1	0	0	1	0.796V
1	1	1	0	1	0	0.780V
1	1	1	0	1	1	0.764V
1	1	1	1	0	0	0.748V
1	1	1	1	0	1	0.732V
1	1	1	1	1	0	0.716V
1	1	1	1	1	1	0.700V

D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.708V
0	0	0	0	0	1	1.692V
0	0	0	0	1	0	1.676V
0	0	0	0	1	1	1.660V
0	0	0	1	0	0	1.644V
0	0	0	1	0	1	1.628V
0	0	0	1	1	0	1.612V
0	0	0	1	1	1	1.596V
0	0	1	0	0	0	1.580V
0	0	1	0	0	1	1.564V
0	0	1	0	1	0	1.548V
0	0	1	0	1	1	1.532V
0	0	1	1	0	0	1.516V
0	0	1	1	0	1	1.500V
0	0	1	1	1	0	1.484V
0	0	1	1	1	1	1.468V
0	1	0	0	0	0	1.452V
0	1	0	0	0	1	1.436V
0	1	0	0	1	0	1.420V
0	1	0	0	1	1	1.404V
0	1	0	1	0	0	1.388V
0	1	0	1	0	1	1.372V
0	1	0	1	1	0	1.356V
0	1	0	1	1	1	1.340V
0	1	1	0	0	0	1.324V
0	1	1	0	0	1	1.308V
0	1	1	0	1	0	1.292V
0	1	1	0	1	1	1.276V
0	1	1	1	0	0	1.260V
0	1	1	1	0	1	1.244V
0	1	1	1	1	0	1.228V
0	1	1	1	1	1	1.212V

PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU CORE POWER	2A
Date: Monday, December 27, 2004	Sheet 33 of 39	


BATTERY CHARGER
ADAPTER 18.5V 65W 3.51A
3S2P 4400mAH
3S4P 8800mAH
Vert_C
From Docking CNN
20 MIL TO CABLE DOCK
Battery Low 7.5V
MAX1772EEI
CELL-SET
HI = LDO = 4 CELL
LOW = LDO/2 = 3 CELL
CC-SET = 1.05V/A
Charge
Current=VICTL*1.24
PROJECT : CT3
Quanta Computer Inc.
MAX1772/CHARGING
Monday, December 27, 2004

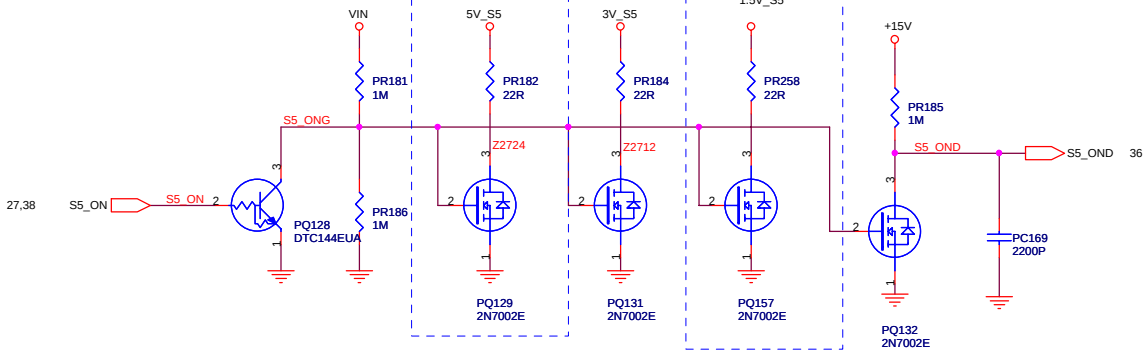


Vert_C

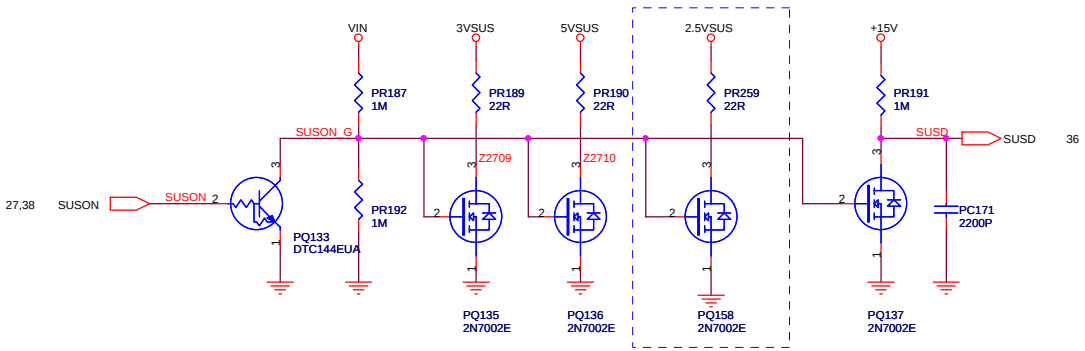
Vert_C

SI stage:
Change PR178 value from 22 ohm to 47 ohm, Intel has required the timing sequence of +1.5V and +3V in the system, we'd like to increase the value to make +3V discharge slowly to meet the specification of falling time.

Sting 10/19/2004

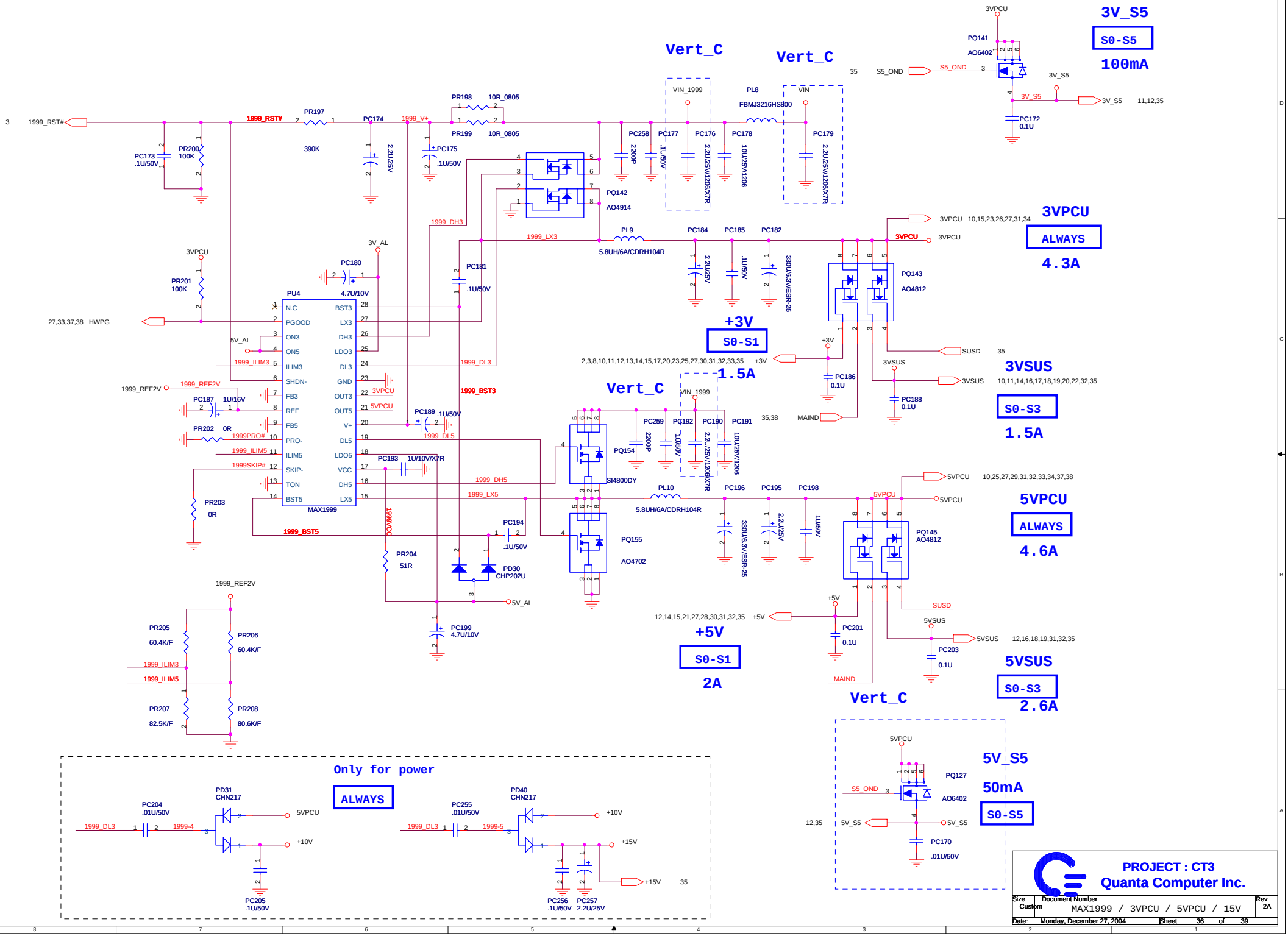


Vert_C



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE	2A
Date: Monday, December 27, 2004	Sheet 35 of 39	


3V_S5
S0-S5
100mA
Vert_C
Vert_C
3VPCU
PQ141
AO6402
S5_OND
3V_S5
PC172
0.1U
3V_S5 11,12,35
1999_RST#
1999_RST#
PR197
390K
PC174
2.2U/25V
1999_V+
PR198 10R_0805
PR199 10R_0805
PC175
.1U/50V
VIN_1999
PL8
FBMJ3216HS800
VIN
PC258 2200P
PC177 .1U/50V
PC176 22U/25V/1206/X7R
PC178 10U/25V/1206
PC179 2.2U/25V/1206/X7R
PQ142
AO4914
1999_DH3
1999_LX3
PL9
5.8UH/6A/CDRH104R
PC184
PC185 .1U/50V
PC182 330U/6.3V/ESR-25
3VPCU 10,15,23,26,27,31,34
3VPCU
3VPCU
3VPCU
ALWAYS
4.3A
PQ143
AO4812
PC180
4.7U/10V
PC181
.1U/50V
PR201
100K
3V_AL
PU4
N.C
PGOOD
ON3
ON5
ILIM3
SHDN-
FB3
REF
FB5
PRO-
ILIM5
SKIP-
TON
BST5
BST3
LX3
DH3
LDO3
DL3
GND
OUT3
OUT5
V+
DL5
LDO5
VCC
DH5
LX5
MAX1999
27,33,37,38 HWPG
5V_AL
1999_ILIM3
1999_REF2V
1999_REF2V
PC187 1U/16V
PR202 0R
1999PRO#
1999_ILIM5
1999SKIP#
PR203
0R
1999_BST3
3VPCU
5VPCU
PC189 .1U/50V
1999_DL5
PC193 1U/10V/X7R
1999_DH5
1999_LX5
1999_BST5
1999VCC
PR204
51R
PC194
.1U/50V
PD30
CHP202U
5V_AL
PC199
4.7U/10V
+3V
S0-S1
1.5A
2,3,8,10,11,12,13,14,15,17,20,23,25,27,30,31,32,33,35 +3V
PC186
0.1U
3VSUS
PC188
0.1U
SUSD 35
3VSUS
3VSUS 10,11,14,16,17,18,19,20,22,32,35
S0-S3
1.5A
Vert_C
VIN_1999
PC259 2200P
PQ154
PC192 .1U/50V
PC190 2.2U/25V/1206/X7R
PC191 10U/25V/1206
35,38
MAIND
SI4800DY
PL10
5.8UH/6A/CDRH104R
PC196
PC195 330U/6.3V/ESR-25
PC198 2.2U/25V
.1U/50V
5VPCU 10,25,27,29,31,32,33,34,37,38
5VPCU
5VPCU
5VPCU
ALWAYS
4.6A
PQ155
AO4702
PQ145
AO4812
+5V
12,14,15,21,27,28,30,31,32,35 +5V
PC201
0.1U
5VSUS
PC203
0.1U
SUSD
5VSUS
5VSUS 12,16,18,19,31,32,35
S0-S3
2.6A
MAIND
Vert_C
PR205
60.4K/F
PR206
60.4K/F
1999_ILIM3
1999_ILIM5
PR207
82.5K/F
PR208
80.6K/F
Only for power
ALWAYS
PC204
.01U/50V
PD31
CHN217
1999_DL3
1999-4
5VPCU
+10V
PC205
.1U/50V
PC255
.01U/50V
PD40
CHN217
1999_DL3
1999-5
+10V
+15V
+15V 35
PC256
.1U/50V
PC257
2.2U/25V
5VPCU
PQ127
AO6402
S5_OND
5V_S5
5V_S5
PC170
.01U/50V
5V_S5
50mA
S0+S5
12,35
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Quanta Computer Inc.
Size
Custom
Document Number
MAX1999 / 3VPCU / 5VPCU / 15V
Rev
2A
Date: Monday, December 27, 2004
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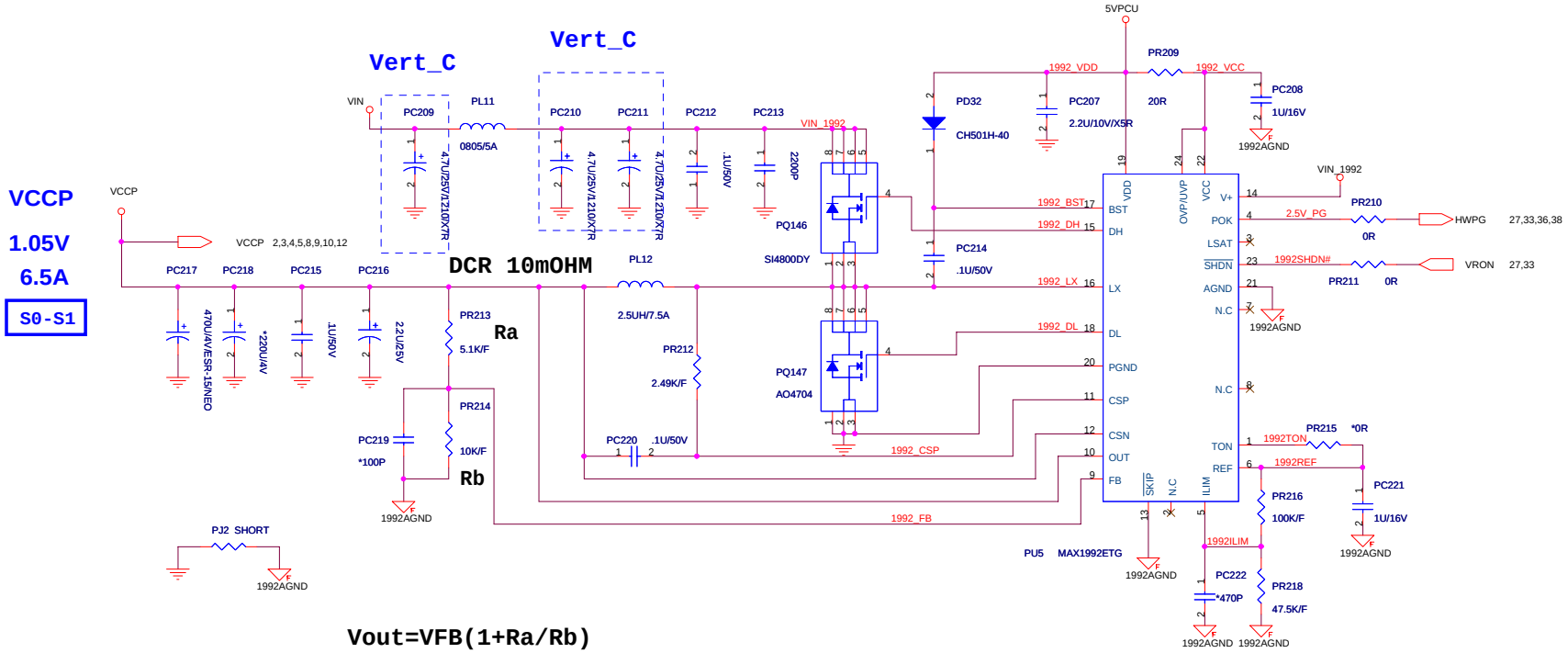

Vout=VFB(1+Ra/Rb)

#VFB=0.7V

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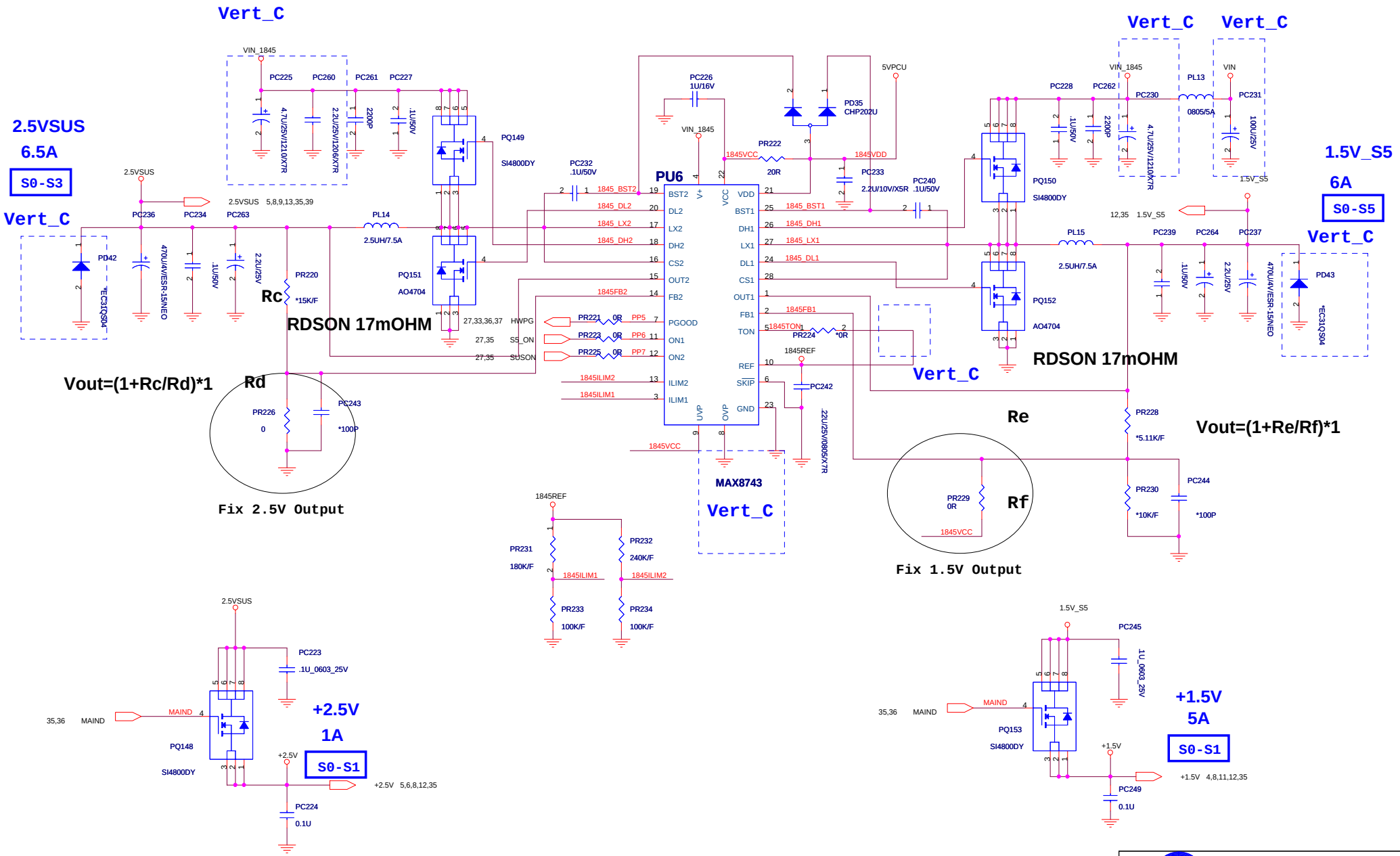

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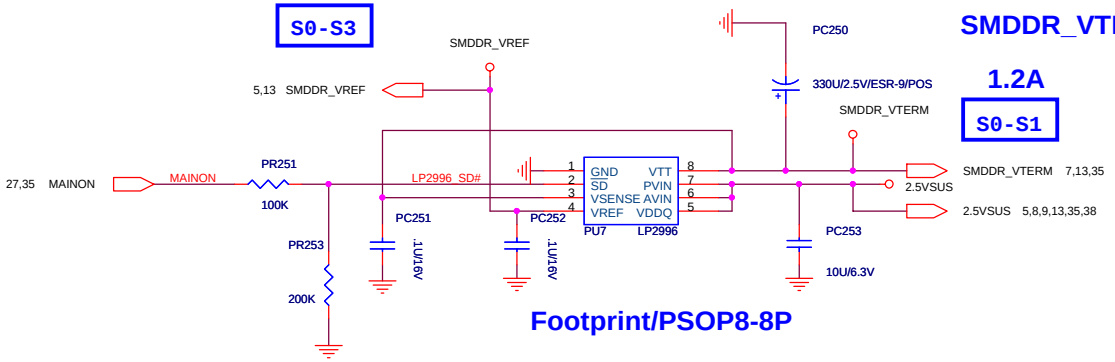
DDR

1.25V (0.2A)

S0-S3



Footprint/PSOP8-8P

SMDDR_VTERM

1.2A

S0-S1

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